



INTERNAL ASSESSMENT APPROVAL FORM (INCLUDING COLLABORATIVE PROVISION)

This form is used to ensure that assessment specifications have been through an internal review process prior to external examination/approval and release to students. It should be completed for each assessment for a particular module. The assessment tasks, criteria and marking scheme should accompany this form.

PARTNER (and taught location if relevant):	Coleg Sir Gar				
EXTERNAL EXAMINER NAME:	Dr Alison Griffiths				
ASSESSMENT AUTHOR :	Mike Hall				
MODULE TITLE:	Electronic Design				
MODULE CODE:	PSDE 6015 / SGEE6000		MODULE LEVEL:	6	
COMPONENT NO. (e.g. 1 of 2):	2 of 2		COMPONENT WEIGHTING (e.g. 50% of the module):	50%	
ASSESSMENT PERIOD	☐ Semester 1	☐ Semester 1 <i>Re-sit</i>	☒ Semester 2	☐ Semester 2 <i>Re-sit</i>	<i>Other, please state</i>
TYPE OF ASSESSMENT:	☐ Coursework		☒ Examination		☐ Practical
LANGUAGE OF ASSESSMENT:	English		TRANSLATION REQUIRED (Y/N):	N	
FOR EXAMINATIONS ONLY. SPECIFY BELOW ANY ADDITIONAL MATERIAL(S) TO BE USED IN THE EXAMINATION					
<i>This box will expand as you type</i>					

INTERNAL MODERATOR PLEASE TICK TO INDICATE THAT THE ASSESSMENT INCLUDES:		Please ✓ YES NO		Comments
1	Tasks that are specified clearly, accurately and comprehensibly, with appropriate use of language and neat presentation	✓		
2	Tasks which enable the module learning outcomes to be demonstrated (as per the module syllabus)	✓		
3	Tasks which conform to the assessment described in the module syllabus	✓		
4	Tasks which are written at the appropriate level of the Framework for Higher Education Qualifications (see http://www.qaa.ac.uk/docs/qaa/quality-code/qualifications-frameworks.pdf?sfvrsn=170af781_14).	✓		
5	Clear criteria for assessment and guidance about how marking/grading will be applied	✓		
6	Guidance about expected evidence for submission, e.g. essay or report, word count, bibliography and references	✓		
7	Reference to good academic conduct, for example referencing, plagiarism and Turnitin	✓		
8	Actions to complete <i>This box will expand as you type</i>			
SIGNATURE OF APPROVAL:		SIGNATURE		DATE
INTERNAL MODERATOR: I confirm that this version of the assessment specification is ready to be sent to the Partnership Team Leader				04/04/2019

ONLY TO BE COMPLETED IF THE ASSESSMENT IS LINKED TO A COLLABORATIVE PARTNER

PARTNERSHIP TEAM LEADER PLEASE TICK TO INDICATE THAT THE ASSESSMENT INCLUDES:		Please ✓		Comments
		YES	NO	
1	Tasks that are specified clearly, accurately and comprehensibly, with appropriate use of language and neat presentation			
2	Tasks which enable the module learning outcomes to be demonstrated (as per the module syllabus)			
3	Tasks which conform to the assessment described in the module syllabus			
4	Tasks which are written at the appropriate level of the Framework for Higher Education Qualifications (see http://www.qaa.ac.uk/docs/qaa/quality-code/qualifications-frameworks.pdf?sfvrsn=170af781_14).			
5	Clear criteria for assessment and guidance about how marking/grading will be applied			
6	Guidance about expected evidence for submission, e.g. essay or report, word count, bibliography and references			
7	Reference to good academic conduct, for example referencing, plagiarism and Turnitin			
8	Actions to complete <i>This box will expand as you type</i>			
SIGNATURE OF APPROVAL:		SIGNATURE		DATE
PTL: I confirm that this version of the assessment specification is ready to be sent to the External Examiner				

UWTSD PROVISION: please submit the completed document to the appropriate Programme Director.

COLLABORATIVE PROVISION: please submit the completed document (or make available electronically) to the Partnership Team Leader. This must be in accord with specific arrangements for sharing electronic documents (e.g. via SharePoint or similar).

The assessment tasks, criteria and marking scheme should accompany this form

LOCATION: COLEG SIR GAR

LLEOLIAD: COLEG SIR GAR

LEVEL 6

LEFEL 6

**EXAMINATION PERIOD
MAY 2019**

**CYFNOD ARHOLIADAU
MAI 2019**

MODULE CODE: PSDE 6015 / SGEE6000

Electronic Design

TIME: 2½ HOURS

THIS PAPER IS IN 2 PARTS:

ANSWER ALL QUESTIONS IN PART A

ANSWER TWO QUESTIONS OUT OF THREE IN PART B

Equipment or materials required – Calculator

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Formulae

$$\text{Voltage Regulation} = \frac{V_{no-load} - V_{full-load}}{V_{full-load}}$$

$$I_{L(max)} = \frac{V_Z}{R_{L(min)}}$$

$$R_{S(max)} = \frac{V_{in} - V_Z}{I_{L(max)} + I_{Z(min)}}$$

$$R_S = \frac{V_{in} - V_Z}{I_B + I_Z}$$

$$T_A = T_J - P_D \theta_{JA}$$

$$\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA}$$

$$T_S = T_J - (\theta_{JC} \times P_d)$$

$$h_c = 2.21 \times 10^{-3} \left(\frac{T_s - T_A}{H} \right)^{\frac{1}{4}}$$

$$h_r = 1.47 \times 10^{-10} \times \varepsilon \left(\frac{T_s + T_A}{2} + 273 \right)^3$$

$$\theta_{SA} = \frac{1}{2 \times H^2 \times \eta \times h}$$

$$I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_{GS(off)}} \right]^2$$

$$V_{DS} = V_{DD} - I_{DSS} R_D$$

$$MTBF = \frac{e^{\frac{tr}{\tau}}}{T_0 \times f \times a}$$

PART A – Answer ALL 8 questions.

- A1. Determine the maximum allowable value of R_S for the zener voltage regulator circuit shown in Figure A1 given that $V_{in} = 10V$, $V_Z = 2.5V$, $I_{Z(min)} = 1.2mA$ and R_L is variable between $1k\Omega$ and $2k\Omega$.

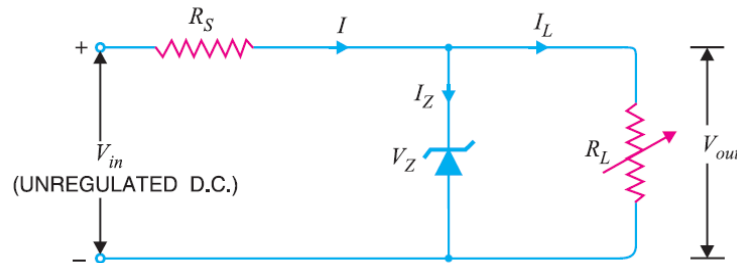


Figure A1

(4 marks)

- A2. Show how the voltage regulator circuit shown in Figure A2 achieves a stable output:

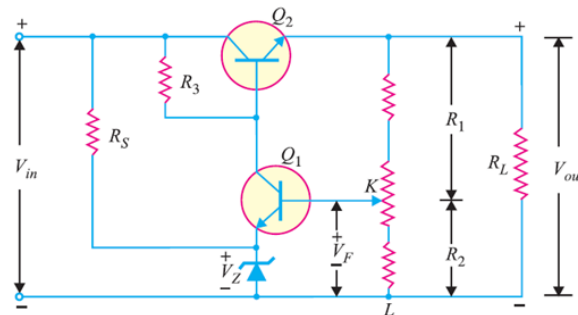


Figure A2

(6 marks)

- A3. Discuss the principle of a switch mode power supply and explain how voltage regulation is generally achieved.

(5 marks)

- A4. A MC7809CT voltage regulator in a TO-220 case is required to dissipate 500mW at a desired junction temperature of $100^{\circ}C$. From the datasheet, θ_{JA} is $180^{\circ}C/W$, $\theta_{cs} = 1.6^{\circ}C/W$ and θ_{JC} is $2.5^{\circ}C/W$.

- i. Determine whether a heat-sink is required for the regulator to operate at normal room temperature ($22^{\circ}C$).
- ii. If the power output was increased to 5W and all other factors remain the same, calculate the required heat-sink. The IC is to be mounted with heatsink compound with a θ_{CS} of $1.6^{\circ}C/W$.

(6 marks)

A5. Explain with the aid of a diagram the operation of a N-channel depletion mode MOSFET.
(6 marks)

A6. Compare and contrast JFETs and bipolar transistors.
(4 marks)

A7. Show how an OR gate may be implemented on a PLD by showing the arrangement of the fusable links.
(3 marks)

A8. Evaluate three considerations which must be taken into account when selecting which type of ASIC to choose for a specific design?
(6 marks)

Total Marks for Part A = 40

PART B – Only answer 2 of the following 3 questions (B1, B2, B3)

Question B1 – Power Supply Design and Thermal Management

- a. A series voltage regulator shown in Figure B1.1 is required to supply a current of 1.2A at a constant voltage of 6V. If the input voltage is 15V, $\beta = 50$, $V_{BE} = 0.6V$ and minimum zener current = 5.6mA. Calculate:

- The zener breakdown voltage
- The value for R_S

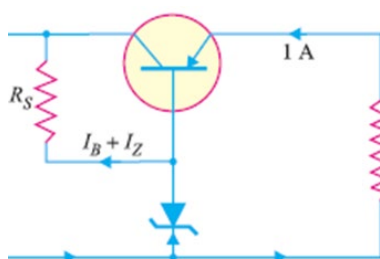


Figure B1.1

(6 marks)

- b. Explain the operation of the current limiting circuit shown in Figure B1.2.

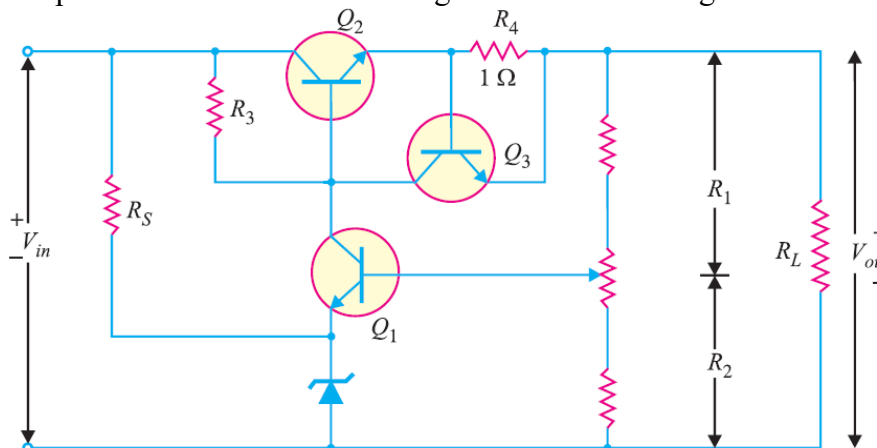


Figure B1.2

(5 marks)

- c. A vertical heat sink solution is required for an IC delivering 5W in an environment with an ambient temperature of 60°C. A 3" square and a 2" square fin of 0.01" oxidised copper is available with an emissivity of 0.7. For each heat sink, determine the value of θ_{SA} and state which is most appropriate for the application given that $T_J = 130^\circ\text{C}$, $\theta_{JC} = 2.5^\circ\text{C/W}$ and $\theta_{CS} = 1.6^\circ\text{C/W}$. A nomograph is included at the end of this paper. **(Remove it and insert it into your answer book)**

(14 marks)

- d. Discuss the operation of the 'boost' converter shown in Figure B1.3.

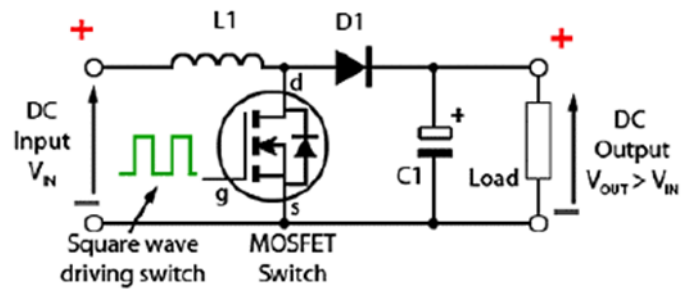


Figure B1.3

(5 marks)

Total Marks for Question B1 = 30

Question B2 – FETs and PLDs

- Explain the principle of operation of a JFET
(5 marks)
- A JFET has a drain current of 8mA. If $I_{DSS} = 12\text{mA}$ and $V_{GS(\text{off})} = -4.5\text{V}$, find the value of V_{GS} .
(4 marks)
- Discuss the term metastability in FPGA design and how it can occur.
(5 marks)
- The circuit shown in Figure B2.1 has two identical flip-flops which are clocked at 20MHz. The synchronising flip-flop is sampling an asynchronous 2MHz input.
(5 marks)

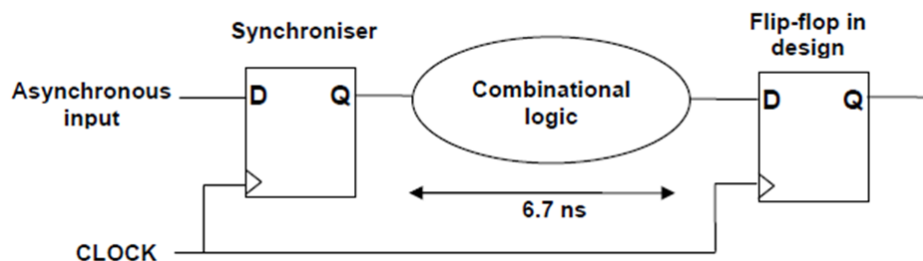


Figure B2.1

Given that:

$$\tau = 0.2\text{ns},$$

$$T_o = 9.6 \times 10^{-18} \text{ s}$$

$$t_{su} = 1\text{ns}$$

- Calculate the resolution time and MTBF of the circuit.
- If the clock frequency in the circuit above is quadrupled, calculate the effect on MTBF and comment on its change.
- Show how the circuit can be redesigned to improve the MTBF. Give an expression to estimate the new MTBF and calculate the new value. Use the quadrupled clock frequency.

(16 marks)

Total Marks for Question B2 = 30

Question B3 – VHDL and ASIC Technology

- a. Evaluate the four main types of Application Specific Integrated Circuits (ASIC). (8 marks)
- b. Compare the following coding methods:
i. Gray State Encoding
ii. One-hot State Encoding (6 marks)
- c. Compare block diagrams representing the design flow for an ASIC and the design flow for a Field Programmable Gate Array (FPGA). (8 marks)
- d. For the the VHDL file shown below:
i. What are the inputs to the device “Gate 1” and what are outputs?
ii. Draw an entity of this device.
iii. Explain the operation of the device with the aid of a truth table and suggest a use for this device in digital communication.

(8 marks)

```
library IEEE;  
use IEEE.STD_LOGIC_1164.ALL;
```

```
entity Gate 1 is  
port (  
  A : in STD_LOGIC;  
  B : in STD_LOGIC;  
  C : in STD_LOGIC;  
  D : in STD_LOGIC;  
  LT : in STD_LOGIC;  
  RBI : in STD_LOGIC;  
  BI : in STD_LOGIC;  
  Y0 : out STD_LOGIC;  
  Y1 : out STD_LOGIC;  
  Y2 : out STD_LOGIC;  
  Y3 : out STD_LOGIC;  
  Y4 : out STD_LOGIC;  
  Y5 : out STD_LOGIC;  
  Y6 : out STD_LOGIC;  
);  
end Gate 1;
```

```

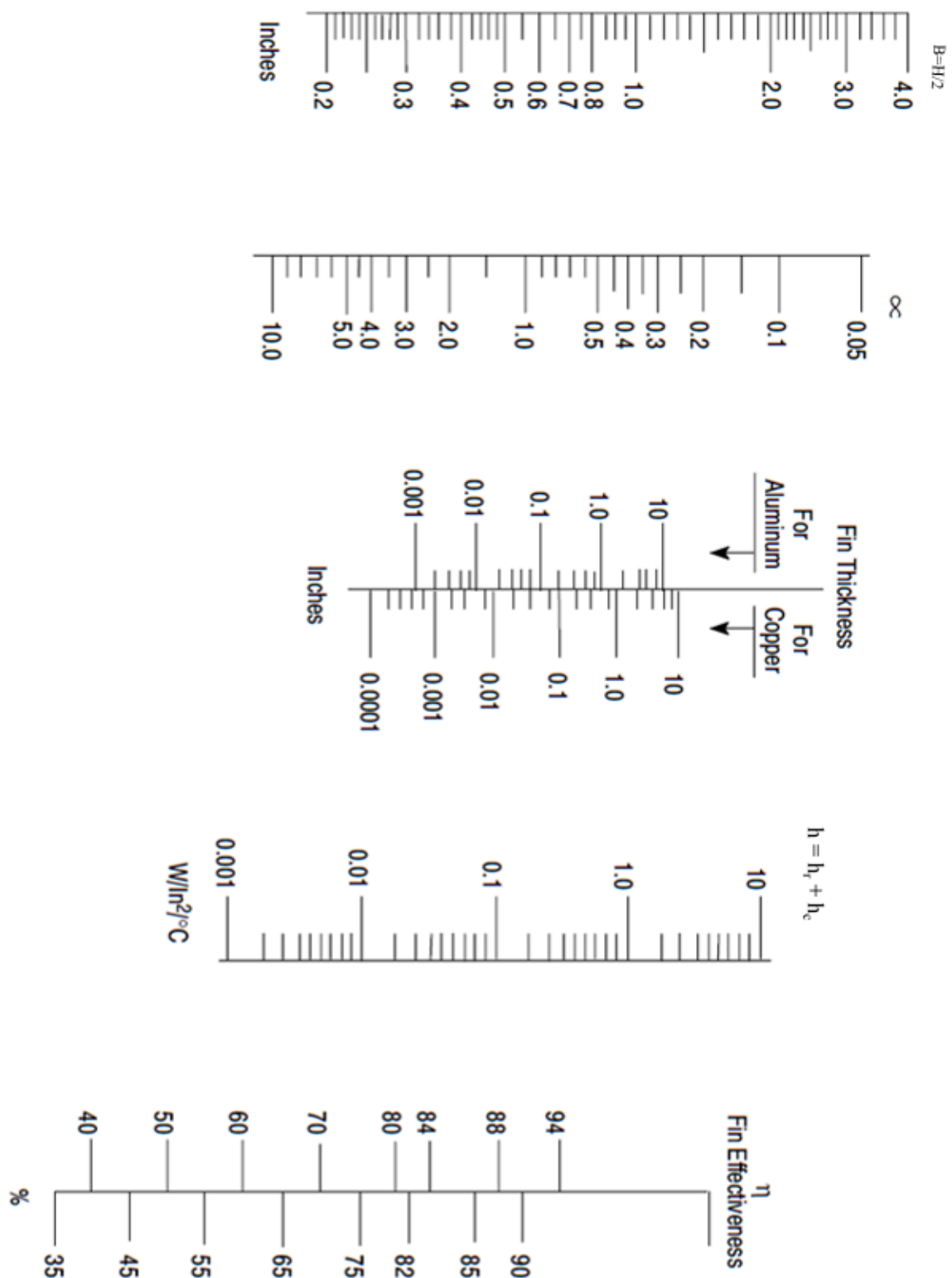
architecture BEHAVIORAL of Gate 1 is
signal O : STD_LOGIC_VECTOR(0 TO 6);
begin
process (BI,LT,RBI,A,B,C,D)
begin
if BI='0' then O<="1111111";
elsif LT='0' then O<="0000000";
elsif (A='0' and B='0' and C='0' and D='0' and RBI='1') then O<="0000001";
elsif (A='1' and B='0' and C='0' and D='0') then O<="1001111";
elsif (A='0' and B='1' and C='0' and D='0') then O<="0010010";
elsif (A='1' and B='1' and C='0' and D='0') then O<="0000110";
elsif (A='0' and B='0' and C='1' and D='0') then O<="1001100";
elsif (A='1' and B='0' and C='1' and D='0') then O<="0100100";
elsif (A='0' and B='1' and C='1' and D='0') then O<="1100000";
elsif (A='1' and B='1' and C='1' and D='0') then O<="0001111";
elsif (A='0' and B='0' and C='0' and D='1') then O<="0000000";
elsif (A='1' and B='0' and C='0' and D='1') then O<="0001100";
elsif (A='0' and B='1' and C='0' and D='1') then O<="1110010";
elsif (A='1' and B='1' and C='0' and D='1') then O<="1100110";
elsif (A='0' and B='0' and C='1' and D='1') then O<="1011100";
elsif (A='1' and B='0' and C='1' and D='1') then O<="0110100";
elsif (A='0' and B='1' and C='1' and D='1') then O<="1110000";
elsif (A='1' and B='1' and C='1' and D='1') then O<="1111111";
end if;
end process;
Y6<=O(6);
Y5<=O(5);
Y4<=O(4);
Y3<=O(3);
Y2<=O(2);
Y1<=O(1);
Y0<=O(0);
end BEHAVIORAL;

```

Total Marks for Question B3 = 30

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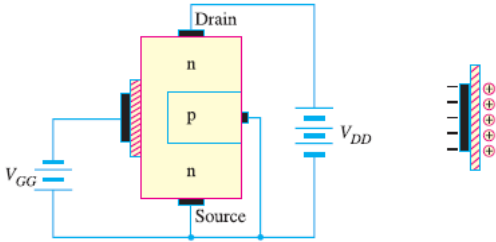




EXAMINATION SOLUTIONS
(to accompany the examination paper sent to the external examiner
but NOT to be seen by students)

Programme:	BSc in Electrical & Electronic Engineering	Level:	6
Module:	PSDE 6015 / SGEE6000 Electronic Design		
Author:	M Hall	Page:	Page 1 of

Part A	Question	Marks
A1	$I_{L(max)} = \frac{V_Z}{R_{L(min)}} = \frac{2.5}{1000} = 2.5mA$	2
	$R_{S(max)} = \frac{V_{in} - V_Z}{I_{L(max)} + I_{Z(min)}} = \frac{10 - 2.5}{2.5m + 1.2m} = \mathbf{2k\Omega}$	2
A2	The unregulated DC supply is fed to the voltage regulator. The circuit maintains a constant output voltage irrespective of the variations in load or input voltage. It does this in the following way: Suppose the output voltage increases due to any reason. This causes an increase in voltage across R2 as it is a part of the output circuit. This in turn means that more VF is fed back to the base of transistor Q1; producing a large collector current in Q1. Most of this collector current flows through R3 and causes the base voltage of Q2 to decrease. This results in less output voltage i.e. increase in voltage is offset. Thus output voltage remains constant. Similarly, if the output voltage tries to decrease, the feedback voltage VF also decreases. This reduces the current through Q1 and R3. This means more base voltage at Q2 and more output voltage. Consequently, the output voltage remains at the original level.	6
A3	A SMPS uses a high frequency square wave to drive an electronic power switching circuit. This circuit is used to convert the DC supply into a high frequency, high current AC, which by various means, depending on the design of the circuit, is reconverted into a regulated DC output. The high frequency AC produced during the conversion process is a square wave, which provides a means of controlling the output voltage by means of pulse width modulation.	

	This allows the regulation of the output to be much more efficient than is possible in linear regulated supplies. Voltage Regulation This is achieved by altering the mark to space ratio of the oscillator waveform before applying it to the switches. Control of the mark to space ratio is achieved by comparing voltage feedback from the output of the supply with a stable reference voltage. By using this feedback to control the mark to space ratio of the oscillator, the duty cycle and therefore the average DC output of the circuit can be controlled.	3 2
A4	$T_A = T_J - P_D \phi_{JA}$ $T_A = 100 - (500m \times 180) = 10^{\circ}C$ Since $T_A = 10^{\circ}C$ a heatsink is required. $\phi_{SA} = \frac{T_J - T_A}{P_D} - \phi_{JC} - \phi_{CS}$ $\phi_{SA} = \frac{100 - 22}{5} - 2.5 - 1.6 = 11.5^{\circ}C/W$ Therefore a $11.5^{\circ}C/W$ heatsink is required.	3 2 1
A5	The diagram below shows a depletion-mode n-channel MOSFET. Since the gate is negative, it means electrons are on the gate as shown. These electrons repel the free electrons in the n-channel, leaving a layer of positive ions in a part of the channel. In other words, we have depleted the n-channel of some of its free electrons. Therefore, lesser number of free electrons are made available for current conduction through the n-channel. This is the same thing as if the resistance of the channel is increased. The greater the negative voltage on the gate, the lesser is the current from source to drain. Thus by changing the negative voltage on the gate, we can vary the resistance of the n-channel and hence the current from source to drain. Because the action with negative gate depends upon depleting the channel of free electrons, the negative-gate operation is called depletion mode. 	6

A6

Any 4 from following 5

They have a very high input impedance (of the order of 100MΩ). This permits high degree of isolation between the input and output circuits.

The operation of a JFET depends upon the bulk material current carriers that do not cross junctions. Therefore, the inherent noise of tubes (due to high-temperature operation) and those of transistors (due to junction transitions) are not present in a JFET.

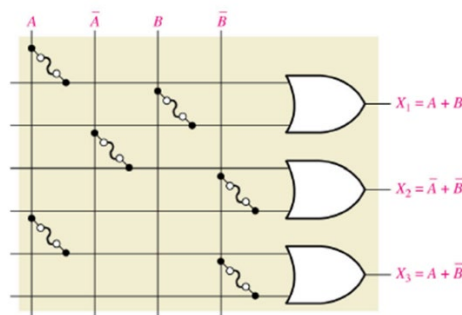
A JFET has a negative temperature co-efficient of resistance. This avoids the risk of thermal runaway.

A JFET has a very high power gain. This eliminates the necessity of using driver stages.

A JFET has a smaller size, longer life and high efficiency.

4

A7



3

A8

Any 3 from following 4

Time to Market

Time to market is a primary driver

Dramatic increase in profit with earlier time-to-market landing

Cutting one month off schedule increases profit roughly 10%

Cost

Standard cell synthesis can cost £125k per license

Typical standard cell non-recurring engineering (NRE) costs are £50K to £200K

If you can't spend at least a million, you are not in the game

One bug in a standard cell design can be a disaster

A standard cell "re-spin" takes possibly 8 weeks and a lot of money

Really cheap tools are available for FPGA implementation – free!

FPGAs cost £10-100 each in single quantity

FPGA bugs are fixed at zero cost in minutes

	<u>Technical Feasibility</u> Can it run fast enough? Is it low enough power? Can it operate at 1.2V? Is the required IP (Intellectual Property) available? <u>Financial Analysis</u> What is the cost to get first prototypes (NRE) What is the volume piece part price? How many will we ship? How much market share would we lose?	2 each (6 total)
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Q. B1	Question	Marks
a.	$V_Z = V_{out} - V_{BE} = 6 - 0.6 = 5.4V$	2
	$R_S = \frac{V_{in} - V_Z}{I_B + I_Z} \quad \text{Where } I_B = \frac{I_C}{\beta} = \frac{1.2}{50} = 24mA$	1
	$R_S = \frac{15 - 5.4}{24m + 5.6m} = 324\Omega$	3
b.	The main drawback of any series regulator is that the pass transistor can be destroyed by excessive load current if the load is accidentally shorted. To avoid such an eventuality, a current limiting circuit is added to a series regulator. A current limiting circuit consists of a transistor (Q3) and a series resistor (R4) that is connected between base and emitter terminals. When the load current is normal, the voltage across R4 equals the voltage across base-emitter of Q3 and Q3 is biased off. Under this condition, the circuit works as normal. If load current becomes excessive, the voltage across R4 becomes large enough to turn on Q3. The collector current of Q3 flows through R3, thereby decreasing the base voltage of Q2. The decrease in base voltage of Q2 reduces the conduction of pass transistor Q2, preventing any further increase in load current. Thus, the load current for the circuit is limited.	5
c.	$\phi_{JA} = \frac{T_J - T_A}{P_D}$	
	$\phi_{JA} = \frac{130 - 60}{5} = 14^\circ C/W$	
	$\text{Required } \phi_{SA} = \phi_{JA} - \phi_{CS} - \phi_{JC}$	
	$= 14 - 1.6 - 2.5 = 9.9^\circ C/W$	2
	$T_S = T_J - (\phi_{JC} \times P_d) = 130 - (2.5 \times 5) = 117.5^\circ C$	1
	$h_r = 1.47 \times 10^{-10} \times \varepsilon \left(\frac{T_s + T_A}{2} + 273 \right)^3$	
	$= 1.47 \times 10^{-10} \times 0.7 \left(\frac{117.5 + 60}{2} + 273 \right)^3 = 4.87 \times 10^{-3} W/^\circ C m^2$	2
	<u>For 3" sink.</u>	
	$h_c = 2.21 \times 10^{-3} \left(\frac{T_s - T_A}{H} \right)^{\frac{1}{4}}$	

$$= 2.21 \times 10^{-3} \left(\frac{117.5 - 60}{3} \right)^{\frac{1}{4}} = 4.62 \times 10^{-3} W/^{\circ}Cm^2$$

3

$$h = h_r + h_c = 4.87 \times 10^{-3} + 4.62 \times 10^{-3} = 9.49 \times 10^{-3} W/^{\circ}Cm^2$$

1

From nomograph

$$\alpha = 0.41$$

$$B = H/2 = 3/2 = 1.5$$

$$\eta = 75\%$$

$$\phi_{SA} = \frac{1}{2H^2 \times \eta \times h} = \frac{1}{2 \times 3^2 \times 0.75 \times 9.49 \times 10^{-3}} = 7.8^{\circ}C/W$$

1

For 2" sink.

$$h_c = 2.21 \times 10^{-3} \left(\frac{T_s - T_A}{H} \right)^{\frac{1}{4}}$$

$$= 2.21 \times 10^{-3} \left(\frac{117 - 60}{2} \right)^{\frac{1}{4}} = 5.1 \times 10^{-3} W/^{\circ}Cm^2$$

1

$$h = h_r + h_c = 4.87 \times 10^{-3} + 5.1 \times 10^{-3} = 9.97 \times 10^{-3} W/^{\circ}Cm^2$$

1

From nomograph

$$\alpha = 0.5$$

$$B = H/2 = 2/2 = 1$$

$$\eta = 90\%$$

$$\phi_{SA} = \frac{1}{2H^2 \times \eta \times h} = \frac{1}{2 \times 2^2 \times 0.9 \times 9.97 \times 10^{-3}} = 13.93^{\circ}C/W$$

1

The 3" sink is therefore the better option

1

d. Although a DC supply, such as a battery may be available, its available voltage is not always suitable. For example, the motors used in driving electric cars require much higher voltages than could be supplied by a battery alone. The answer is to boost the available DC voltage to the required level by using a boost converter. Another problem with batteries is that their output voltage varies as the available charge is used up, and at some point the battery voltage becomes too low to power the circuit being supplied. However, if this low output level can be boosted back up to a useful level again, the life of the battery can be extended.

During the initial ON period of the high frequency square wave the MOSFET conducts, placing a short circuit from the right hand side of L1 to the negative input supply terminal. Therefore a current flows between the positive and negative supply terminals through the inductor, which stores energy. There is virtually no current flowing in the remainder of the circuit as the combination of diode, capacitor and the load represent a much higher impedance than the path directly through the heavily conducting MOSFET.

During the OFF period of the switching square wave cycle the MOSFET is rapidly turned off, the sudden drop in current causes the inductor to produce a back e.m.f. in the opposite polarity to the voltage across the inductor during the on period, to keep current flowing. This results in two voltages, the supply voltage and the back e.m.f. across the inductor.

This higher voltage, forward biases the diode and the resulting current charges up the capacitor to $V_{IN} + V_L$.

Q.B2	Question	Marks
a.	The two PN junctions at the sides form two depletion layers. The current conduction of charge carriers (i.e. free electrons in this case) is through the channel between the two depletion layers and out of the drain. The width and hence resistance of this channel can be controlled by changing the input voltage V_{GS}. The greater the reverse voltage V_{GS}, the wider will be the depletion layers and narrower will be the conducting channel. The narrower channel means greater resistance and hence source to drain current decreases. Reverse will happen should V_{GS} decrease. Thus JFET operates on the principle that width and hence resistance of the conducting channel can be varied by changing the reverse voltage V_{GS}.	5
b.	$I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_{GS(off)}} \right]^2$ $V_{GS} = V_{GS(off)} \left[1 - \sqrt{\frac{I_D}{I_{DSS}}} \right] = -4.5 \left[1 - \sqrt{\frac{8m}{12m}} \right] = -0.83V$	4
c.	Metastability within an FPGA design will typically occur in one of two ways: When an incoming signal is asynchronous with regard to the clock domain. This may be an external input signal or a signal crossing between clock domains. In this case, the design engineer is expected to resynchronise the signal to address metastability, which is certain to occur eventually. This is where a multi-stage synchroniser is typically employed. When multiple register elements in a synchronous design are using the same clock, but phase alignments or clock skew issues mean that the output from one register violates another register's setup and hold time. This may be addressed by modifying the place-and-route constraints or by changing the logic design itself.	5
d.	Given: f_{clk} = 20MHz, t_{clk} = 50 ns a = 2MHz t_{prop} = 6.7ns τ = 0.2nS T_o = 9.6 x 10⁻¹⁸ S t_{setup} = 1ns Resolution time: $t_r = t_{clk} - t_{setup} - t_{prop}$ = (50ns – 1ns – 6.7ns) = <u>42.3ns</u>	2

$$MTBF = \frac{e^{\frac{t_r}{\tau}}}{T_o \times f_{clk} \times a}$$

$$MTBF = \frac{e^{\frac{42.3n}{0.2n}}}{(9.6 \times 10^{-18}) \times (20 \times 10^6) \times (2 \times 10^6)} = \frac{e^{211.5}}{384u} = 1.86 \times 10^{95} S$$

Equivalent to 5.89×10^{40} years

Quadrupling the clock frequency

Given:

$F_{clk} = 80\text{MHz}$, $t_{clk} = 12.5\text{ns}$

Resolution time: $t_r = t_{clk} - t_{setup} - t_{prop}$

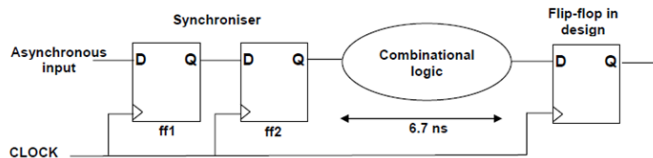
$$= (12.5\text{ns} - 1\text{ns} - 6.7\text{ns})$$

$$= 4.8\text{ns}$$

$$MTBF = \frac{e^{\frac{t_r}{\tau}}}{T_o \times f_{clk} \times a}$$

$$MTBF = \frac{e^{\frac{4.8n}{0.2n}}}{(9.6 \times 10^{-18}) \times (80 \times 10^6) \times (2 \times 10^6)} = \frac{e^{24}}{1.536m} = 1.725 \times 10^{13} S$$

Equivalent to 546852 years.



$$MTBF = \left\{ \frac{e^{\frac{t_r}{\tau}}}{T_o \times f_{clk} \times a} \right\} \times k \left\{ \frac{e^{\frac{t_r}{\tau}}}{T_o \times f_{clk}} \right\}$$

Where $k = 1$ for one extra flip-flop

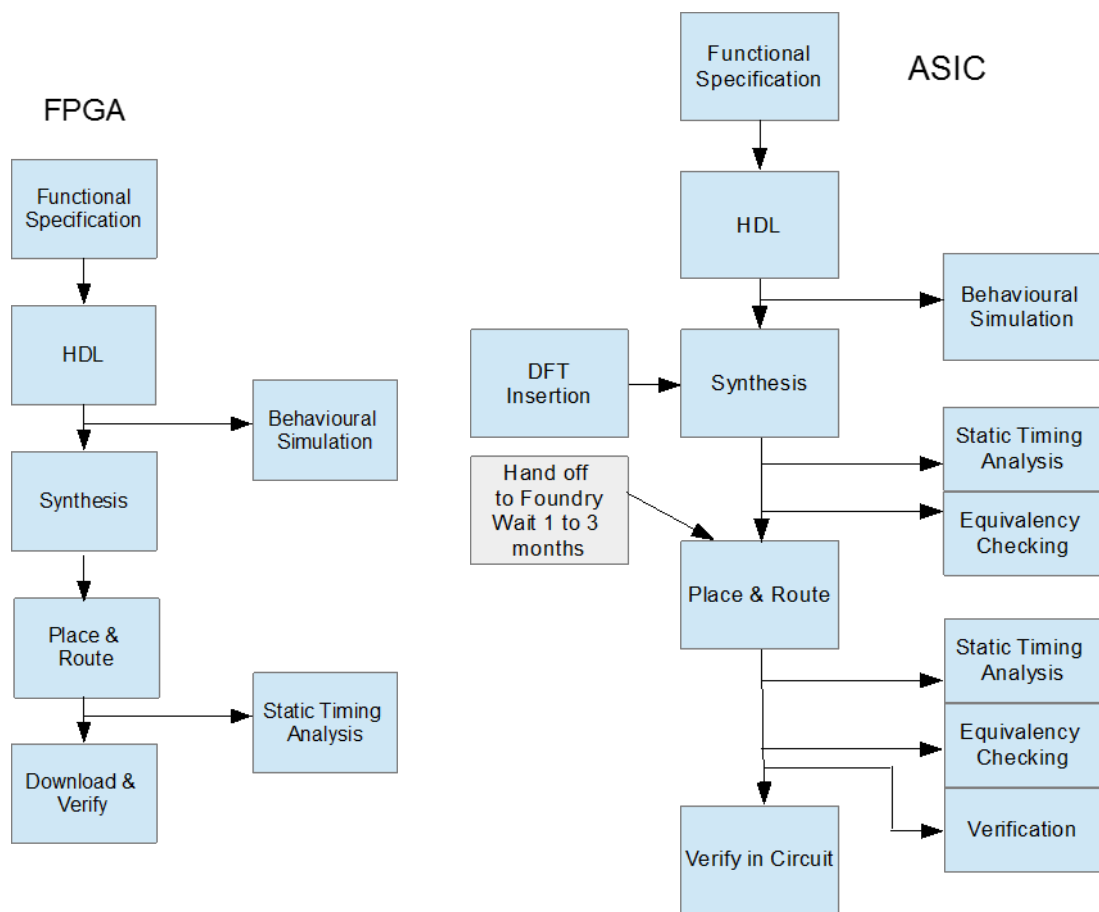
$$MTBF = \left\{ \frac{e^{\frac{4.8n}{0.2n}}}{(9.6 \times 10^{-18}) \times (80 \times 10^6) \times (2 \times 10^6)} \right\} \times \left\{ \frac{e^{\frac{4.8n}{0.2n}}}{(9.6 \times 10^{-18}) \times (80 \times 10^6)} \right\}$$

New MTBF = $5.95 \times 10^{32} S$

Equivalent = 1.89×10^{25} years

Q. B3	Question	Marks
a.	<u>Full Custom</u> Each transistor is hand drawn Analogue parts are done this way Highest performance, longest design time Hand optimized parts of high-end uPs Full set of masks needed <u>Standard Cell ASIC</u> Predesigned (standard) cells in a library are used These cells are connected together to form the design High performance, much shorter design time than full custom Most digital ASICs are designed this way Usually uses HDLs with logic synthesis Full set of masks needed <u>Gate Array ASIC</u> Pre-drawn transistors are on a die These transistors are connected together to form cells The cells are connected to form a design Usually digital in nature Lower performance, but very quick to fabricate Only metallization masks are needed Usually uses HDLs with logic synthesis	2 2 2
	<u>FPGA ASIC</u> Fully predesigned silicon, logic functions and interconnect Programmed with a "bit file" to configure logic and interconnect Medium performance, higher power consumption Very quick to implement, minutes Better for more limited volume applications Almost always uses HDLs plus logic synthesis No DFT structures required Popular for ASIC prototyping	2
	b. Gray State Encoding Guarantees that only one bit switches between two consecutive states. It is appropriate for controllers exhibiting long paths without branching. Minimizes hazards and glitches. Good results can be obtained when implementing the state register with T flip-flops. Can be used to minimize power dissipation.	3
	One-hot State Encoding One-Hot State Encoding is the default encoding scheme. It assigns a distinct bit of code to each FSM state. As a result, the state register is implemented with one flip-flop for each state. In a given clock cycle during operation, one and only one bit of the state register is asserted. Only two bits toggle during a transition between two states. One-Hot State Encoding is usually a good choice for optimizing speed or reducing power dissipation.	3

c.



8

d.

Inputs to the Design

A : in STD_LOGIC;
 B : in STD_LOGIC;
 C : in STD_LOGIC;
 D : in STD_LOGIC;
 LT : in STD_LOGIC;
 RBI : in STD_LOGIC;
 BI : in STD_LOGIC;

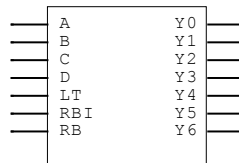
Outputs from the Design

Y0 : out STD_LOGIC
 Y1 : out STD_LOGIC
 Y2 : out STD_LOGIC
 Y3 : out STD_LOGIC
 Y4 : out STD_LOGIC
 Y5 : out STD_LOGIC
 Y6 : out STD_LOGIC

1

1

Entity Block Diagram



2

The VHDL file converts a binary/hex code into the corresponding digit on a 7 segment display. LT is the lamp test input which turns all LEDs on to check they work. RB and RBI are ripple blanks which can be used to turn off unwanted displays in a multi digit system.

DEC NO.	INPUTS							OUTPUTS						
	LT	RBI	D	C	B	A	BI/RBO	OA	OB	OC	OD	OE	OF	OG
0	H	H	L	L	L	L	H	L	L	L	L	L	L	H
1	H	X	L	L	L	H	H	H	L	L	H	H	H	H
2	H	X	L	L	H	L	H	L	L	H	L	L	H	L
3	H	X	L	L	H	H	H	L	L	L	L	H	H	L
4	H	X	L	H	L	L	H	H	L	L	H	H	L	L
5	H	X	L	H	L	H	H	L	H	L	L	H	L	L
6	H	X	L	H	H	L	H	H	H	L	L	L	L	L
7	H	X	L	H	H	H	H	L	L	L	H	H	H	H
8	H	X	H	L	L	L	H	L	L	L	L	L	L	L
9	H	X	H	L	L	H	H	L	L	L	H	H	L	L
10	H	X	H	L	H	L	H	H	H	H	L	L	H	L
11	H	X	H	L	H	H	H	H	H	L	L	H	H	L
12	H	X	H	H	L	L	H	H	L	H	H	H	L	L
13	H	X	H	H	L	H	H	L	H	H	L	H	L	L
14	H	X	H	H	H	L	H	H	H	H	L	L	L	L
15	H	X	H	H	H	H	H	H	H	H	H	H	H	H
BI	X	X	X	X	X	X	L	H	H	H	H	H	H	H
RBI	H	L	L	L	L	L	L	H	H	H	H	H	H	H
LT	L	X	X	X	X	X	H	L	L	L	L	L	L	L

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