



SURNAME: Williams

FORENAME(S): Alex

12 Pages

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2. Enter your name in the space provided to the right, fold over and seal down (using the label provided) to hide your name.
3. The answers must be legibly written. The Examiners can either ignore illegible script or have it typed and the expense of typing charged to the candidate.
4. Write your answers in ink.
5. Begin each answer on a fresh page. Do all rough work in the answer book and cross it through.
6. No part of this book is to be torn out; it must be handed in complete.
7. If more books than one are used, fasten them together using the tags available from the invigilator(s).
8. **Every book must be handed in. In no circumstances may answer books, used or unused, be taken out of the examination venue.**

1	Student Number	
2	Title of Examination Paper	Elec. Production and Test
3	Module Code	SGEE 6002
4	Date and Time of Examination	19/05/23 9:30
5	Examination Venue	Colleg Sir gor
6	Seat Number	
7	Number of Answer Books handed in	

List the numbers of the questions you have attempted	Office Use
1	20
2	24
4	14
3	0
Total	58%

(Gweler yr ochr arall am y fersiwn Cymraeg)

MARK
AGREED.
58%.



Prifysgol Cymru
Y Drindod Dewi Sant
University of Wales
Trinity Saint David

Llyfr Atebion Arholiadau

12 Tudalen

Cyfarwyddiadau i Ymgeiswyr

1. Rhwch yr holl wybodaeth y gofynnir amdani yn y blychau isod.
2. Rhwch eich enw yn y lle a ddarparwyd ar y dde, plynwch ef a'i seilio i lawr (gan ddefnyddio'r label a ddarparwyd) i guddio'ch enw.

3. Rhaid i'r atebion fod mewn llawysgriften ddarlennadwy. Gall yr Arholwyr naill ai anwybyddu sgript annarllennadwy, neu drefnu iddi gael ei theipio a chael yr ymgeisydd i dalu.
4. Ysgrifennwch eich atebion mewn inc.
5. Dechreuwch bob ateb ar dudalen newydd. Gwnewch unrhyw fras nodiadau yn y llyfr atebion a thynnu llinell drwyddynt.
6. Ni ddylid rhwgo unrhyw ran o'r llyfr hwn; rhaid ei gyflwyno yn gyfan.
7. Os defnyddir mwy nag un llyfr, rhwymwch hwy gyda'i gilydd gan ddefnyddio'r tagiau sydd ar gael oddi wrth y gwyllwyr/gwylwyr.
8. Rhaid dychwelyd pob llyfr. Ni chaniateir mynd â llyfrau atebion, wedi eu defnyddio neu heb eu defnyddio, allan o'r lleoliad arholi o dan unrhyw amgylchriadu.

[illegible]

7	Nifer y Llyfrau Atebion a gyflwynwyd	
6	Rhif Sedd	
5	Lleoliad yr Arholiad	
4	Dyddiad ac Amser yr Archoliad	
3	Cod y Modwl	
2	Teitl y Papur Arholiad	
1	Rhif Myfyrwr	

(See the other side for English version)

CYFENN:

ENW(AU) CYNTAF:

Llenwch, plynwch a seliwch
(gweler nodyn 2 isod)

- 1 a) The function of Single Stuck at Fault models allow for the CUT (circuit under test) to be tested against a sequence and be compared to a good circuit using an XOR gate as a ~~Comp~~ Comparator ✓ 3

- b) The number of test vectors can be determined by $m+1$ (m = number of inputs) ✓ to eliminate redundancies.

NAND

Test	A	B	C	Q	Test	A	B	C	Q
1	0	0	0	1	1	1	1	1	0
2	0	0	1	0	2	1	1	0	1
3	0	1	0	0	3	1	0	1	1
4	0	0	0	0	4	0	1	1	1

All inputs are required to ~~be~~ have a logic 0 for an output of 1. All redundant test vectors have been removed. 2

NOR

Test	A	B	C	Q
1	1	1	1	1
2	1	1	0	0
3	1	0	1	0
4	0	1	1	0

All logic 1 are required to give an output of logic 1. Any logic 0 as an input will give a logic 0 output.

c) Step 1 Would be to Calculate the Conditions at the x node. A logic 1 is needed at node x in order for z to be 1.

Using the Conditions in Part B x can be made to logic 1. If any of the inputs A, B or C contain a logic 0 output at x will be 1.

Node y will need to also be at logic 1 to have node z at 1. If a fault was introduced at any input that forced node x or node y to go to logic 0 node z will also go to logic 0 ~~then~~ as x and y pass through an AND gate. z then will determine output

4

d) i)

Current State						Next State					
A	B	C	D	E	F	A ⁺	B ⁺	C ⁺	D ⁺	E ⁺	F ⁺
1	1	1	0	0	0	0	1	1	0	0	0
0	1	1	0	0	0	1	0	1	0	0	0
1	0	1	0	0	0	1	1	0	0	0	0
1	1	0	0	0	0	0	0	0	1	0	0
0	0	0	1	0	0	0	0	0	0	1	0
0	0	0	0	1	0	1	1	1	1	1	0
1	1	1	1	1	0	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	0	0	0

2 1/2

2

		01324576							
A+	ABC	000	001	011	010	100	101	111	110
DEF	000	0	0	1	0	0	1	0	0
001	0	0	0	0	0	0	0	0	0
011	0	0	0	0	0	0	0	0	0
010	1	0	0	0	0	0	0	0	0
100	0	0	0	0	0	0	0	0	0
101	0	0	0	0	0	0	0	0	0
111	0	0	0	0	0	0	1	0	0
110	0	0	0	0	0	0	1	0	0

$$A^+ = A.B.C.D.E + \overline{A}.B.C.\overline{D}.\overline{E}.\overline{F} + A.\overline{B}.C.\overline{D}.\overline{E}.\overline{F} + \overline{A}.\overline{B}.\overline{C}.\overline{D}.E.\overline{F}$$

B+	ABC	000	001	011	010	100	101	111	110
DEF	000	0	0	0	0	0	1	1	0
001	0	0	0	0	0	0	0	0	0
011	0	0	0	0	0	0	0	0	0
010	0	0	0	0	0	0	0	0	0
100	0	0	0	0	0	0	0	0	0
101	1	0	0	0	0	0	0	0	0
111	0	0	0	0	0	0	1	0	0
110	0	0	0	0	0	0	1	0	0

$$B^+ = A.B.C.D.E + A.C.\overline{D}.\overline{E}.\overline{F} + \overline{A}.\overline{B}.\overline{C}.\overline{D}.E.\overline{F}$$

1/2

1/2

4

3 1/2

C ⁺	ABC	000	001	011	010	100	101	111	110
DEF	000	0	0	1	0	0	0	1	0
001	0	0	0	0	0	0	0	0	0
011	0	0	0	0	0	0	0	0	0
010	1	0	0	0	0	0	0	0	0
100	0	0	0	0	0	0	0	0	0
101	0	0	0	0	0	0	0	0	0
111	0	0	0	0	0	0	0	1	0
110	0	0	0	0	0	0	0	1	0

$$C^+ = A.B.C.D.E + NA.B.C.ND.NE.NF + A.B.C.ND.NE.NF + NA.NB.NC.ND.E.NF$$

D ⁺	ABC	001	011	010	100	101	111	110
DEF	000	0	0	0	0	0	0	1
001	0	0	0	0	0	0	0	0
011	0	0	0	0	0	0	0	0
010	1	0	0	0	0	0	0	0
100	0	0	0	0	0	0	0	0
101	0	0	0	0	0	0	0	0
111	0	0	0	0	0	0	0	0
110	0	0	0	0	0	0	1	0

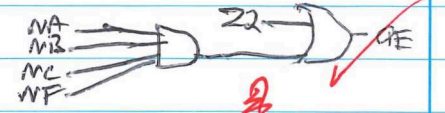
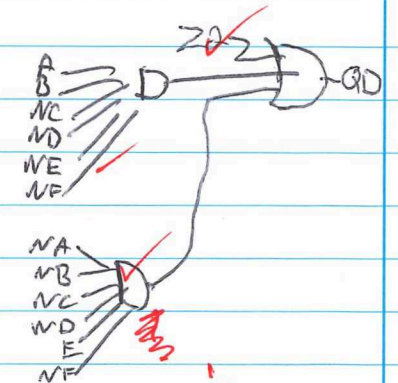
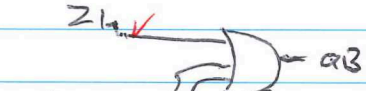
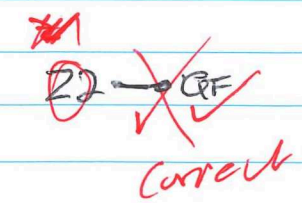
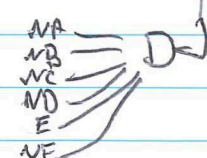
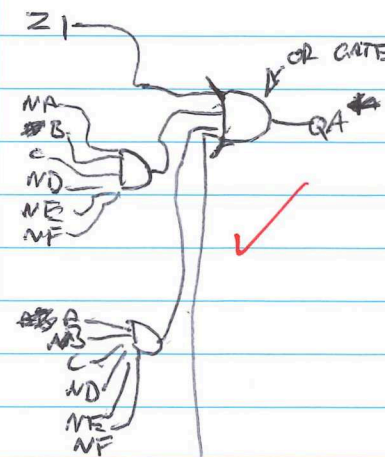
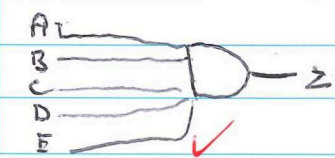
$$D^+ = A.B.NC.ND.NE.NF + NA.NB.NC.ND.E.NF + A.B.C.D.E.NF$$

E ⁺	ABC	000	001	011	010	100	101	111	110
DEF	000	0	0	0	0	0	0	0	0
001	0	0	0	0	0	0	0	0	0
011	0	0	0	0	0	0	0	0	0
010	1	0	0	0	0	0	0	0	0
100	1	0	0	0	0	0	0	0	0
101	0	0	0	0	0	0	0	0	0
111	0	0	0	0	0	0	0	0	0
110	0	0	0	0	0	0	0	1	0

$$E^+ = NA.NB.NC.NF + A.B.C.D.E.NF$$

F ⁺	ABC	000	001	011	010	100	101	111	110
DEF	000	0	0	0	0	0	0	0	0
001	0	0	0	0	0	0	0	0	0
011	0	0	0	0	0	0	0	0	0
010	0	0	0	0	0	0	0	0	0
100	0	0	0	0	0	0	0	0	0
101	0	0	0	0	0	0	0	0	0
111	0	0	0	0	0	0	0	0	0
110	0	0	0	0	0	0	0	1	0

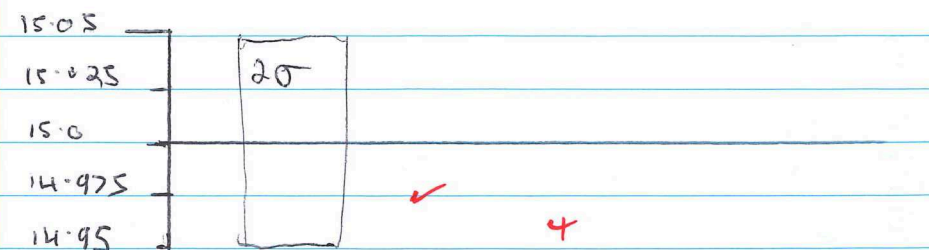
$$F^+ = A.B.C.D.E.NF$$



dii) The System would go through the sequence changing on each clock rise. The circuit would then compare against a goal via an XOR gate as a comparator. When a fault is detected the toll gate will flag up as a fault on the cut. ✓ 2

2a) mean = 15mm Range = 0.05

i) $Std = 0.05 \div 2 = 0.025$ ✓ 2



ii) $Upper - Lower / 6\sigma$
 $15.05 - 14.95 / 6 \times 0.025 = 0.6$

$CP \leq 1$ ∴ process is not capable ✓ 3

Using 3 Sigma
 $Std = 0.05 \div 3 = 0.016$

$Upper - Lower / 6\sigma$

$0.1 / 6 \times 0.016 = 1.04$ ✓

Process is capable using 3 Sigma as $CP > 1$
 Process is only just capable and recommendation would be to increase Sigma process eg. 4 to take CP further above 1 ✓ 3

iii) Sigma is a process quality goal which looks at a deviation either side of a mean value to ensure the quality mean is met. CP is the process variable that is measured and anything < 1 is said to be not capable. 6 Sigma is the best process. ✓ 2/3

2b)

$$0.05 \div 4 = 0.0125 \quad \checkmark \quad 1$$

$$\text{upper limits} = 15.0125, 15.025, 15.0375, 15.05 \quad \checkmark \quad 1$$

$$\text{lower limits} = 14.9875, 14.975, 14.9625, 14.95 \quad \checkmark \quad 1$$

$$\text{i)} \quad Cpk = \min \left(\frac{\text{upper} - \text{mean}}{3\sigma}, \frac{\text{mean} - \text{lower}}{3\sigma} \right)$$

$$Cpk = \min \left(\frac{15.05 - 15.02}{(3 \times 0.0125)}, \frac{15.02 - 14.95}{(3 \times 0.0125)} \right) \quad \checkmark \quad 2$$

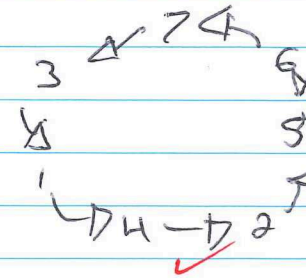
$$Cpk = 0.8, 1.86 \quad \checkmark \quad 1$$

ii) Process is now not capable as $Cpk < 1$
as one side of the mean (upper limit) is less than
1 as only 0.8 will fit in the upper limit
due to the shift. $\checkmark \quad 2$

v) The CP does not take into account drift in the
machine due to wear and tear where the Cpk
is the index that accounts for changes in the mean. $\checkmark \quad 2$

4) Random generators allow circuits to be in
a different test sequence $\checkmark$ to detect results in
the log2. $\checkmark \quad 1$

1i)



Current

Next

11 1

00 01

01 1

00 1

00 1

10 0

10 0

01 0

01 0

10 1

10 1

11 0

11 0

11 1 $\checkmark \quad 3$

At

AB

C 00 10 01 11

0 0 0 0

1 1 0 0

1 1 0 0

1 1 0 0

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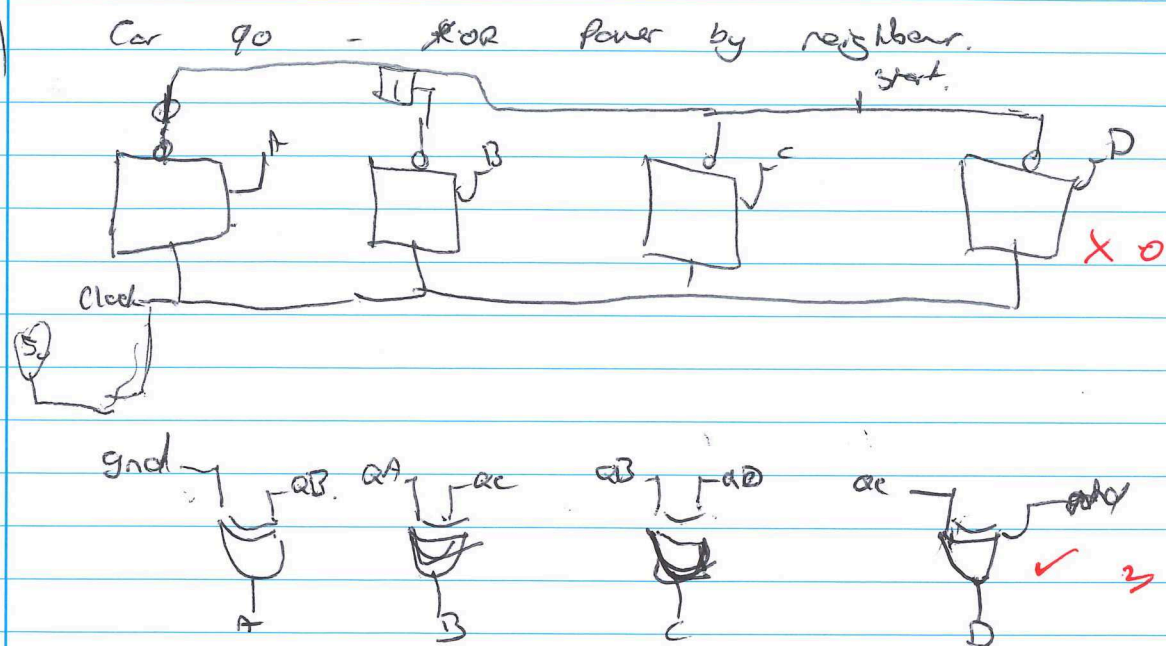
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b) i)

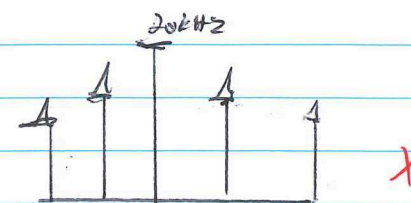


ii)

Clk	Count	Current QA = 0 QB = 0 QC = 0 QD = 1 NA = 0	QA = 0 QB = 0 QC = 0 QD = 1	QA = 0 QB = 0 QC = 0 QD = 1	QA = 0 QB = 0 QC = 0 QD = 1
1	1	QA = 0 QB = 0 QC = 0 QD = 1	QA = 0 QB = 0 QC = 0 QD = 1	QA = 0 QB = 0 QC = 0 QD = 1	QA = 0 QB = 0 QC = 0 QD = 1
2	2	QA = 0 QB = 0 QC = 0 QD = 1	QA = 0 QB = 0 QC = 0 QD = 1	QA = 0 QB = 0 QC = 0 QD = 1	QA = 0 QB = 0 QC = 0 QD = 1
3	3	QA = 0 QB = 0 QC = 0 QD = 1	QA = 0 QB = 0 QC = 0 QD = 1	QA = 0 QB = 0 QC = 0 QD = 1	QA = 0 QB = 0 QC = 0 QD = 1
4	4	QA = 1 QB = 0 QC = 0 QD = 0	QA = 1 QB = 0 QC = 0 QD = 0	QA = 1 QB = 0 QC = 0 QD = 0	QA = 1 QB = 0 QC = 0 QD = 0
5	5	QA = 0 QB = 1 QC = 0 QD = 0	QA = 0 QB = 1 QC = 0 QD = 0	QA = 0 QB = 1 QC = 0 QD = 0	QA = 0 QB = 1 QC = 0 QD = 0
6	6	QA = 1 QB = 0 QC = 1 QD = 0	QA = 1 QB = 0 QC = 1 QD = 0	QA = 1 QB = 0 QC = 1 QD = 0	QA = 1 QB = 0 QC = 1 QD = 0

c) CAR System has to start with a 1 ✓ or the count will not start. The flip-flops are inverted on inputs. CAR System allows for a random count ✓

3. d)



3. c)

$$\frac{\sin(\omega t)}{\pi} = \frac{\sin(\omega t)}{\pi}$$

$$\frac{\sin(2000 \times 5)}{5\pi} = \frac{\sin(2000 \times 5)}{5\pi} \quad \text{X} \quad 0$$

3

3

2

8