

12 Pages

1. Please give the information requested in the boxes below.
2. Enter your name in the space provided to the right, fold over and seal down (using the label provided) to hide your name.
3. The answers must be legibly written. The Examiners can either ignore illegible script or have it typed and the expense of typing charged to the candidate.
4. Write your answers in ink.
5. Begin each answer on a fresh page. Do all rough work in the answer book and cross it through.
6. No part of this book is to be torn out; it must be handed in complete.
7. If more books than one are used, fasten them together using the tags available from the invigilator(s).
8. **Every book must be handed in. In no circumstances may answer books, used or unused, be taken out of the examination venue.**

1	Student Number	1451789
2	Title of Examination Paper	ELEC PRON & TEST
3	Module Code	SCPE 6002
4	Date and Time of Examination	9:30 19/5/23
5	Examination Venue	HALL
6	Seat Number	32
7	Number of Answer Books handed in	1

(Gweler yr ochr arall am y fersiwn Cymraeg)

List the numbers of the questions you have attempted	Office Use
2	25
3	4 1/2
1	21
4	1
Total	51 1/2

MAR
AGREED.
52%

SURNAME: Williams

FORENAME(S): Joshua
Jordan

(See the other side for English version)

7	Nifer y Llyfrau Atebion a gyflwynwyd	
6	Rhif Sedd	
5	Lleoliad yr Arholiad	
4	Dyddiad ac Amser yr Archoliad	
3	Cod y Modwl	
2	Teitl y Papur Arholiad	
1	Rhif Myfyrwr	

[illegible]

Cyfarwyddiadau i Ymgeiswyr

Llyfr Atebion Arholiadau



Prysgol Cymru
Y Drindod Dewi Sant
University of Wales
Trinity Saint David

Llenwch, plygwch a seliwch
(gweler nodyn 2 isod)

CYFENN:

ENW(AU) CYNTAF:

1. Rhwch yr holl wybodaeth y gofynnir amdani yn y blychau isod.
2. Rhwch eich enw yn y lle a ddarparwyd ar y dde, plynwch ef a'i selio i lawr (gan ddefnyddio'r label a ddarparwyd) i guddio'ch enw.

guddio'ch enw.

3. Rhaid i'r atebion fod mewn llawysgrifen dda gael ei theipio a chael yr ymgeisydd i dalu.

4. Ysgriennwch eich atebion mewn inc.

5. Dechreuwch bob ateb ar dudalen newydd. Gwnewch unrhyw fras nodiadau yn y llyfr atebion a thynnwch llinell drwyddyn.

6. Ni ddylid rhwgo unrhyw ran o'r llyfr hwn; rhaid ei gyflwyno yn gyfan.

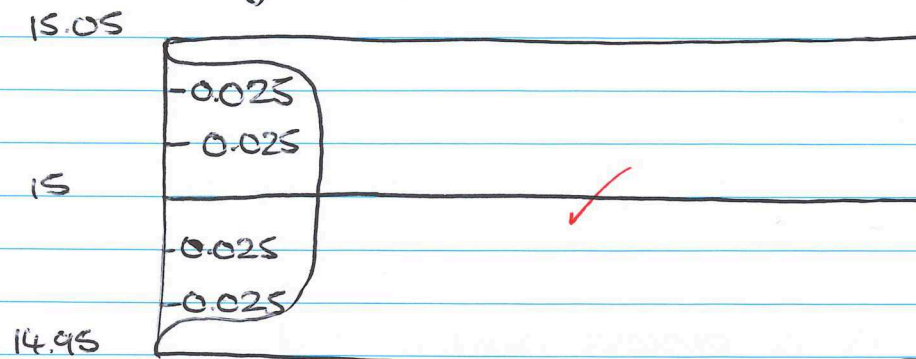
7. Os defnyddir mwy nag un llyfr, rhwymwch hwy gyda'i gilydd gan ddefnyddio'r tagiau sydd ar gael oddi wrth y gwyllwyr/gwyllwyr.

8. Rhaid dychwelyd pob llyfr. Ni chaniad arholi o dan unrhyw amgylchiadau.

8. Rhaid dychwelyd pob llyfr. Ni chaniateir mynd â llyfrau atebion, wedi eu defnyddio neu heb eu defnyddio, allan o'r lleoliad

Question 2

- i) 15mm = mean STD = $0.05/2 = 0.025$ ✓²
 ± 0.05 = range
 2 = Sigma ✓



- ii) 6 sigma

$$STD = 0.025 \quad \checkmark$$

upper spec - lower spec / 6σ

$$15.05 - 14.95 / 6(0.025)$$

$$Cp = 0.6 \quad \checkmark$$

3

As the Cp value is less than one (<1)
 this is not capable. ✓

3 sigma

$$STD = 0.05/3 = 0.016$$

upper spec - lower spec / 6σ

$$15.05 - 14.95 / 6(0.016)$$

$$Cp = 1.04 \quad \checkmark$$

3

6

As ~~this~~ (in spec) the CP value is equal this is somewhat equal.

The 2 Sigma level is not capable as the CP value is less than one (<1).

To improve the process the Sigma value will have to be increased so that the CP is above the minimum.

- iii) Six Sigma is a process quality goal. Sigma is a Statistical measure of variability in a System. The standard deviation should be no more than 1 twelfth of the total ^{allowable} spread.

In Six Sigma, the upper limits above the mean should be >1 and lower limit below the mean should be >1 this is known as 'capable' if the limits do not fit either side of the mean (<1) this is 'not capable'.

- b) i) $4\sigma \text{ (STD)} = \text{range} / 4 = 0.025 / 4 = 0.0125$.

upper limits = 15.0125, 15.025, 15.0375, 15.05.

lower limits = 14.9875, 14.975, 14.9625, 14.95.

ii) $CPK = \min(\frac{\text{mean} - L_{\text{spec}}}{3\sigma}, \frac{U_{\text{spec}} - \text{mean}}{3\sigma})$

$CPK = \min(\frac{15.02 - 14.95}{3(0.0125)}, \frac{15.05 - 15.02}{3(0.0125)})$

$CPK = \min(1.86, 0.8)$

$CPK = 0.8$.

- iii) This indicates that the 4 Sigma level is not capable. As the upper limit above the mean is 0.8 and the lower limit below the mean is 1.86. To fit both values either side of the mean has to be greater than one (>1). This is according to the 3 sigma rule.

- vi) CP does not change. This is down to the standard deviation stays the same. None of the attributes in the CP calculation change this due to the change in the mean value.

CPK value caters for the shift in mean and this compares the result with the 3 sigma rule (ie. does the CP value fit either side of the mean). Where as the CP does not cater for the shift in mean.

Question 3.

a)

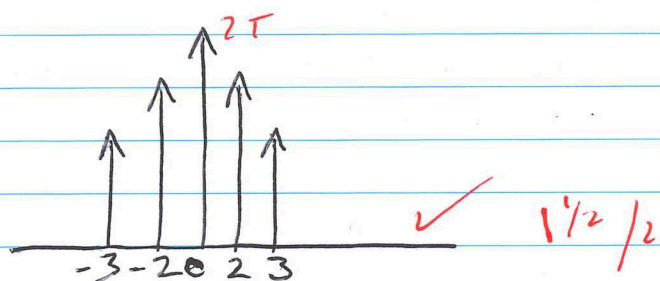
$$i) x(t) = \frac{2}{2} e^{-j2\pi} \times 3000t + \frac{4}{2} e^{-j2\pi} \times 2000t.$$

$$+ \frac{2}{2} e^{j\pi} \times 3000t + \frac{4}{2} e^{j\pi} \times 2000t.$$



3

ii)

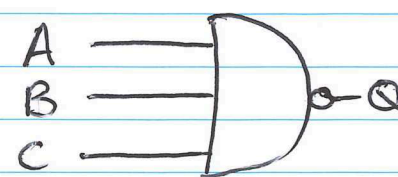


1 1/2

Question 1

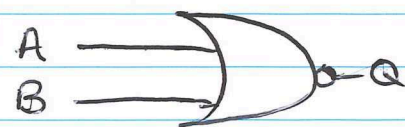
a) Auto function and the reduced test sequence can be used. The method for designing complex digital systems can use the form of simple logical gates. Reduced test sequence is derived from eliminating redundant test vectors. The other method is using the 'wild cards' to eliminate the redundant test vectors.

b)



	A	B	C	Q
1	1	1	1	0
2	0	1	1	1
3	1	0	1	1
4	1	1	0	1

The NAND function ^{and} uses the following rule of the $(m)+1 = \text{No of test vectors}$.



	A	B	Q
1	0	0	1
2	1	0	0
3	0	1	0

The NOR Function uses the logic 1 output test. All inputs are set to logic 1 ~~then~~ ^{the propagated} for all positions in turn.

c) STEP 1 - Implement the fault model to the gates for the circuit in test.

STEP 2 - determine ^{the propagated} path to a node and set the test vector.

If the gate at the fault is carrying to propagated through a NAND or AND function. All inputs are set to logic 1 except those carrying faults.

NOR output logic is set to logic 1.

NAND output logic is set to logic 0. ✓ 4/6

i)

Present State						NEXT STATE					
A	B	C	D	E	F	A+	B+	C+	D+	E+	F+
1	1	1	0	0	0	0	1	1	0	0	0
0	1	1	0	0	0	1	0	1	0	0	0
1	0	1	0	0	0	1	1	0	0	0	0
1	1	0	0	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	0	1	0
0	0	0	0	1	0	1	1	1	1	1	0
1	1	1	1	1	0	1	1	1	1	1	1
1	1	1	1	1	1	1	1	0	0	0	0

A+	00	01	11	10	100	101	111	110
00	0	0	0	1	0	0	0	0
01	0	0	0	0	0	0	0	0
11	0	0	0	0	0	0	0	0
10	1	0	0	0	0	0	0	0
100	0	0	0	0	0	0	0	0
101	0	0	0	0	0	0	0	0
111	0	0	0	0	0	0	1	0
110	0	0	0	0	0	0	1	0

$$A+ = DA = A.B.C.D.E. + A.NB.C.ND.NE.NF + NA.B.C.ND.NE.NF + NA.NB.NC.ND.E.NF.$$

B+	00	01	11	10	100	101	111	110
00	0	0	0	0	0	1	1	0
01	0	0	0	0	0	0	0	0
11	0	0	0	0	0	0	0	0
10	1	0	0	0	0	0	0	0
100	0	0	0	0	0	0	0	0
101	0	0	0	0	0	0	0	0
111	0	0	0	0	0	0	1	0
110	0	0	0	0	0	0	1	0

$$B+ = DB = A.C.ND.NE.NF + A.B.C.D.E + NA.NB.NC.ND.E.NF.$$

C+	00	01	11	10	100	101	111	110
00	0	0	0	1	0	0	1	0
01	0	0	0	0	0	0	0	0
11	0	0	0	0	0	0	0	0
10	1	0	0	0	0	0	0	0
100	0	0	0	0	0	0	0	0
101	0	0	0	0	0	0	0	0
111	0	0	0	0	0	0	1	0
110	0	0	0	0	0	0	1	0

$$C+ = B.C.ND.NE.NF + A.B.C.D.E + NA.NB.NC.ND.E.NF.$$

D+	00	01	11	10	100	101	111	110
00	0	0	0	0	0	0	0	1
01	0	0	0	0	0	0	0	0
11	0	0	0	0	0	0	0	0
10	1	0	0	0	0	0	0	0
100	0	0	0	0	0	0	0	0
101	0	0	0	0	0	0	0	0
111	0	0	0	0	0	0	0	0
110	0	0	0	0	0	0	0	0

$$D+ = ND = NA.NB.NC.ND.E.F + NA.NB.NC.ND.NE.NF + A.B.C.D.E.NF.$$

E+	00	01	11	10	100	101	111	110
00	0	0	0	0	0	0	0	0
01	0	0	0	0	0	0	0	0
11	0	0	0	0	0	0	0	0
10	0	0	0	0	0	0	0	0
100	0	0	0	0	0	0	0	0
101	0	0	0	0	0	0	0	0
111	0	0	0	0	0	0	1	0
110	0	0	0	0	0	0	0	0

1/2

1/2

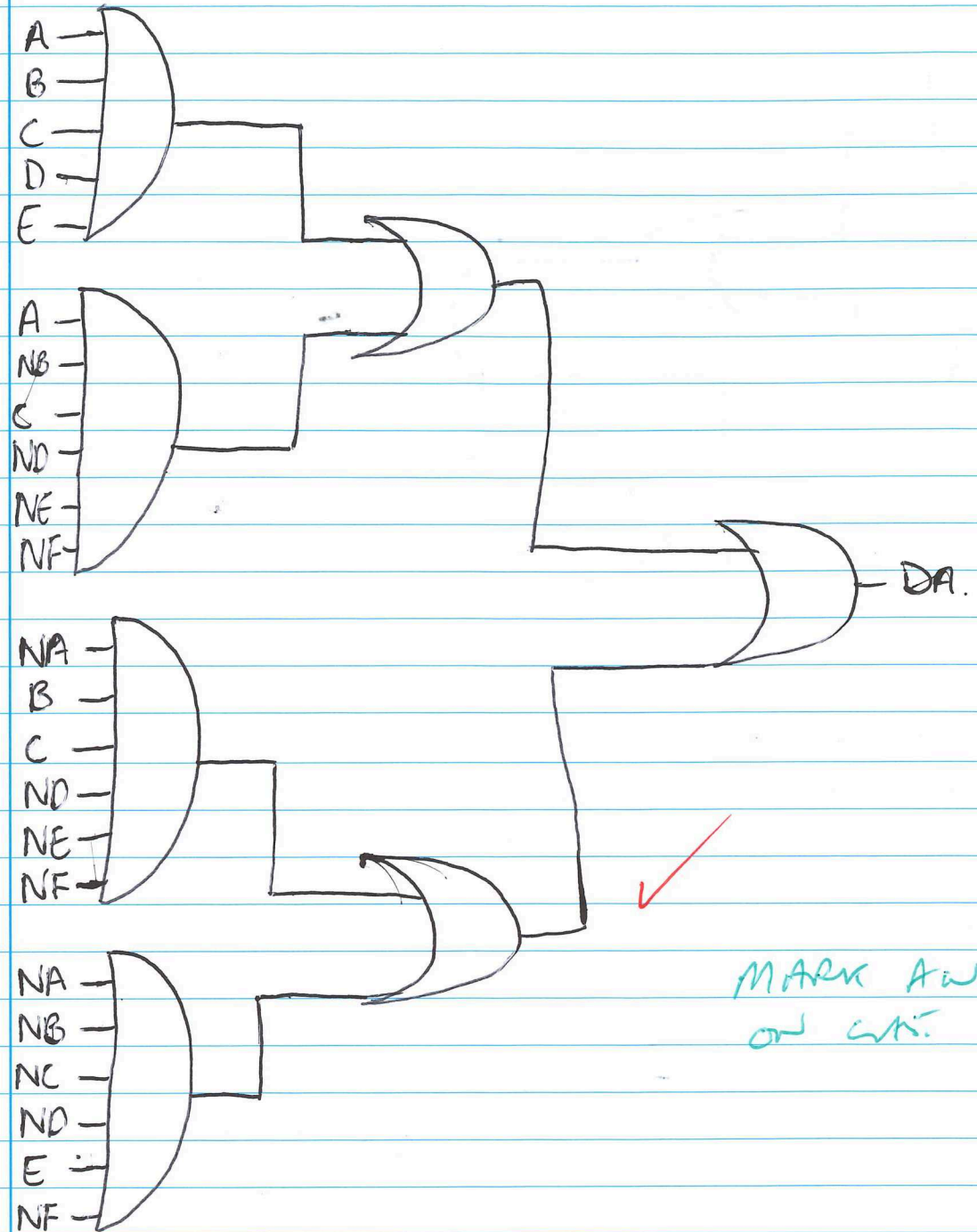
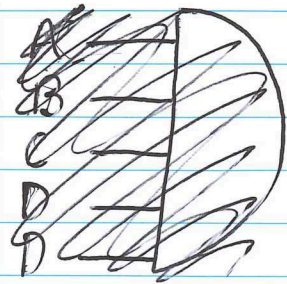
$$E+ = DE = \overline{N_A} \cdot \overline{N_B} \cdot \overline{N_C} \cdot \overline{N_D} \cdot E \cdot \overline{N_F} + \overline{N_A} \cdot \overline{N_B} \cdot \overline{N_C} \cdot D \cdot \overline{N_E} \cdot \overline{N_F} + A \cdot B \cdot C \cdot D \cdot E \cdot \overline{N_F}$$

F+	00	01	11	10	100	101	111	110
00	0	0	0	0	0	0	0	0
01	0	0	0	0	0	0	0	0
11	0	0	0	0	0	0	0	0
10	0	0	0	0	0	0	0	0
100	0	0	0	0	0	0	0	0
101	0	0	0	0	0	0	0	0
111	0	0	0	0	0	0	0	0
110	0	0	0	0	0	0	1	0

1

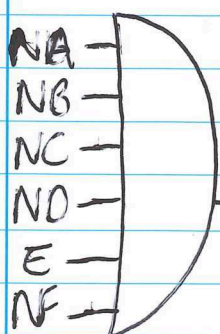
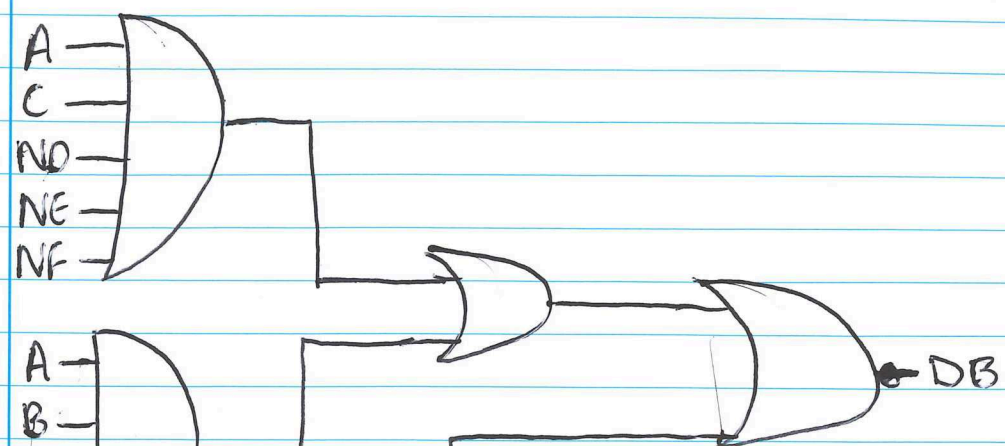
1

$$F+ = DF = A \cdot B \cdot C \cdot D \cdot E \cdot \overline{N_F}$$

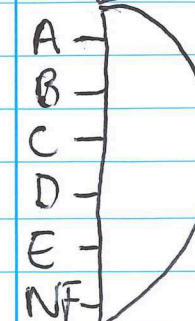
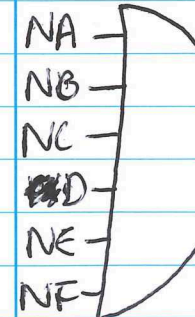
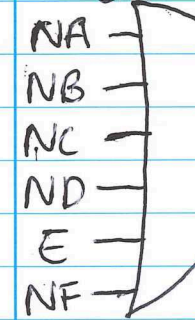
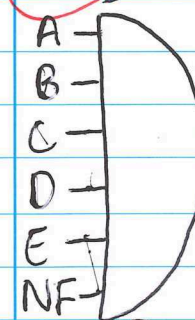
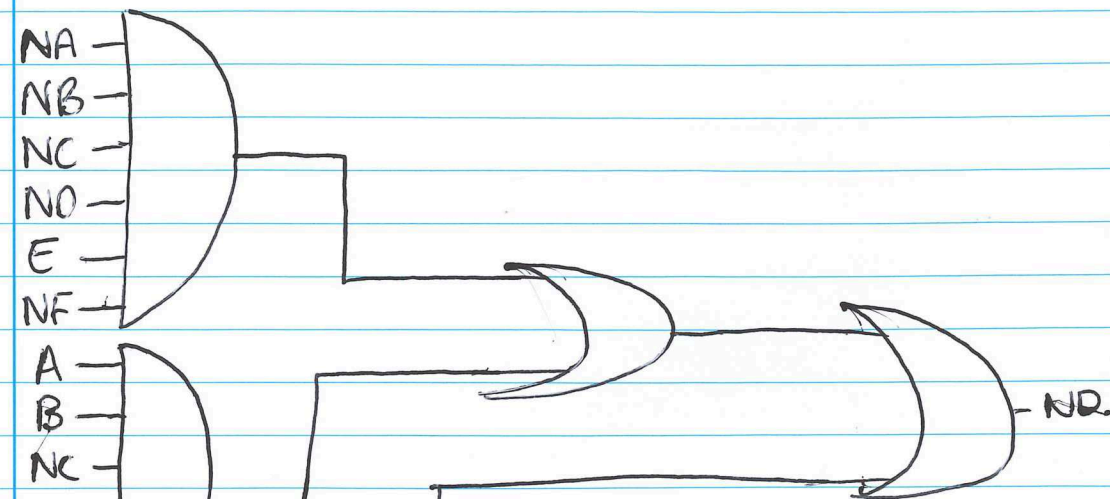
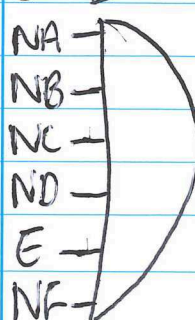
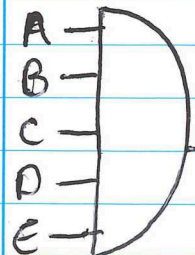
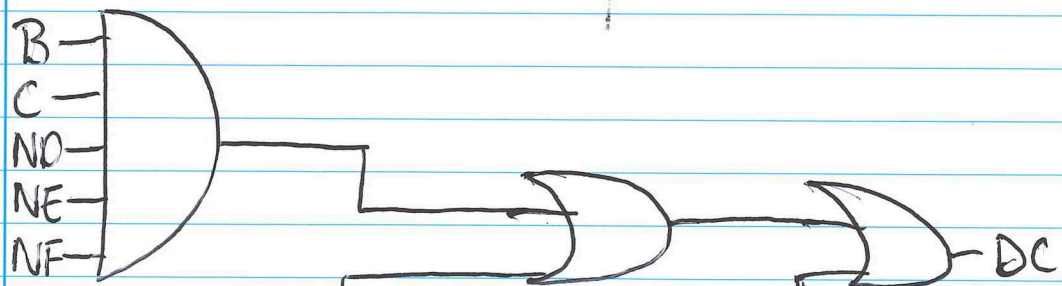


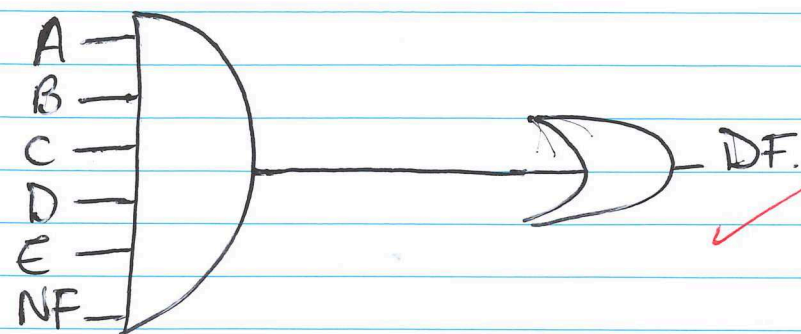
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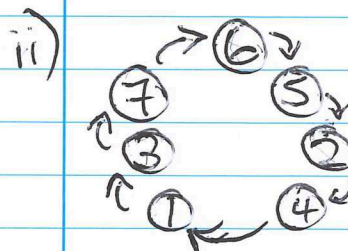
- ii) The 6 bit register will run through the test vectors at the sample clock rate. The inputs ~~rely~~ are determined by the logical conditioning of the register input. ✓

Ex-or is logical state is at 1 when differences are detected at input. ✓

2

2

Question 4



1

Q1 = 3 1/2

Q2 = 1

Rhif y Cwestiwn

3 1/2