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FORENAME(S): BRYAN

12 Pages

1. Please give the information requested in the boxes below.
2. Enter your name in the space provided to the right, fold over and seal down (using the label provided) to hide your name.
3. The answers must be legibly written. The Examiners can either ignore illegible script or have it typed and the expense of typing charged to the candidate.
4. Write your answers in ink.
5. Begin each answer on a fresh page. Do all rough work in the answer book and cross it through.
6. No part of this book is to be torn out; it must be handed in complete.
7. If more books than one are used, fasten them together using the tags available from the invigilator(s).
8. **Every book must be handed in. In no circumstances may answer books, used or unused, be taken out of the examination venue.**

1	Student Number	2307828
2	Title of Examination Paper	Micros, Peripherals and Interfaces
3	Module Code	ACDA 4004
4	Date and Time of Examination	08/01/2025 09:00
5	Examination Venue	1Q310
6	Seat Number	024
7	Number of Answer Books handed in	1

List the numbers of the questions you have attempted	Office Use
1	10
2	10
3	3
4	7 + 3
5	10
6	6
	49
Total	98%

(Gweler yr ochr arall am y fersiwn Cymraeg)

1.

a. RETURN

- Returns from a subroutine.
- The stack is POPed and the ~~the~~ address that was in the top of the stack is loaded into the program counter.

2

2

b. SLEEP

- Puts the microcontroller into sleep mode.
- This sleeps the microcontroller and stops operations until a waking interrupt signal is seen.

2

2

c. ADDLW

- Add~~s~~ literal to w register.
- This adds the specified literal value to the value in the w register and puts the result into the w register.

2

2

d. BCF F, ~~F~~

- Bit Clear F
- This sets the bit, b, of the byte located at file location F to zero.

2

2

e. DECF

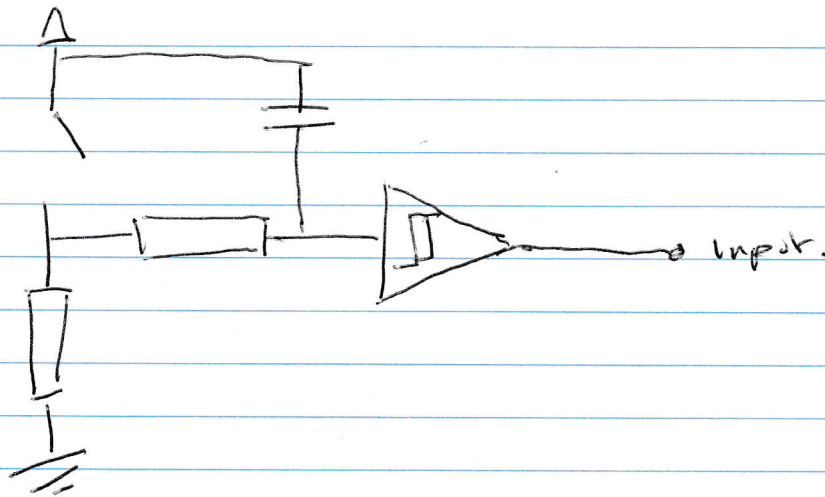
- Decrement F
- This subtracts 1 from the value located at file F.

2

2

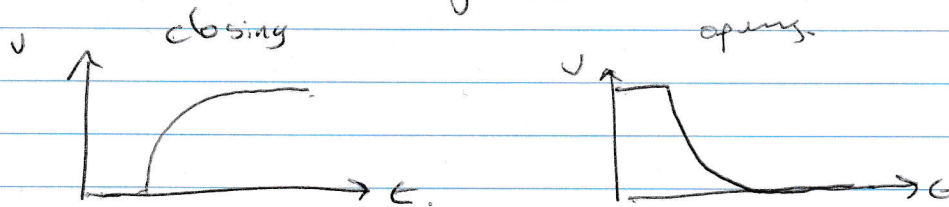
10.

2. One hardware method for dealing with switch bounce is by adding a capacitor and Schmitt trigger:



The addition of the capacitor adds a RC time constant (delay) to the opening and closing signals from the switch as when the switch is closed the capacitor charges over the period of the switch bounce and when opened discharges over a period.

signals seen:



Feeding this into a Schmitt trigger ensures that only discrete stable signals are seen at the input. This is achieved by the Schmitt trigger using 2 voltage thresholds which latch to the previous state when in between. This ensures only defined states are seen at the input.

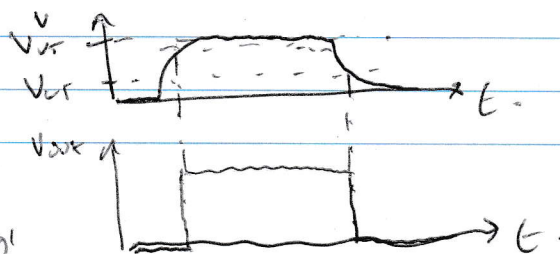
Schmitt trigger operation:

$$V_{in} > V_{UT}$$

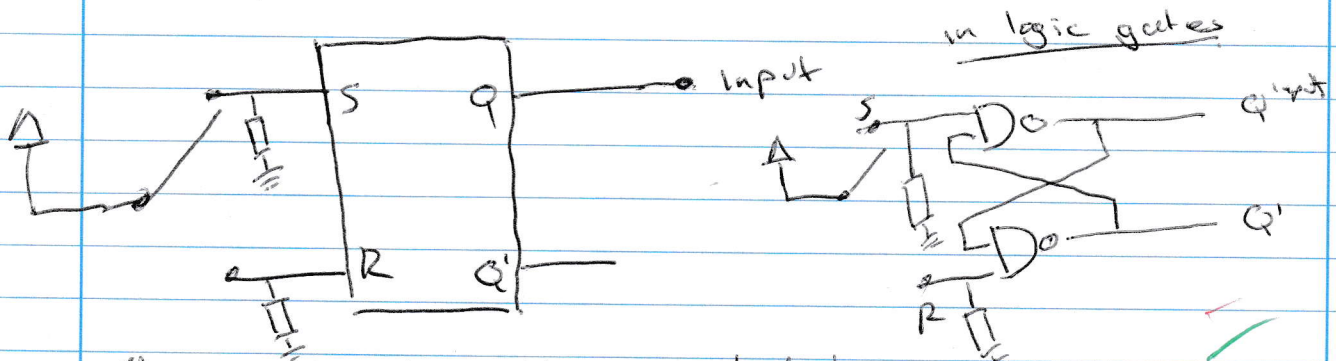
Logic '1'
previous output.

$$V_{in} < V_{LT}$$

Logic '0'



Another method which can be used for a double pole switch is the inclusion of an SR latch.



This works by the SR latch only being able to output 2 states high or low and once set latches to output high and when reset can only output low. This means when the switch is in the set position, only logic '1' will be outputted and when in the reset position only logic '0' can be outputted.

Table showing

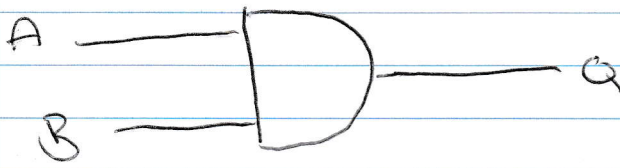
the two states of the switch and its outputs.

S	R	Q
1	0	1
0	1	0

3.

AND gate

Truth table.



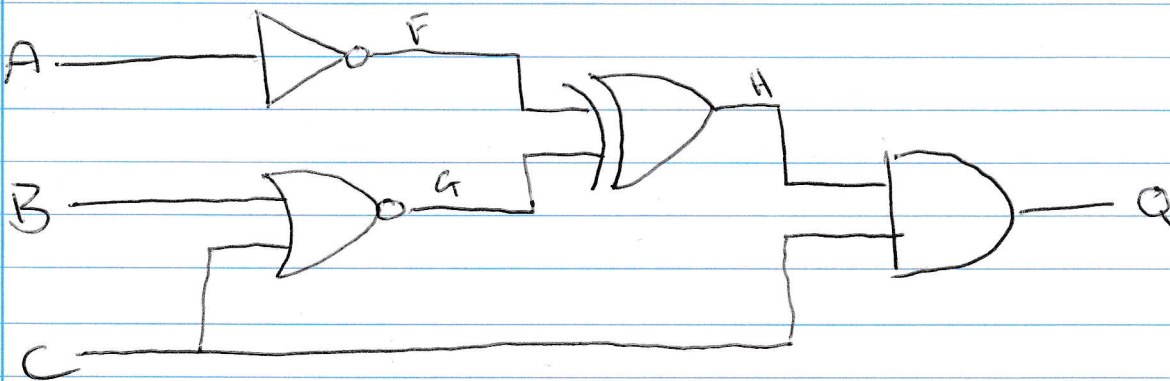
A	B	Q
0	0	0
0	1	0
1	0	0
1	1	1

3

3

4.

a.



A	B	C	F	G	H	Q
0	0	0	1	1	0	0
0	0	1	1	0	1	1
0	1	0	1	0	1	0
0	1	1	1	0	1	1
1	0	0	0	1	1	0
1	0	1	0	0	0	0
1	1	0	0	0	0	0
1	1	1	0	0	0	0

$$F = \bar{A}$$

$$G = B + C$$

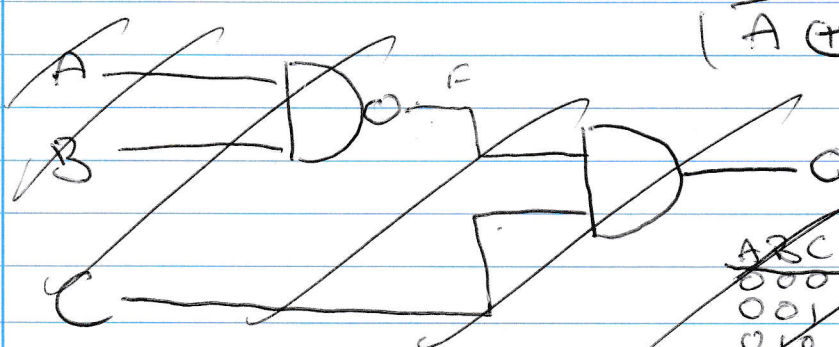
$$H = F \oplus G$$

$$Q = H \cdot C$$

7

7

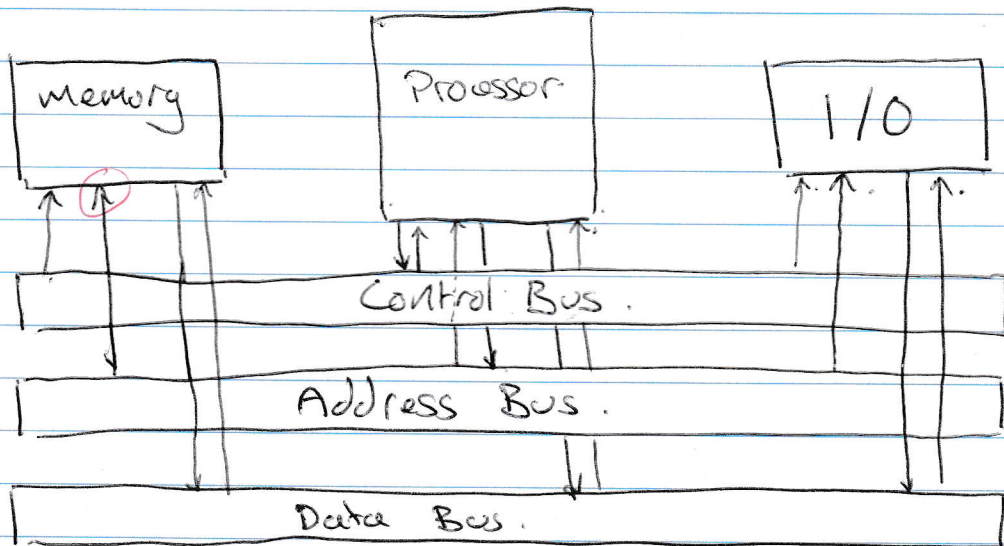
b.



$$(\bar{A} \oplus (B + C)) \cdot C = Q$$

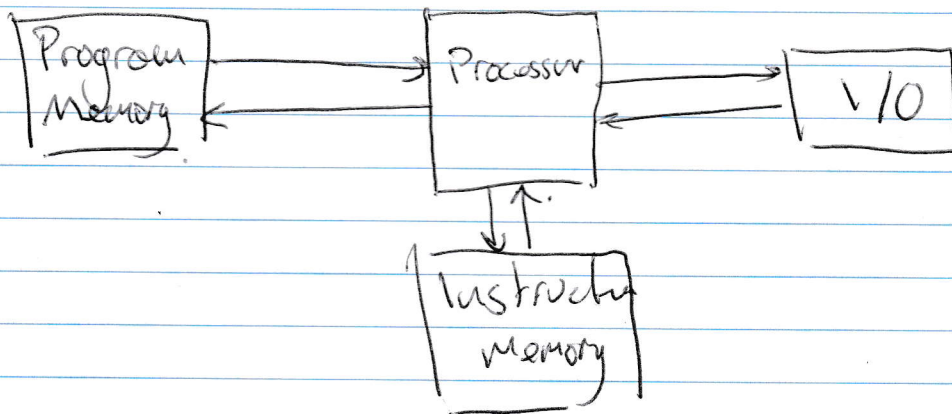
A	B	C	F	Q
0	0	0	1	0
0	0	1	1	1
0	1	0	1	0
0	1	1	1	1
1	0	0	0	0
1	0	1	0	0
1	1	0	0	0
1	1	1	0	0

5. Von Neumann:



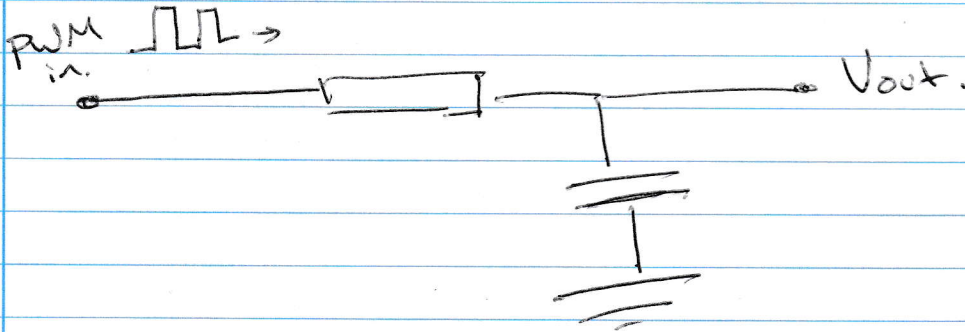
- Von Neumann architecture contains common bus with shared program and instruction memory.
- Advantage over Harvard is its simplicity with less tracks required to connect components together and is cheaper to construct.

Harvard:

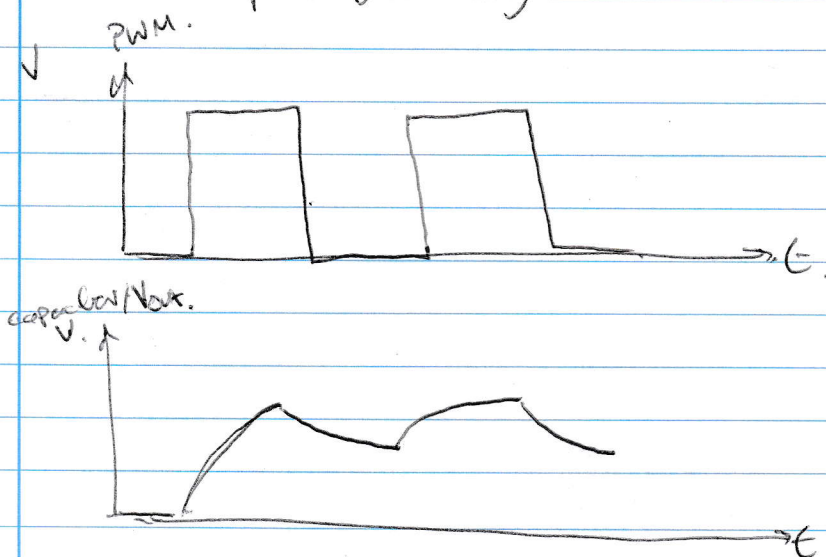


- Harvard architecture uses split instruction and program memory with separate buses.
- Advantage over von Neumann is speed and power efficiency with ability to get instructions and program data simultaneously.

6. A DAC can be constructed by using PWM and passing it through an RC filter. This will cause the capacitor to be charged and discharged at a rate which produces a constant voltage relative to the duty cycle of the PWM signal.

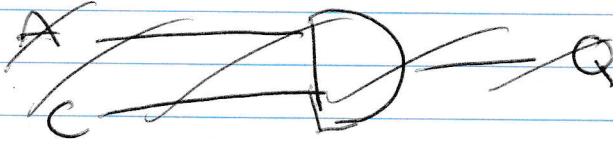


When the PWM signal is high the capacitor briefly charges and when low briefly discharges when done with the correct frequency the charge and discharge produces a relatively stable output voltage during the duty cycle of the signal will charge the voltage the capacitor charges to charging the output voltage. with the 100% duty cycle being equal to the maximum voltage of the PWM high and other periods being relative to that.

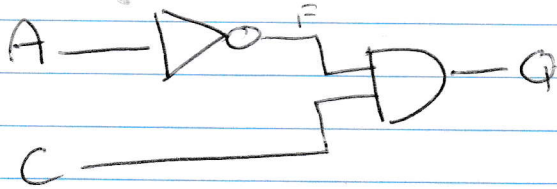


6

6.

4.
b.

A	C	Q
0	0	0
0	1	1
1	0	1
1	1	1



A	C	Q
0	0	0
0	1	0
1	0	0
1	1	1

A	C	$\bar{A}$	Q
0	0	1	0
0	1	1	1
1	0	0	0
1	1	0	0

3

3