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Complete, fold and seal
(see note 2 below)

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Examination Answer Books

12 Pages

Instructions to Candidates

1. Please give the information requested in the boxes below.
2. Enter your name in the space provided to the right, fold over and seal down (using the label provided) to hide your name.
3. The answers must be legibly written. The Examiners can either ignore illegible script or have it typed and the expense of typing charged to the candidate.
4. Write your answers in ink.
5. Begin each answer on a fresh page. Do all rough work in the answer book and cross it through.
6. No part of this book is to be torn out; it must be handed in complete.
7. If more books than one are used, fasten them together using the tags available from the invigilator(s).
8. Every book must be handed in. In no circumstances may answer books, used or unused, be taken out of the examination venue.

1	Student Number	2308433
2	Title of Examination Paper	Micros Peripherals and Interfacing
3	Module Code	ACDA4004
4	Date and Time of Examination	08/01/2025 9:00
5	Examination Venue	IQ109
6	Seat Number	
7	Number of Answer Books handed in	

List the numbers of the questions you have attempted	Office Use
1	8
2	2
3	3
4	10
5	3
6	0
	26
	x 2
Total	52%

8
2
3
10
3
0

26

Duty Run

1. A. Return, Return from function to the main code
- B. Sleep, Go into standby mode
- C. Add literal with W, Add the literal value with the W register and store the results in the W register
- D. Bit clear F, Clear the f register and store it in b.
- E. Decrement F, Decrement the F register

 $1\frac{1}{2}$ $1\frac{1}{2}$

2 2

2 2

$$\begin{array}{r} 1\frac{1}{2} \quad 1\frac{1}{2} \\ \hline 8 \end{array}$$

2. One way to reduce switch bounce using hardware is the use of a capacitor placed after the switch to provide a stable voltage. A circuit diagram for this would look something like the circuit in Fig 1.

2

Without reducing switch bounce the input provided to a pic for example would look like the view from an oscilloscope in Fig 2.

2

Second way to reduce switch bounce in hardware is add smoothing resistors.

x

5.

Advantage of Harvard Architecture: Separate memory and data bus making it quicker.

Advantages of Von Neumann Architecture: Less complex making it cheaper.

1

1

4.b.

By visually inspecting the table I can see that when only A is 0 and C is 1 when get an output in all other conditions no output is given. This means that the far simple logic diagram would be: Not A and C. Diagram can be seen in Fig Q4B.

$$\begin{array}{r} 2 \\ +1 \\ \hline 3 \end{array}$$

6.

You can implement a simple DAC (Digital to Analog Converter) using a microcontroller that produces a PWM (pulse width modulation) signal. The PWM is used to provide a reference clock into the DAC which in turn goes through the components to a comparator which outputs the analogue signal.

x

Q2:

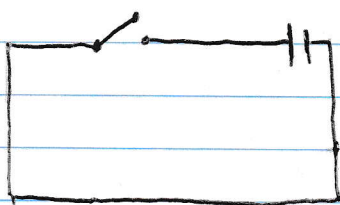


Fig 1

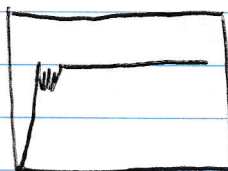
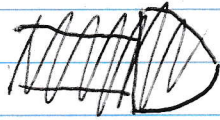


Fig 2

Q3:



AND Gate

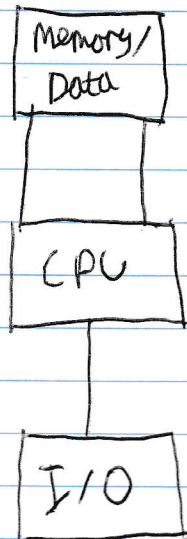
A	B	C
0	0	0
0	1	0
1	0	0
1	1	1

Truth table

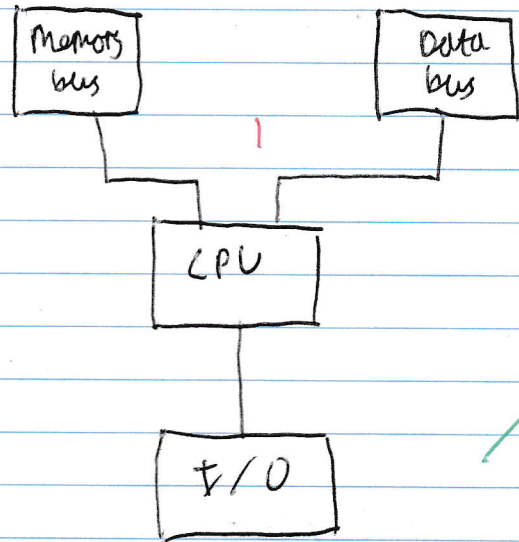
3

3

Q5:



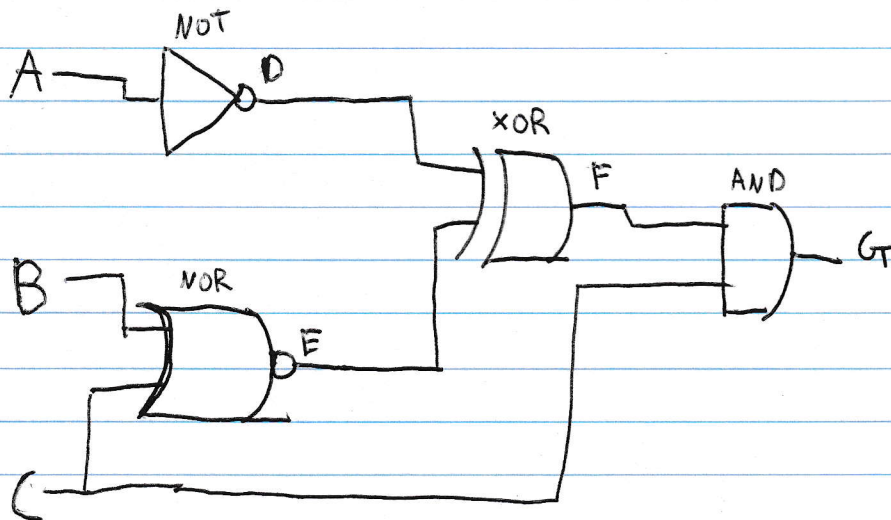
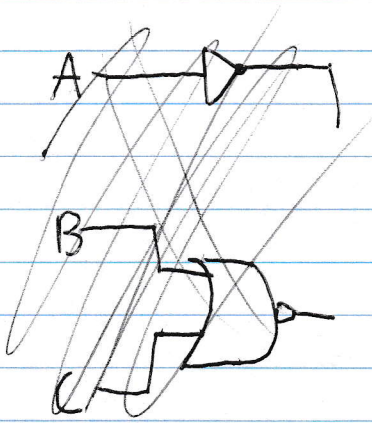
Von Neumann



Harvard

Q4:

a:



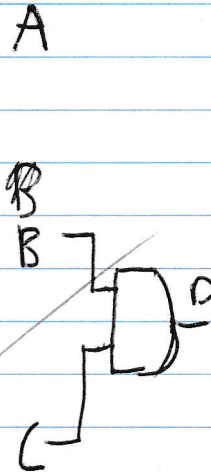
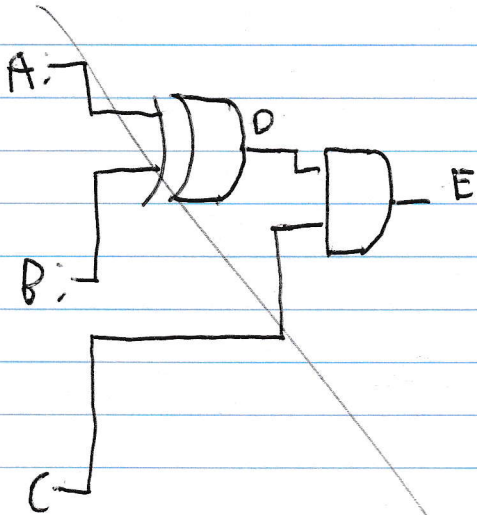
A	B	C	D	E	F	G
0	0	0	1	1	0	0
0	0	1	1	0	1	1
0	1	0	1	0	1	0
0	1	1	1	0	1	1
1	0	0	0	1	1	0
1	0	1	0	0	0	0
1	1	0	0	0	0	0
1	1	1	0	0	0	0

✓

7

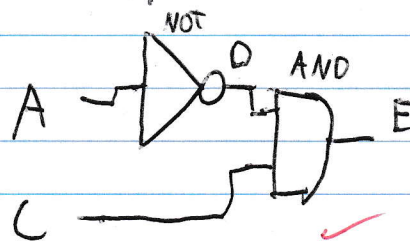
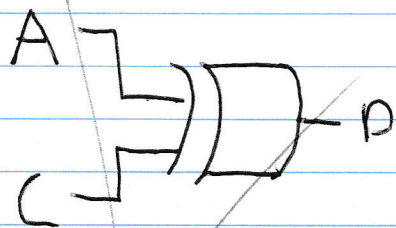
7

Q4:
b:



A	B	C	D	E
0	0	0	0	0
0	0	1	0	0
0	1	0	1	0
0	1	1	1	1
1	0	0	1	0
1	0	1	1	1
1	1	0	0	0
1	1	1	0	0

A	B	C	D
0	0	0	
0	0	1	
0	1	0	
0	1	1	1
1	0	0	
1	0	1	
1	1	0	
1	1	1	1



A	C	D
0	0	0
0	1	1
1	0	1
1	1	0

A	C	D	E
0	0	1	0
0	1	1	1
1	0	0	0
1	1	0	0

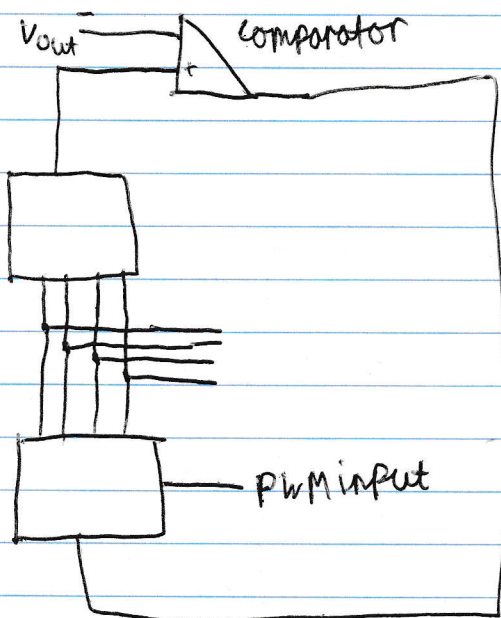
Fig Q4B

3

3

10.

Q6.



x

x.