

LEVEL 4 ASSESSMENT SPECIFICATION

Student name:	Maia Hough	Student ID number:	
Programme:	HNC Electrical/Electronic Engineering		
Module:	Electronics		
Module code:	PCEE4006	Contribution to Overall Module Assessment (%):	50%
Lecturer:	Jason Pointer	Internal Verifier:	Nigel Richards
Assignment Title:	Diodes and Amplifiers	Word count (or equivalent):	2000
Submission deadline:	19/01/23	Return date of provisional marks & written feedback:	02/02/23
Submission method:	All written assessments, where practical and possible, must be submitted via Turnitin unless otherwise instructed by the Lecturer. (Please DO NOT put this assessment specification into Turnitin or it will match many similarities with other students' submissions.) Alternative submission method (if applicable): Late submission of the assessment will result in a late penalty mark. Penalties for late submission: Up to one week late, maximum mark of 40%. Over one week late, 0%. Only the Extenuating Circumstances Panel may approve a change to submission dates.		
Academic honesty / referencing:	Academic honesty is required. In the main body of your submission you must give credit to authors on whose research and ideas your work is based. Append to your submission a reference list that indicates the books, articles, etc. that you have used, cited or quoted in order to complete this assessment.		

Module Learning Outcomes (from module syllabus)

1. Demonstrate an understanding of semi-conductor components and characteristics and their application in **analogue** and digital electronic circuits.
2. To design, simulate, build, test and evaluate **analogue** and digital electronic circuits using information gained from datasheets.

STUDENT FEEDBACK FORM

This section details the *extent* to which the assessment criteria are demonstrated by you, which in turn determines your mark. The marks available for each category of skill are shown. Lecturers will use the space provided to comment on the achievement of the task(s), including those areas in which you have performed well and areas that would benefit from development/improvement.

Generic Assessment Criteria	Marks available	Marks awarded
1. Engagement with Literature Skills	10	6
Engagement with a wide range of literature sources, including sources retrieved independently. Generally sound referencing, with very few inaccuracies or inconsistencies.		
2. Knowledge and Understanding Skills	35	19
Task 1 achieved 45%. Task 2 achieved 68%, Task 3 achieved 50%. Knowledge of the basic underlying concepts and principles is accurate with a good understanding in most areas. In some of the calculation work you have there are errors, Task 1 the numbers for calculating the resistors are the wrong way around. Also have include all of the design work for some of the circuits.		
3. Cognitive and Intellectual Skills	15	9
Sound evaluation of the underlying concepts and principles for all tasks.		
4. Practical Application Skills	30	16.7
Task 1 achieved 54%. Task 2 achieved 68%. Task 3 achieved 45%. A good application of practical work for Task 1 and 2, very good use of the test equipment and Multisim to obtain the required test results. There were a number of test results missing for Task 3.		
5. Transferable Skills for Life and Professional Practice	10	5.5
Mostly coherent, organised and accurate work, in a suitable structure and is for the most part clearly expressed.		

Assessment Mark (Assessment marks are subject to ratification at the Exam Board. These comments and marks are to give feedback on module work and are for guidance only until they are confirmed.)	Late Submission Penalties (tick if appropriate)		56%
	Up to 1 week late (40% Max)		
	Over 1 week late (0%)		

Assessment 1 for Electronics with Jason Pointer

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Diodes

Both Germanium and Silicon have four valence electrons, which enable them to form four covalent bonds in a rigid three-dimensional grid structure known as “diamond structure” or “lattice crystals”. Germanium has a larger atomic radius because unlike silicon, it has valence electrons in the higher energy d configuration, which gives it higher conductivity at warmer temperatures since there are more free electrons. Because of this it becomes unstable at higher temperatures so is not often used. ✓

Diodes are made of a semiconductor such as silicon or germanium that has been doped with another element having three or five electrons. Semiconductors’ atoms are arranged in a three-dimensional grid structure because each atom has four electrons in its outer valence shell which it shares with the valence shells of the four atoms equidistant around it, forming covalent bonds. When a small amount of atoms with three or five valence electrons are added, there occur places in the material which are electrically positive or negative. They can move freely within the crystal lattice because of its continuous grid structure. ✓

A diode consists of two halves of the same material, one half positively doped (the anode) and one half negative (the cathode). This creates a potential gradient at the junction, where electrons migrate to fill holes, creating an electrical charge depletion zone, but as no current is flowing across the material, there is insufficient energy to deplete very much of it. ✓

This changes the border of the negative zone neutral, with no holes to fill, and the border of the positive zone neutral instead of negative, creating a hinterland where electrical charge energy spent by electron movement diffusing has exhausted the limits it can travel under the influence of charge attraction. ✓

Thermal excitation frees some electrons and their holes, these are called minority carriers, and as the diode heats up at low voltages, this creates leakage current.

Forward biasing applies positive charge to the positive side and negative to the negative. The electrons repulsed towards the depletion zone change the negative side to positive, reducing the depletion zone and its resistance, and increasing the contact potential difference, enabling the free flow of electrons in the direction of charge, viz towards the p-zone, away from the n-zone. A certain initial voltage's energy is wasted un-charging the depletion zone “about 0.2V for germanium and ✓

0.6V for silicon" (Bird, 2019 p.215) but above this charge flows freely. ✓

This initially forces more electrons and holes towards the depletion zone, where more form covalent bonds and the depletion zone widens, increasing resistance. At a certain voltage however, resistance breaks down, firstly because minority carriers continue crossing the depletion zone "since it is, in effect, forward biased for these carriers" (Bird, 2019 p.217a) but with greater energy, colliding with electrons in the p-zone, knocking them loose from covalent bonds so they too move forwards under repulsion from the flow of electrons; this is called the "avalanche effect"; and the applied voltage energy becomes high enough to initiate breaking down of internal covalent bonds, releasing electrons in the direction of current flow. This voltage level is called the "breakdown voltage". ✓

Good intro.

Experiment

The forward and reverse bias outputs of a germanium and a silicon diode were measured, wiring the diode to a breadboard in line with a resistor and applying $V_D = 0.7$ volts in forward bias and $V_D = 9V$ in reverse bias, from which the static and dynamic resistances were calculated.

Results

The static resistance in forwards bias

$$R = V/I$$

$$\text{for Silicon } R = 32.7\text{mA} / 0.7V = 46.7143\text{m}\Omega$$

$$\text{for Germanium } R = 5.15\text{mA} / 0.7V = 7.357\text{m}\Omega$$

Because at both points the graph to 0.8V was straight, the gradient was calculated as:

$$\Delta R = \Delta I \text{ across } 0.7 - 0.8V / \Delta V \text{ } 0.7 - 0.8V \text{ thus:}$$

$$\text{Silicon} = \Delta I (32.7 - 7.41) \times 10^{-3} / \Delta V 1 \times 10^{-1} = 25.29 \times 10^{-2} = 0.2529\Omega \Delta R$$

$$\text{Germanium } \Delta R = \Delta I (6.6 - 5.15) \times 10^{-3} / \Delta V 1 \times 10^{-1} = 1.45 \times 10^{-1} = 0.145\Omega$$

$$\text{Reverse bias static resistance at } -9V \text{ for Silicon is } 105 \times 10^{-3} / -9 = -0.011667\Omega = 11.67\text{m}\Omega$$

$$\text{Reverse bias static resistance at } -9V \text{ for Germanium} = 162 \times 10^{-3} / -9 = -18\text{m}\Omega$$

Silicon graph is straight between -9 – -10.5mA therefore this was used

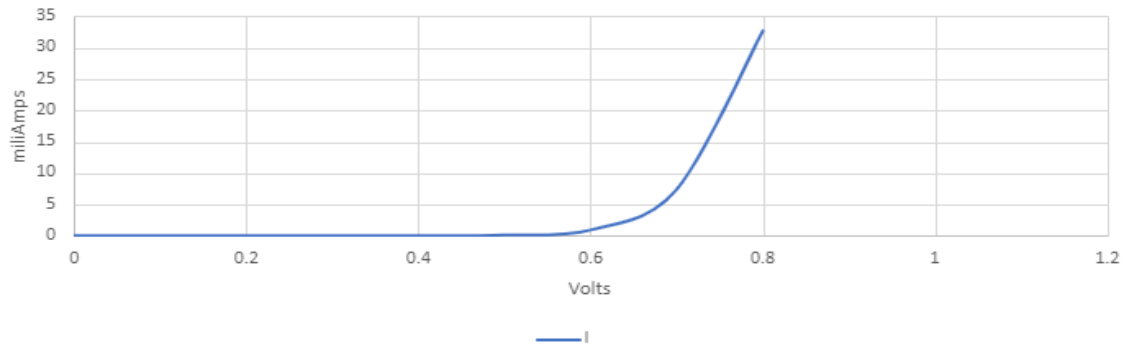
$$\begin{aligned} \text{Dynamic reverse bias resistance for Silicon} &= (108.7 - 102.5) \times (10^{-3}) / (10.5 - 9) \\ &= 6.2 \times 10^{-3} / 1.5 = 4.133\text{m}\Omega \Delta R \end{aligned}$$

Dynamic reverse bias resistance for Germanium: the graph was curved at -9V so the value between -7.5 and -10.5 was used

$$\Delta R = (213 - 118) \times (10^{-3}) / (10.5 - 7.5) = 9.5 \times 10^{-3} / 3 = 0.3167\Omega$$

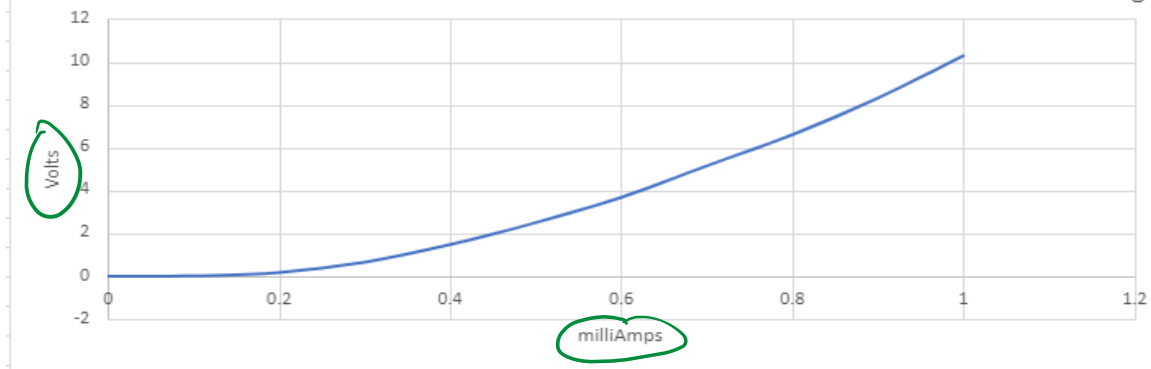
You have used the incorrect prefixes

Forwards current in silicon diodes across voltage increase



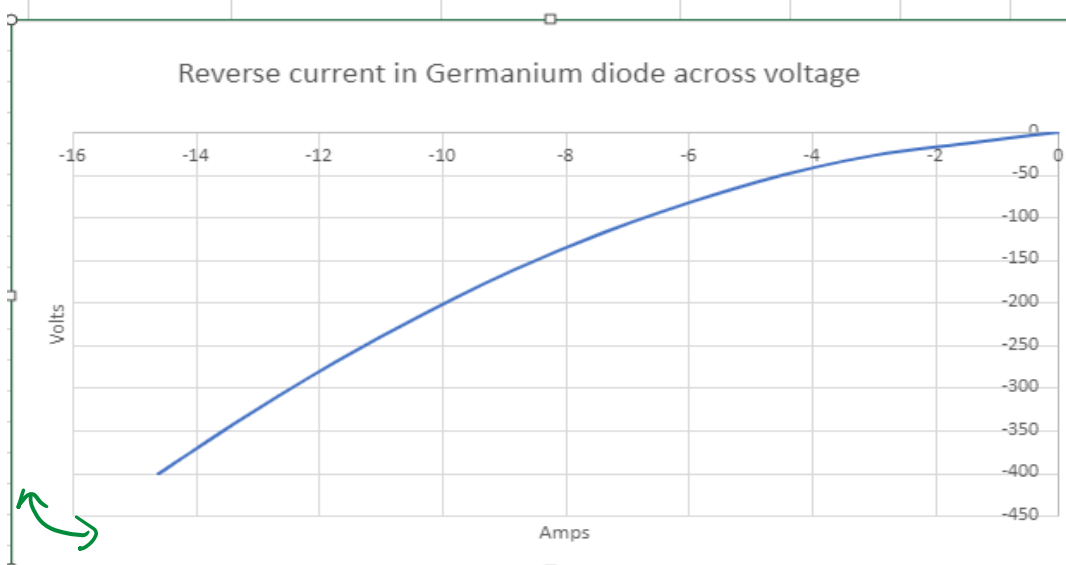
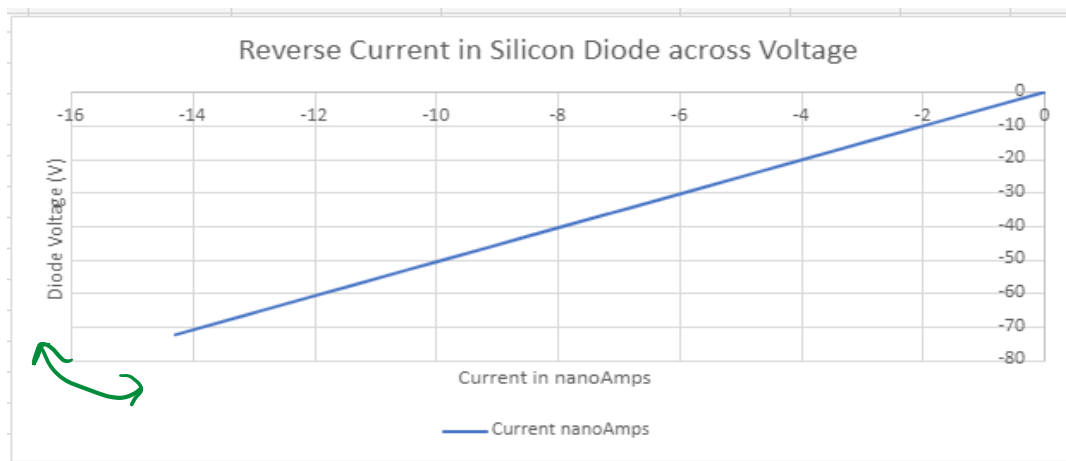
✓

Forwards current in Germanium diode across voltage



✓

Have not included tables of results.



Conclusion

Germanium starts to allow current through at a lower current because it has lower resistance but silicon has more sudden shift to conducting. This is because Germanium has more loose electrons, so minority carriers are moving at lower currents and the avalanche effect starts sooner but is more chaotic and the diamond-crystal structure is stronger so this inhibits conductance comparably at higher currents. Reverse current starts at a higher level in both diodes as the internal resistance of the diode must be overcome. However reverse current breakdown in Germanium is more sudden and leakage current at all levels is far higher. This makes silicon a better semiconductor. ✓

Full Wave Rectifier

When AC current is fed into a diode, only the forward bias pulses exit, the reverse bias cycles are blocked. Output is intermittent DC, half rising and falling phase alternating with half no current.

Full wave DC can be derived from AC by channelling AC down a conductor which forks, one conductor fork accepting current in one direction but blocking the reverse, using diodes, and the second fork only accepting the current that flows in the opposite direction. Whichever way the current flows, it has an exit. By joining these two forks back together, each now single-direction intermittent pulses of DC current, is achieved: both the combined full DC output of AC input, and current filling of the empty halves of phased DC cycles.

(Two diodes suffice when used with a centre-tapped transformer as input so it can earth both cycles, but these are expensive (Bird, 2019 p.291). Therefore circuits using four diodes (“full-wave bridge rectifiers”) are used so that the same earth as the input circuit can be used.)

	Full-Wave Rectification	Half-Wave Rectification
Circuit Configuration		
Input Voltage Waveform		
Voltage Waveform After Rectification		
Voltage Waveform After Rectification Smoothing		

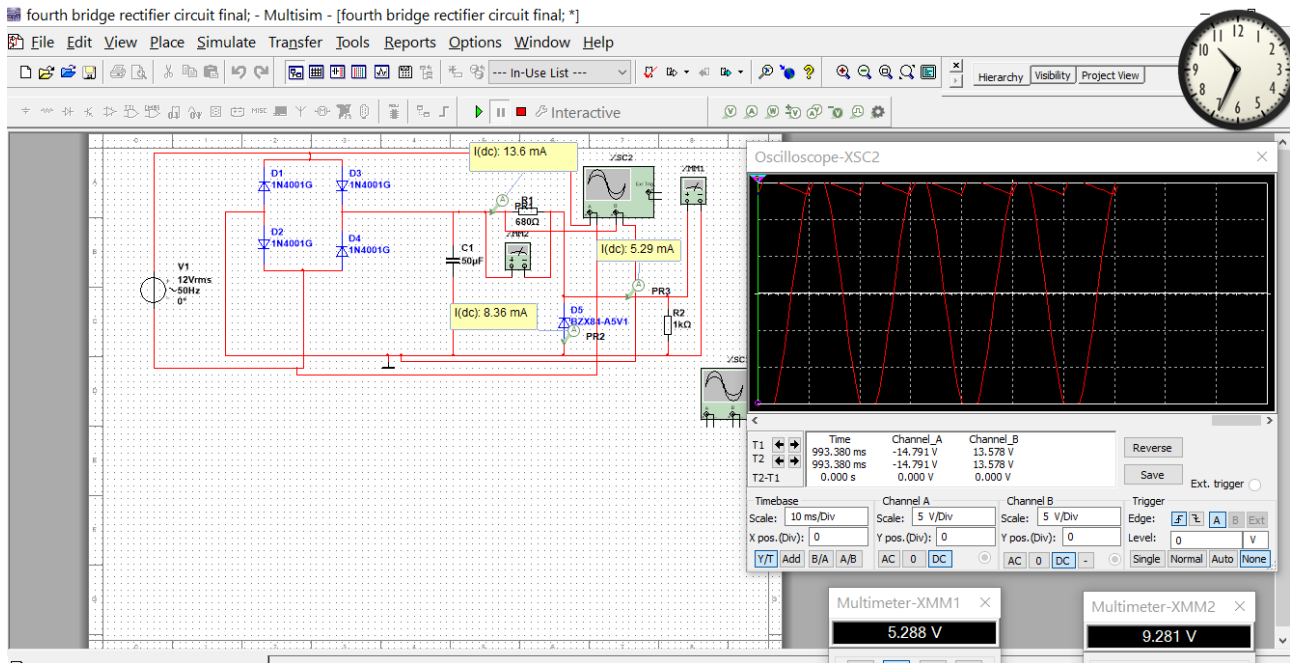
(for some reason they've put lord not load)

From: <https://www.rohm.com/electronics-basics/ac-dc/rectification>

However, this output current constantly rises and falls, being both intermittent (unreliable) and full of surges. This problem can be solved using capacitors. As capacitors fill with charge on the first plate until so much charge is collected that the charge density creates a force of repulsion from more electrons arriving that is greater than the resistance of the electrolyte blocking onward flow to the second capacitor plate is lower and the charge is transmitted onwards in the circuit. Peaks in current collect on the plates and discharge during troughs, so it is called a “reservoir capacitor” (Bird 2019,

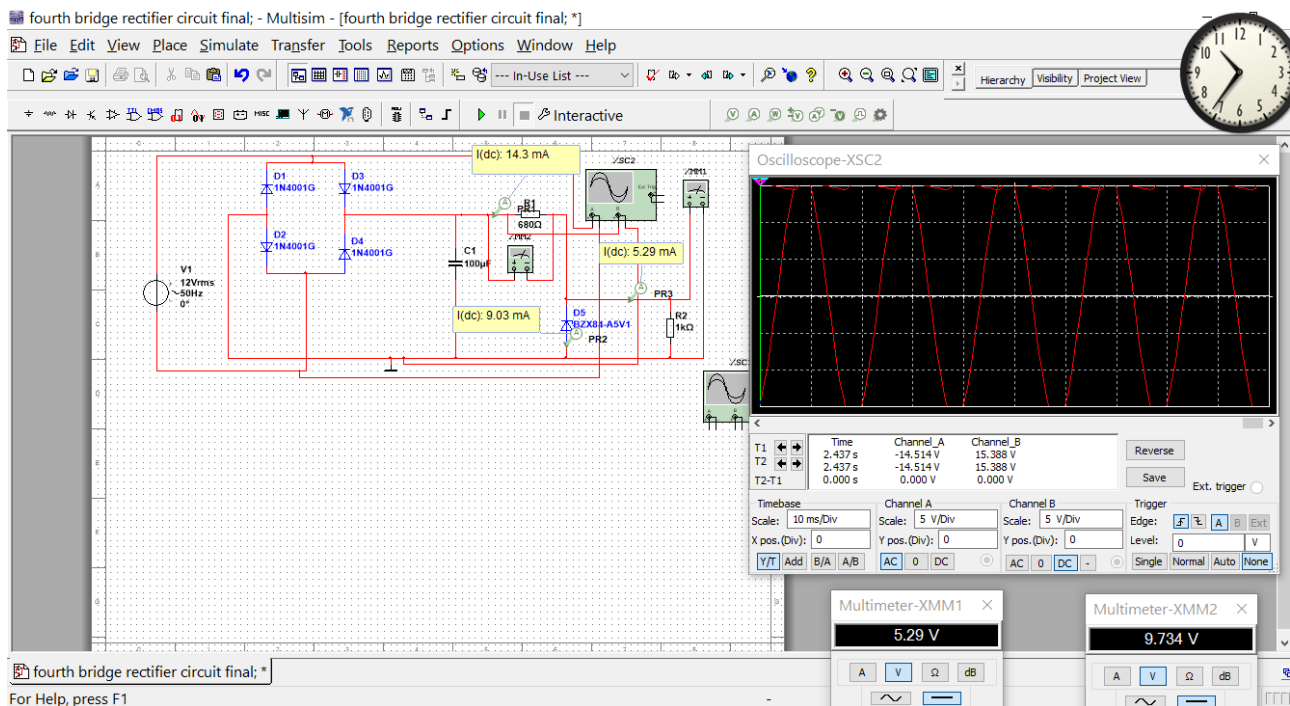
ch.16.9 p.292) A capacitor combined with an inductor to smooth out remaining current “ripple” in capacitor's output is called a rectifier or filter and enables DC devices to function on output current (Bird, 2019).

A full wave rectifier using a BZX84c5V1 microchip was built and tested using multisim.



This shows smoothing with a 50µF capacitor.

The AC wave input and the DC smoothed output are shown together on the oscilloscope.



This shows smoothing with a 100µF capacitor. By comparison with the 50µF capacitor the waveform is much smoother, showing that greater cycle absorption during peaks with longer following release smooths the waveform more. As the capacitance is increased, the ripple effect is reduced. ✓

You have not discussed or shown the design for the regulation.

Bipolar Junction Transistor

A bipolar junction transistor is the next iteration of a diode. It consists of three, not two, charge zones, each with its own electrode. Arranged in alternating layers, they can be NPN or PNP. They work in reverse ways, only the NPN transistor was used and will be discussed. Unlike a diode, they are arranged in concentric valleys around the core ('emitter') charge zone, with the outermost 'collector'. ✓

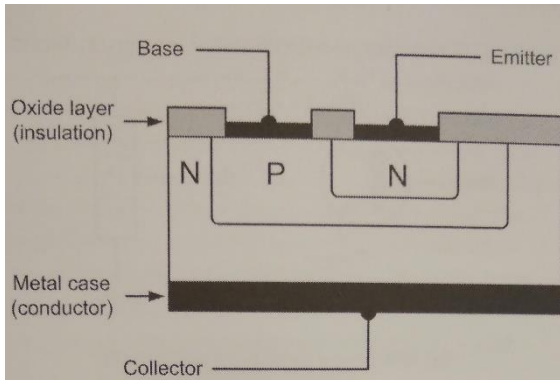
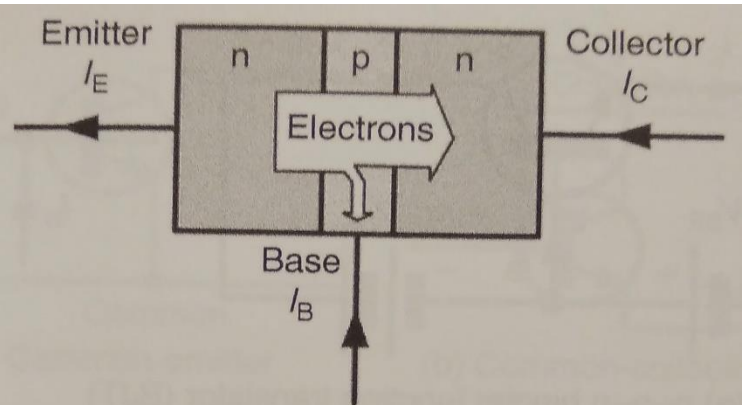


Figure 5.17 NPN transistor construction



(a) n-p-n bipolar junction transistor

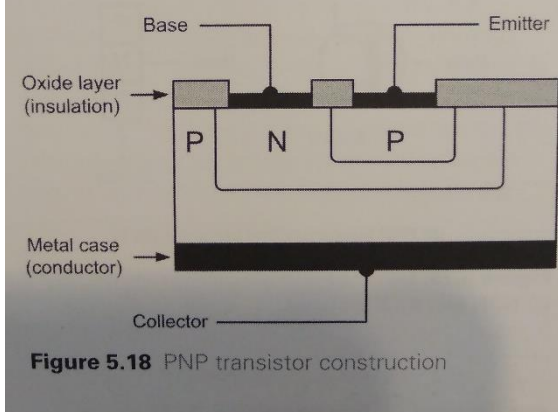
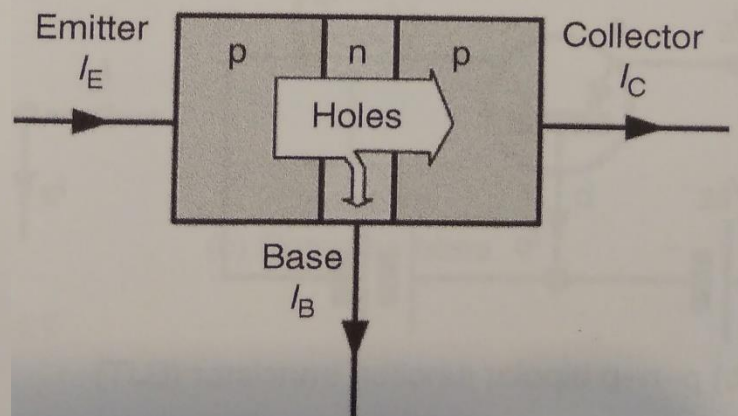


Figure 5.18 PNP transistor construction



(b) p-n-p bipolar junction transistor

Left: image 5.18 from Tooley, 2016 p.99

Right: image 14.6 from Bird, 2019 p.229

The middle layer ('base') in a BJT transistor is very thin, a narrow slice of silicon (Tooley, 2016 p.99) This means that some of the opposite charge flowing into it from the inner or outer zones is partially absorbed and partly flows through into the other zone, so that initial PD is absorbed by the current pushing electrons or holes to form covalent bonds with it, functioning as the depletion zone,

causing resistance by electrons binding to the holes of the thin layer, but above a certain voltage, the current flows on. This gives it the function of a normally-open switch, blocking current flow until sufficient current is applied to the middle, base, layer that electrons can freely from the emitter to the collector. (With PNP transistors, current must be drawn from the emitter through and out of the base, to fill its holes and enable electrons to flow on into the collector region.) So current applied to the base turns it from a normally-open switch to a latching ON switch.

Because the base is thin with few holes, “current flowing in the emitter is typically a hundred times greater than that flowing in the base” (Bird, 2019 p.230) with most flowing on into the collector.

Therefore

$$I_E = I_B + I_C$$

Therefore input resistance is

$$I_R = I_{BE} / I_B \text{ (base-emitter current/base current)}$$

(Like diodes, a leakage current of thermally-generated minority carriers persists, but the base serves as the neutral.)

Initial applied current is increases output current so potential difference does not increase until full flow is reached; therefore collector-emitter PD does not increase because the extra current is constantly being absorbed and flowing through the BJT. This range of input values is called the 'saturation region'.

In the 'active region', the base-emitter junction is forward biased and collector-base junction is reverse biased, so increasing the base input electron current directly decreases the collector-base resistance and proportionally increases the emitter-collector output current.

However, when the depletion layer is saturated, the emitter-collector current cannot increase beyond the BJT's charge-carrying capacity, as it is a diode: this region of constant output current values is called the “active region”. Like diodes, they have a breakdown voltage. In practise, this burns them out.

Because in the 'active region' the output emitter-collector current is directly linearly proportional to input emitter-base current, they are useful as current amplifiers.

DC input outputs a ratio gain h_{FE} specified on the manufacturer's data sheet

$$h_{FE} = \Delta I_C / \Delta I_B$$

AC input is specified as differential, gradient of the curve

$$h_{fe} = \Delta I_C / \Delta I_B$$

When wired with emitter connected to both input and output, they are called “common-emitter amplifier”. Effectively, they are two separate circuits with separate power supplies that join where they both flow through the base and emitter sections of the BJT. Then, the base-emitter-signal input circuit is amplified in fixed proportion h_{FE} by the collector-emitter circuit's output current.

$$I_C = I_B \times h_{FE}$$

Experiment

A common emitter BJT amplifier was designed using a suitable transistor, BJT BC183 with h_{FE} of 318 I_C / I_B as per manufacturer's datasheet REF.

For the quiescent current $I_C = I_Q$ a collector current of 2 mA and voltage of 11V_{CC} were chosen where $R_E R_C$ will balance the current. $R_C = V_{CC} / 2 \times I_C = 11/4$, the nearest resistor value of 2.75k Ω was chosen. 2.7k Ω

V_E should be 10% - 15% of V_{CC} 13% was chosen 1.43V

$$R_E = V_E / I_C = 0.13 \times 11 / 2 \text{ mA} = 1.43 / 0.002 = 715\Omega \text{ the nearest value of } 680\Omega \text{ was used}$$

The base voltage was calculated

$$V_B \text{ should be } 0.7 \text{ higher than } V_E \text{ datasheet } V_B = V_{BE} + V_E = 2.75 + 0.7 = 2.13$$

the value for the base current was calculated

$$I_B = I_C / h_{fe} = 0.002 / 318 = \text{c. } 6.3 \times 10^{-6}$$

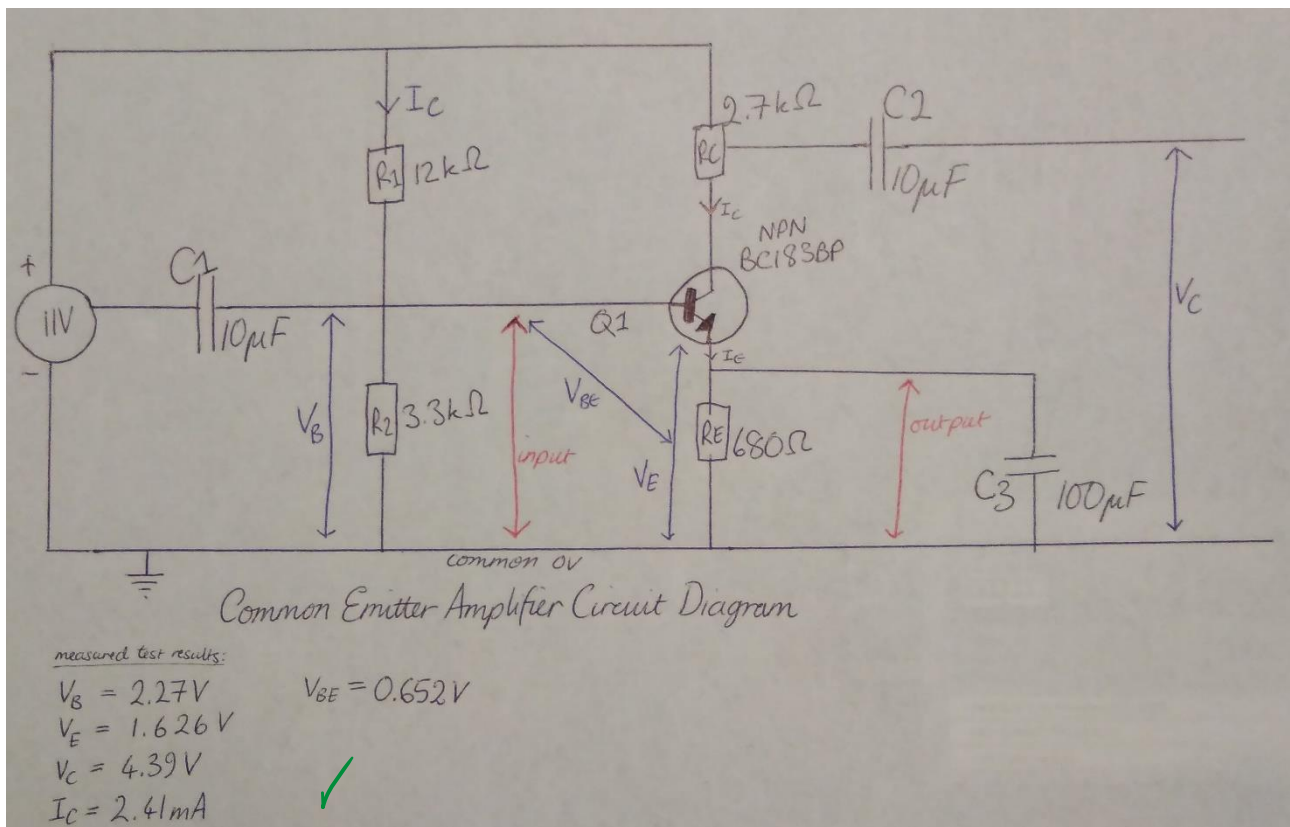
The resistance of R_2 stabilises the bias current

$$R_2 = V_B / 10 \times I_B = 2.13 / 63 \times 10^{-5} = 33.9\text{k}\Omega$$

R_1 is the base voltage divided by the base current

$$R_1 = V_{CC} - V_B / 11 \times I_B = 11 - 2.13 / 11 \times 6.3 \times 10^{-6} = 8.87/11 \times 6.3 \times 10^{-6} = 128\text{k}\Omega$$

The circuit was built and measured under both DC and AC conditions. The circuit was then built and tested under DC conditions on Multisim in order to compare experimental with ideal results.



Common Emitter Amplifier design circuit diagram.

The diagram show the wrong size resistors for R_1 and R_2 .

The maximum possible signal output of a BJT-CEA is the maximum current multiplied by the fraction ratio f_{HE} so $I_E = I_B + I_C$

R_1 & R_2 divide the voltage into emitter-base circuit voltage and current and emitter-collector voltage and current. This determines the ratio of current flowing out the base and out the collector, so controlling how saturated the collector-base junction is and how much current from the output current I_C can flow from emitter to collector.

The voltage divider created by R_1 & R_2 because R_2 increases forward bias and forward bias is inversely proportional to R_1 so the ratio of the input current across them fixes the signal to be amplified so that it does not distort. It holds the signal stable. This is vital because the difference between the AC cycles is magnified, bias up to 180° can erase half the cycle.

Capacitors are used as voltage regulators to remove AC signal distortions and remove low frequency signal which is like removing outliers from statistics, it clarifies signal contrast and removes errors, increasing bandwidth by reducing gain at low end and increasing it across the centre of the signal.

When the base-emitter region is saturated all resistance becomes negligible and maximum output current signal flows. Because the base-emitter junction is much thinner and less doped than the base-collector junction, it is very quickly saturated so the input current needs to be held very low, in this case $2\mu\text{A}$ was chosen. This also enables maximum possible output signal.

Once I_C saturation of base-emitter junction is reached, maximum current can flow through to the collector and the base-collector junction becomes saturated. After saturation, both junctions are forward-biased to incoming current, small increments in input voltage V_{CE} cause hugely magnified output current I_C changes, until build-up of electrons at the collector causes an increasing negative charge slope exiting the BJT and this holds a limit on exit current, which stays stable across collector-emitter voltage increases. This is called the “cut-off zone”.

As V_{CC} increases, the collector-base depletion zone increases, increasing its resistance to I_C which proportionally reduces. This gives common emitter amplifiers the characteristic that alterations in output voltage change input current flow which proportionally increases input voltage.

The current input to the base and output the emitter needs to operate at Quiescent current Q_1 of half the input load to avoid distorting output signal, this is achieved by balancing viz. $V_{CE} = V_{CC} / 2$

Results

When built, the circuit tested as:

$$V_B \text{ across } R_2 = 2.27\text{V}$$

$$V_E = 1.626\text{V}$$

$$V_C = 4.39\text{V}$$

$$V_{BE} = 0.652\text{V}$$

$$I_C = 2.41\text{mA}$$

$V_E + V_{BE} = V_B$ so $V_B - V_{BE} = V_E$ but $2.27 - 1.626 = 0.644$ showing 0.006 difference from measured quantities



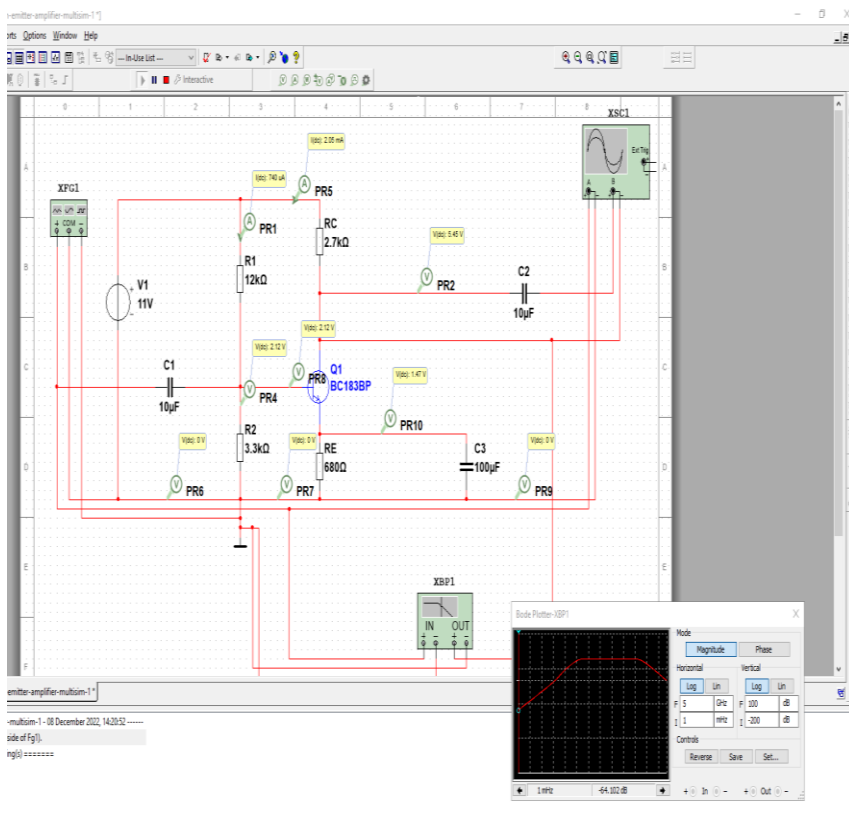
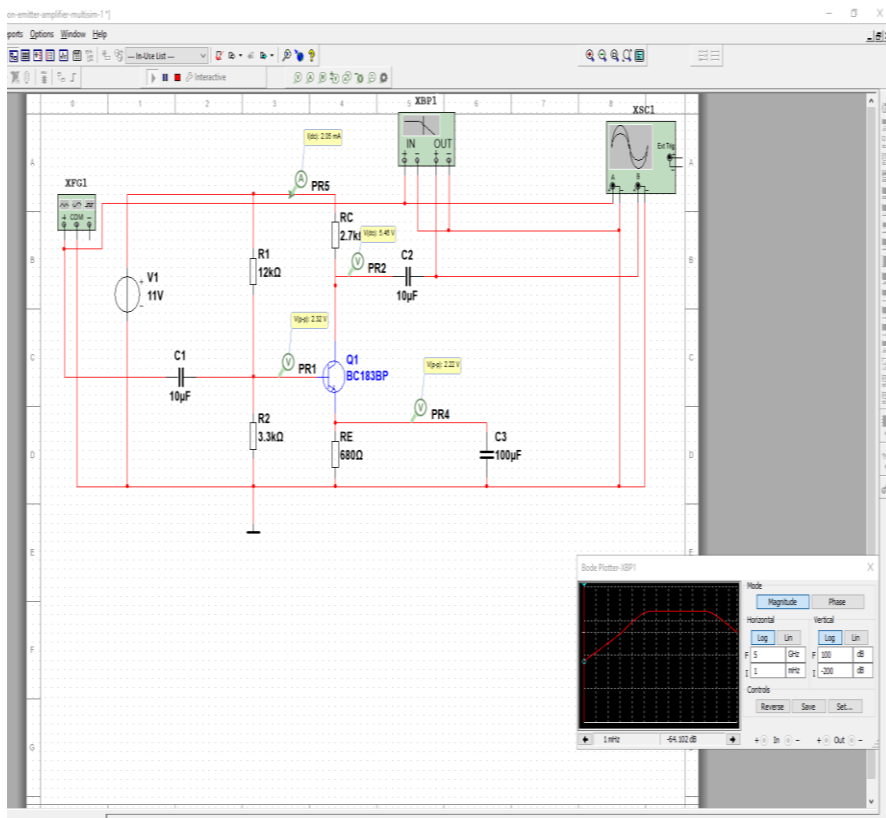
Results: max. gain = 46.6dB

Half power point: $46.6 - 3 = 43.4\text{dB}$

$f_2 = 61.2\text{MHz}$

$f_1 = 0.14\text{Hz}$

Bandwidth = $f_2 - f_1 = 61200 - 0.14 = 61199.86 = 61.2\text{MHz}$



Design values:

$$V_B = 2.13V$$

$$V_E = 1.43V$$

$$I_C = 2mA$$

$$R_C = V_{CC} / 2 \times I_C = 11/0.004 = 2750\Omega$$

$$V_C = I_C \times R_C = 0.002 \times 2750 = 5.5V$$

$$V_{BE} = V_B - V_E = 2.13V - 1.43V = 0.7V$$

Multisim AC simulation results were:

$$I_C = 2.05mA$$

$$V_B = 2.33V \text{ and } 2.12V$$

$$V_C = 5.45V$$

$$V_E = 2.22V \text{ and } 1.47V$$

$$\text{gain} = 64dB/1mHz$$

When built, the circuit tested as:

$$V_B \text{ across } R_2 = 2.27V$$

$$V_E = 1.626V$$

$$V_C = 4.39V$$

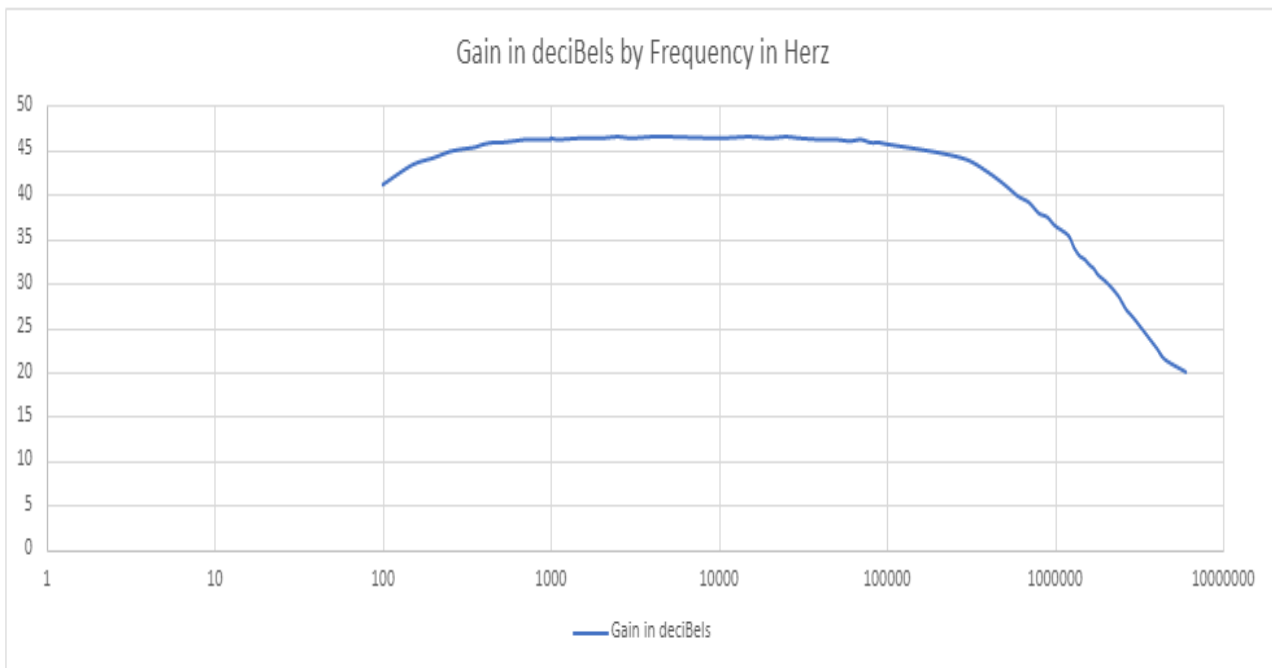
$$V_{BE} = 0.652V$$

$$I_C = 2.41mA$$

$$\text{max. Gain} = 46.6dB$$

$$\text{bandwidth} = 61.2MHz$$

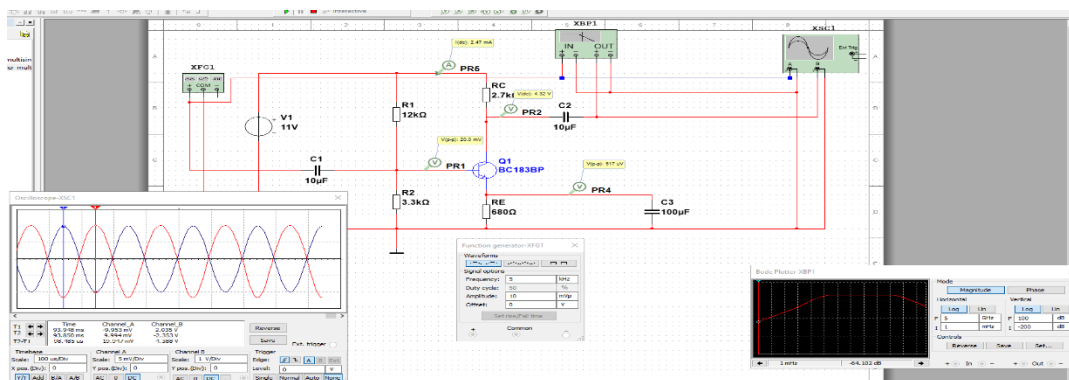
$$\text{half power point} = 43.4dB$$



Conclusion

This shows consistent but not significant differences between theoretical and actual results.

There are several reasons for this. First, the circuit was built using approximate resistor values approximating input design values. Second, components especially resistors have tolerances which apply small multiplications of inaccuracy across the circuit. Thirdly, human error results in conductors not fully touching or touching and short-circuiting, especially multimeter probes. ✓



This shows the cycle's amplification.

Multisim DC simulation results:

$$I_C = 2.47\text{mA}$$

$$V_B = 20\text{mV}$$

$$V_C = 4.32\text{V}$$

Why include this?

$$V_E = 517\mu\text{V}$$

$$\text{gain} = 64\text{dB}/1\text{mHz}$$

Under DC conditions the amplification is far lower but the bandwidth remains the same.

For f_{HE} values see appendix 1 manufacturer's datasheet.

Operational Amplifier

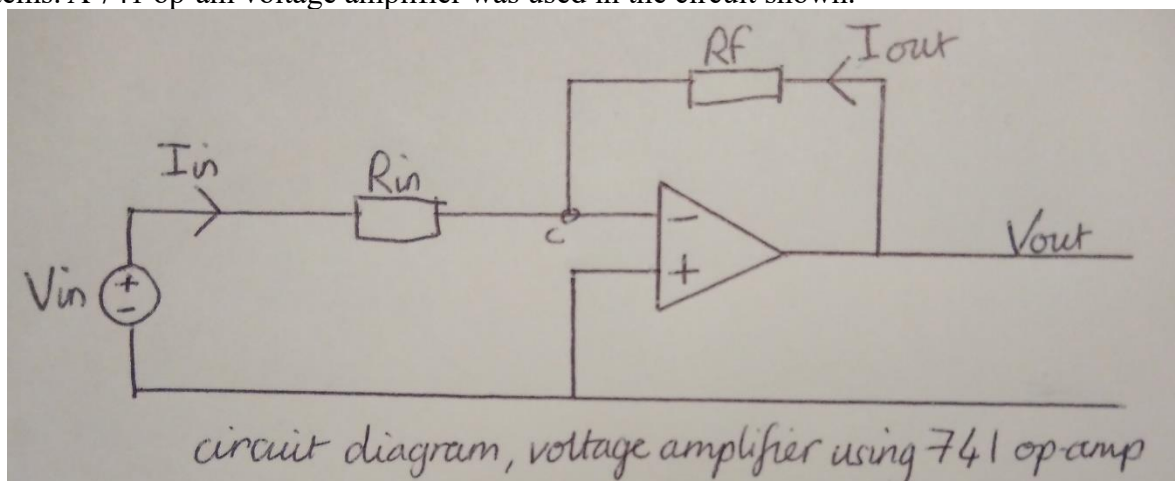
An operational amplifier ("op-amp") amplifies the differences between two voltage inputs. Both input and output supply have their own power supply and share neutral, which is connected to the op-amp and used the reference voltage of 0V (Tooley, 2016 p.161) The difference between input1 and input2 is output multiplied by the gain factor A_{VO}

$A_{VO} = V_{out} / V_{in}$ where A_{VO} = gain for open-loop voltage. ✓

Because the open-loop gain is unlimited, it easily becomes very high, distorting the signal. This limits the range of input voltage difference that can be amplified without distortion. This extremely high open loop DC gain A_{VO} of an operational amplifier is uncontrollable unless resistance is put into its circuit. In order to increase the range, the output gain needs to be limited resistance. Inverting the output and feeding it back into the op-amp circuit not only provides both more stable, less distorted, wider signal range, but does so in proportionally, preserving the ratio of gain and therefore the faithful reduplication of the input signal. Gain is reduced but signal breadth increased. (Bird, 2019 p.368) Gain is always directly inverse of bandwidth, since their product is static (Tooley, 2016 p.165). (Inversion is in fact 180° phase shifting.) Finally, it stabilises the current values, so that the circuit is easily controlled. ✓

Experiment

An op-amp circuit was designed to output a gain of around 20+Hz in order to be suitable for audio systems. A 741 op-am voltage amplifier was used in the circuit shown.



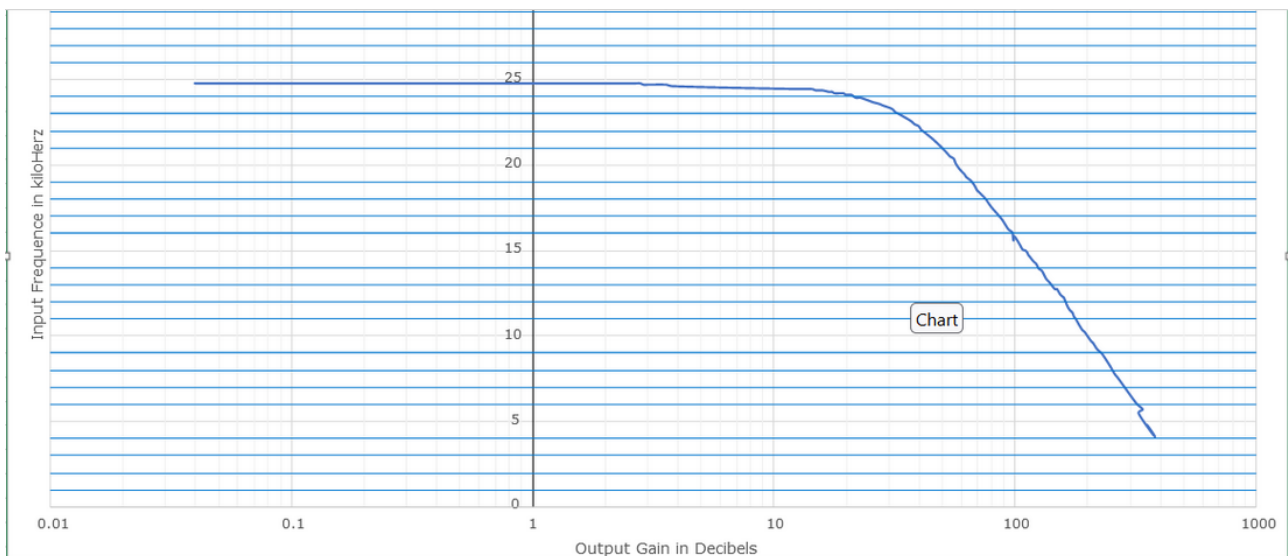
Voltage gain can be calculated using voltage or resistance:

$$V_{gain} = V_{out} / V_{in} = -R_f / R_{in}$$

✓

Need to show how the resistor value were calculated

Have not included all measured values.



Op-Amp graph of output gain in decibels across input frequency in kiloherz

The gain is above 18, so audible and usable in a pre-amp for audio, from 0.04 – 72Hz

Results: max. gain = 24.75dB

Half power point $24.75 - 3 = 21.75\text{dB}$ ✓

$f_2 = 42\text{kHz}$ (using results tables)

$f_2 =$ since it starts high, assuming initial signal frequency of 0.04kHz

Bandwidth = $f_2 - f_1 = 42 - 0.04 = 41.96\text{kHz}$ ✓

This is the signal range across which the amplifier would be useable. ✓

The slew rate is the amount of voltage the op-amp signal can rise or fall per μS . The 741 cannot change rise or fall more than 0.5V signal output each μS . Therefore if the signal rises or falls far more per μS , the signal lags, so the slope of the rate of change will be more gradual and the signal speed has changed. Digital signals and square wave-forms therefore become curved and so this distortion can alter the signal's wave shape. In audio terms, clear sudden spikes in noise or silence would fade in and out more and contrast and clarity would be lost. ✓

References

Bird, J. (2019) *Electrical and Electronic Principles and Technology* 6th Edn. New York: Routledge.

Tooley, M. (2016) *Electronic Circuits: Fundamentals and Applications* 4th Edn. New York: Routledge.



Rohm at: <https://www.rohm.com/electronics-basics/ac-dc/rectification> Accessed: 29/1/23.

Bibliography

Bird, J. (2019) *Electrical and Electronic Principles and Technology* 6th Edn. New York: Routledge.

Doyle, S (2021) *WJEC Mathematics: Applied*. Cheltenham, Gloucester: Illuminate.

Tooley, M. (2016) *Electronic Circuits: Fundamentals and Applications* 4th Edn. New York: Routledge.

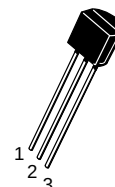
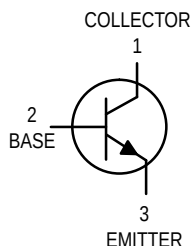


Appendices

Amplifier Transistors

NPN Silicon

BC182,A,B
BC183
BC184



CASE 29-04, STYLE 17
TO-92 (TO-226AA)

MAXIMUM RATINGS

Rating	Symbol	BC 182	BC 183	BC 184	Unit
Collector–Emitter Voltage	V_{CEO}	50	30	30	Vdc
Collector–Base Voltage	V_{CBO}	60	45	45	Vdc
Emitter–Base Voltage	V_{EBO}	6.0			Vdc
Collector Current — Continuous	I_C	100			mAdc
Total Device Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	350 2.8			mW mW/°C
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	1.0 8.0			Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to +150			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	357	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	125	°C/W

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Collector–Emitter Breakdown Voltage ($I_C = 2.0\text{ mA}$, $I_B = 0$)	BC182 BC183 BC184	$V_{(BR)CEO}$	50 30 30	— — —	— — —	V
Collector–Base Breakdown Voltage ($I_C = 10\text{ }\mu\text{A}$, $I_E = 0$)	BC182 BC183 BC184	$V_{(BR)CBO}$	60 45 45	— — —	— — —	V
Emitter–Base Breakdown Voltage ($I_E = 100\text{ }\mu\text{A}$, $I_C = 0$)		$V_{(BR)EBO}$	6.0	—	—	V
Collector Cutoff Current ($V_{CB} = 50\text{ V}$, $V_{BE} = 0$) ($V_{CB} = 30\text{ V}$, $V_{BE} = 0$)	BC182 BC183 BC184	I_{CBO}	— — —	0.2 0.2 0.2	15 15 15	nA
Emitter–Base Leakage Current ($V_{EB} = 4.0\text{ V}$, $I_C = 0$)		I_{EBO}	—	—	15	nA

BC182,A,B BC183 BC184**ELECTRICAL CHARACTERISTICS** ($T_A = 25^\circ\text{C}$ unless otherwise noted) (Continued)

Characteristic		Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS						
DC Current Gain ($I_C = 10\ \mu\text{A}$, $V_{CE} = 5.0\ \text{V}$) ($I_C = 2.0\ \text{mA}$, $V_{CE} = 5.0\ \text{V}$) ($I_C = 100\ \text{mA}$, $V_{CE} = 5.0\ \text{V}$)	BC182	h_{FE}	40	—	—	—
	BC183		40	—	—	
	BC184		100	—	—	
	BC182		120	—	500	
	BC183		120	—	800	
	BC184		250	—	800	
	BC182		80	—	—	
	BC183		80	—	—	
	BC184		130	—	—	
Collector–Emitter On Voltage ($I_C = 10\ \text{mA}$, $I_B = 0.5\ \text{mA}$) ($I_C = 100\ \text{mA}$, $I_B = 5.0\ \text{mA}$) ⁽¹⁾		$V_{CE(sat)}$	— —	0.07 0.2	0.25 0.6	V
Base–Emitter Saturation Voltage ($I_C = 100\ \text{mA}$, $I_B = 5.0\ \text{mA}$) ⁽¹⁾		$V_{BE(sat)}$	—	—	1.2	V
Base–Emitter On Voltage ($I_C = 100\ \mu\text{A}$, $V_{CE} = 5.0\ \text{V}$) ($I_C = 2.0\ \text{mA}$, $V_{CE} = 5.0\ \text{V}$) ($I_C = 100\ \text{mA}$, $V_{CE} = 5.0\ \text{V}$) ⁽¹⁾		$V_{BE(on)}$	— 0.55 —	0.5 0.62 0.83	— 0.7 —	V
DYNAMIC CHARACTERISTICS						
Current–Gain — Bandwidth Product ($I_C = 0.5\ \text{mA}$, $V_{CE} = 3.0\ \text{V}$, $f = 100\ \text{MHz}$) ($I_C = 10\ \text{mA}$, $V_{CE} = 5.0\ \text{V}$, $f = 100\ \text{MHz}$)	BC182	f_T	—	100	—	MHz
	BC183		—	120	—	
	BC184		—	140	—	
	BC182		150	200	—	
	BC183		150	240	—	
	BC184		150	280	—	
Common Base Output Capacitance ($V_{CB} = 10\ \text{V}$, $I_C = 0$, $f = 1.0\ \text{MHz}$)		C_{ob}	—	—	5.0	pF
Common Base Input Capacitance ($V_{EB} = 0.5\ \text{V}$, $I_C = 0$, $f = 1.0\ \text{MHz}$)		C_{ib}	—	8.0	—	pF
Small–Signal Current Gain ($I_C = 2.0\ \text{mA}$, $V_{CE} = 5.0\ \text{V}$, $f = 1.0\ \text{kHz}$)	BC182	h_{fe}	125	—	500	—
	BC183		125	—	900	
	BC184		240	—	900	
	BC182A		125	—	260	
	BC182B		240	—	500	
Noise Figure ($I_C = 0.2\ \text{mA}$, $V_{CE} = 5.0\ \text{V}$, $R_S = 2.0\ \text{k}\Omega$, $f = 1.0\ \text{kHz}$) ($I_C = 0.2\ \text{mA}$, $V_{CE} = 5.0\ \text{V}$, $R_S = 2.0\ \text{k}\Omega$, $f = 1.0\ \text{kHz}$, $f = 200\ \text{Hz}$)	BC184	NF	—	2.0	4.0	dB
	BC182		—	2.0	10	
	BC183		—	2.0	10	
	BC184		—	2.0	4.0	

1. Pulse Test: T_p 300 s, Duty Cycle 2.0%.

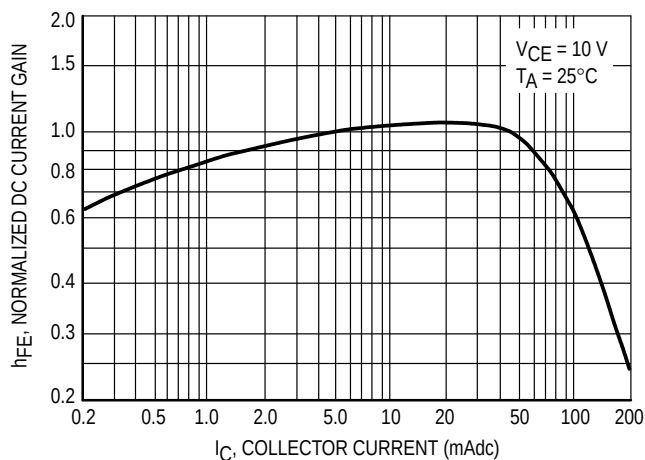


Figure 1. Normalized DC Current Gain

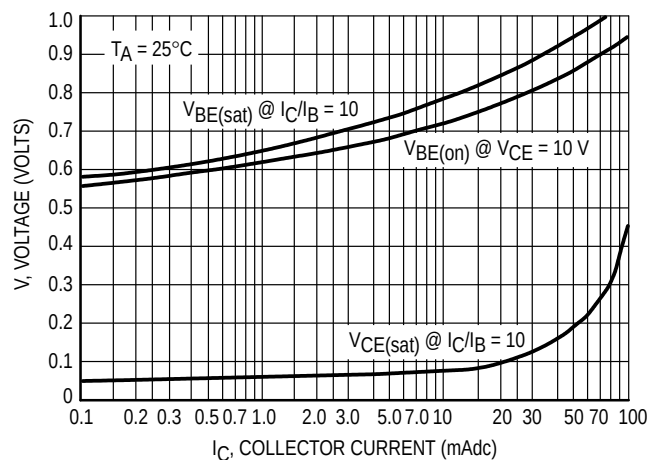


Figure 2. "Saturation" and "On" Voltages

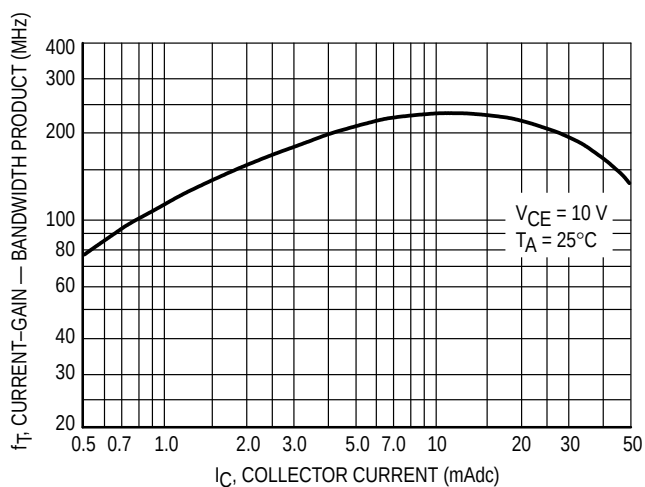


Figure 3. Current-Gain — Bandwidth Product

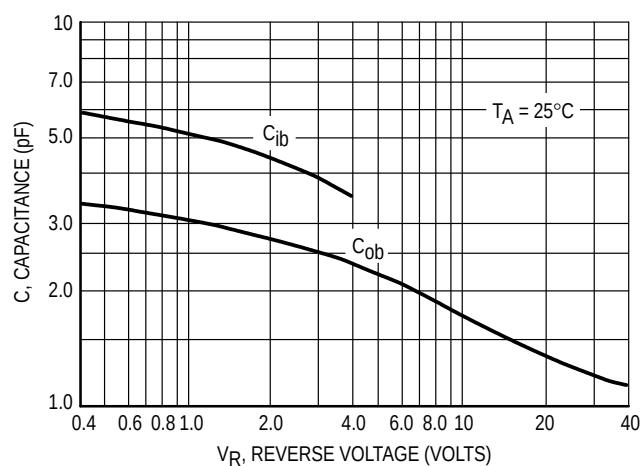


Figure 4. Capacitances

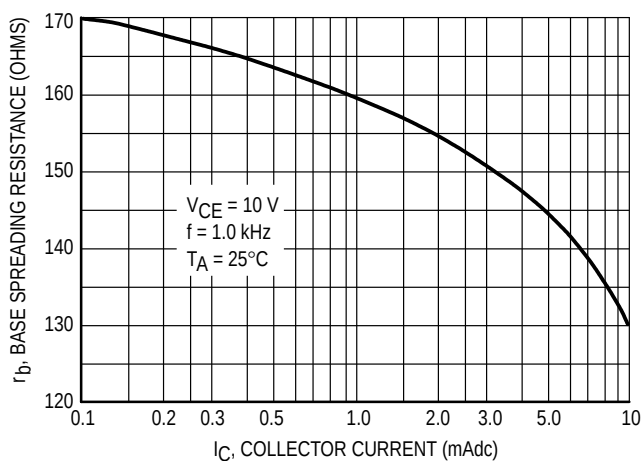


Figure 5. Base Spreading Resistance