



Prifysgol Cymru
Y Drindod Dewi Sant
University of Wales
Trinity Saint David

RESULT

61%

School of Applied Computing ASSIGNMENT SPECIFICATION

Student name:	Richie Jones	Student P number:	
Programme:	HND Electrical/Electronic Engineering		
Lecturer:	Jason Pointer	Internal Verifier:	Steve Roberts
Assignment Title:	Digital Circuits		
Hand Out Date:	23/03/18	Submission deadline:	11/05/18

Referencing:	In the main body of your submission you must give credit to authors on whose research your work is based. Append to your submission a reference list that indicates the books, articles, etc. that you have read or quoted in order to complete this assignment (e.g. for books: surname of author and initials, year of publication, <u>title of book</u> , edition, publisher: place of publication).		
Disclosure:	I declare that this assignment is all my own work and that I have acknowledged all materials used from the published or unpublished works of other people. All references have been duly cited.		
Student's Signature:	Hardcopy assignments will not be accepted without a signature here	Date:	

Late submission will result in a late penalty mark, as follows:

Up to one week late, maximum mark of 40% for first attempts and 0% for resubmissions.

(Academic Quality Handbook 2015/16 7.5 (5))

Learning Outcomes tested (from module syllabus)

1. Demonstrate an understanding of semi-conductor components and characteristics and their application in analogue and **digital** electronic circuits.
2. To design, simulate, build, test and evaluate analogue and **digital** electronic circuits using information gained from datasheets.

MARKING CRITERIA AND STUDENT FEEDBACK

This section details the assessment criteria. The *extent* to which these are demonstrated by you determines your mark. The marks available for each criterion are shown. Lecturers will use the space provided to comment on the achievement of the task(s), including those areas in which you have performed well and areas that would benefit from development/improvement.

Common Assessment Criteria Applied	Marks available	Marks awarded
1. Research-informed Literature Extent of research and/or own reading, selection of credible sources, application of appropriate referencing conventions	10	4
References to a limited range of mostly relevant sources. Some omissions and minor errors.		
2. Knowledge and Understanding of Subject Extent of knowledge and understanding of concepts and underlying principles associated with the discipline	30	20
Knowledge is extensive. Exhibits very good understanding of digital circuits. Did not simplify the Boolean equations.		
3. Analysis Analysis, evaluation and synthesis; logic, argument and judgement; analytical reflection; organisation of ideas and evidence	20	10.5
Evidence of some logical, analytical thinking. Has analyse new data and situations without guidance.		
4. Practical Application and Deployment Deployment of methods, materials, tools and techniques, application of concepts; formulation of innovative and creative solutions to solve problems	30	22
Excellent practical work, very little guidance was needed. All relative results were obtain and showed a clear understanding of the design work.		
5. Skills for Professional Practice Attributes in professional practice; individual and collaborative working; deployment of appropriate media; presentation and organisation	10	4.5
Work lacks coherence in places and could be better structured.		

Assignment Mark (Assessment marks are subject to ratification at the Exam Board. These comments and marks are to give feedback on module work and are for guidance only until they are confirmed.)

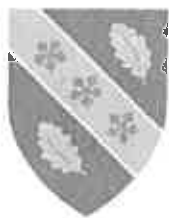
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First Attempt?

✓

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LEVEL/ LEFEL 4

SEMESTER 2

MODULE CODE/ COD Y MODIWL: PSDE 4004 - ELECTRONICS 1

ASSESSMENT TYPE/ MATH O ASESU: ASSIGNMENT

ASSESSMENT/COMPONENT/ ASESAD/CYDRAN: 3

COMPONENT WEIGHTING/ PWYSAU'R CYDRAN: 35%

WORD COUNT/ NIFER Y GEIRIAU: XXXX WORDS/O EIRIAU

MODULE TUTOR / TIWTOR Y MODIWL: Jason Pointer

SUBMISSION DETAILS/ MANYLION CYFLWYNO:

- Make sure that Your Name , Your Student P Number, Your Module Title, Assignment Title and Your Module Lecturer's Name are clearly shown on the front page of your assignment
- All assignments must be submitted electronically to Turnitin unless indicated by the module lecturer here:
- If a paper submission is required then it will be indicated here: Yes
you will then be required to submit the assignment parts in a suitable report folder—not in poly-pockets - to the library.
- For paper submissions this form (ALL PAGES) MUST be printed out, signed, attached to the front of your assignment and submitted to the library separately from your electronic assignment submission.
- Assignments will not be accepted without this form as it is a requirement that you sign the disclosure regarding the referencing convention.
- DO NOT put this form into Turnitin or it will match many similarities with other students' submissions.



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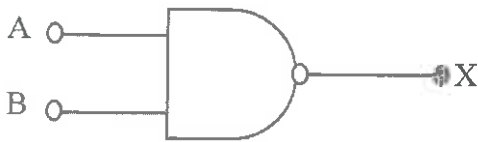
1. Demonstrate an understanding of semi-conductor components and characteristics and their application in analogue and **digital** electronic circuits.
2. To design, simulate, build, test and evaluate analogue and **digital** electronic circuits using information gained from datasheets.

TASK DESCRIPTION

Part 1 - Combinational Logic

Construct and test the following circuits using NAND gates. For each circuit complete a truth table and measure the logic value at each point indicated in the truth table. Write down the simplified Boolean expression and check that the measured values agree with the expected values.

(a)

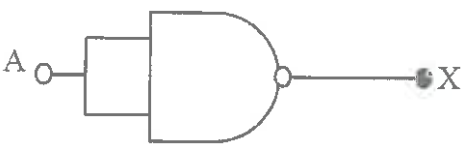


A	B	X
0	0	1
0	1	1
1	0	1
1	1	0

$$X = \bar{A}\bar{B} + \bar{A}B + A\bar{B} = \bar{A}\bar{B}$$

Could have included an introduction

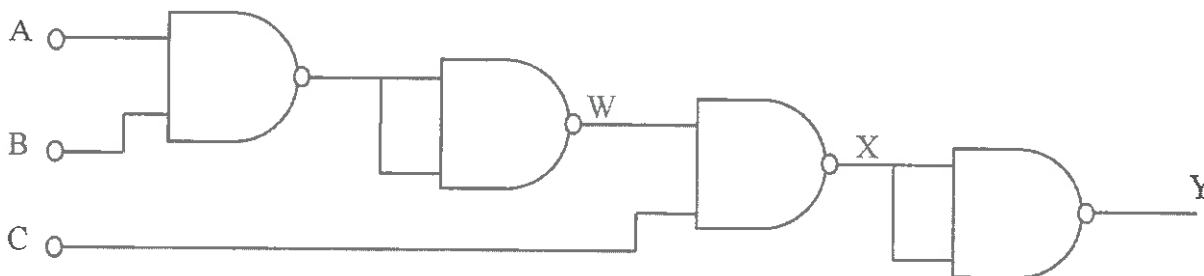
(b)



A	X
0	1
1	0

$$X = \bar{A}$$

(c)



A	B	C	W	X	Y
0	0	0	0	1	0
0	0	1	0	1	0
0	1	0	0	1	0
0	1	1	0	1	0
1	0	0	0	1	0
1	0	1	0	1	0
1	1	0	1	1	0
1	1	1	1	0	1

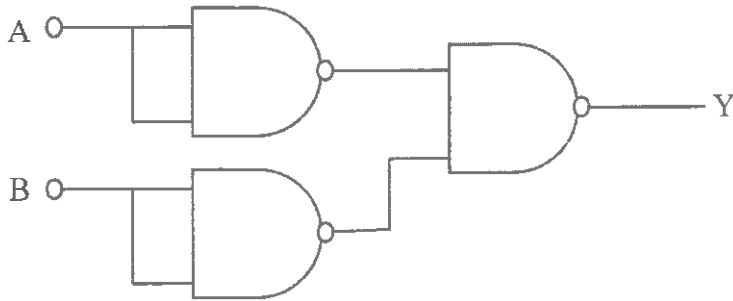
State the logic function for W, X and Y and simplify.

W = AB (two-input AND gate)

X = $\bar{A}\bar{B}\bar{C}$ (three-input NAND gate)

Y = ABC (three-input AND gate)

- (d) What will be the output of the circuit below? If A of circuit (b) is connected to Y what will be the new output.



A)

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

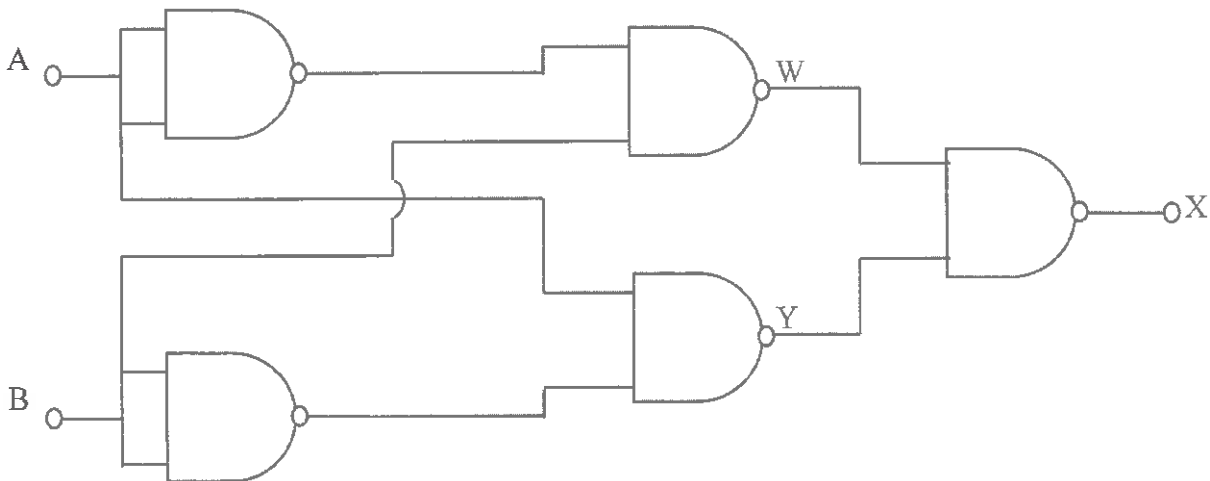
$$X = A + B \text{ (OR gate)}$$

B)

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

$$X = \overline{A + B} \text{ (NOR gate)}$$

- (e) Construct the following circuit and measure the logic values at W, Y and X. Determine the output equation and confirm that the theoretical values agree with the measured values.



A	B	W	Y	X
0	0	1	1	0
0	1	0	1	1
1	0	1	0	1
1	1	1	1	0

$$X = \bar{A}B + A\bar{B} \text{ (XOR gate)}$$

When the circuit was constructed the results given agreed with the truth table above.

Answer the following questions:

1. Compare the following logic families:

- ECL,
- TTL,
- CMOS.

ECL (Emitter Coupled Logic)

- ECL is based on use of current steering switch, using a differential transistor pair.
- ECL is the fastest logic family, due to avoidance of saturation region for application
- Propagation rate is about 1-2ns
- Noise immunity and power dissipation is worst of all the logic families.
- High Level is 0.8V and Low Level is 1.8V
- Has differential input amplifier, internal temperature and voltage compensated bias network; either follower output
- ECL gate provides both true as well as complemented outputs

TTL (Transistor Transistor Logic)

- TTL gate has 3 different type of output configurations:
 1. Open collector output
 2. Totem pole output
 3. Three state output (tristate)
- Totem pole provide less power dissipation, high speed of operation and high fanout
- Standard TTL series of logic families starts with 7404, 74586 & 74ALS161
- The other two families are for military and industrial application; 54-military and 84-industrial

CMOS (Complementary Metal Oxide Semiconductor)

- MOS logic families has more delay as compared to transistor logic families
- lowest power dissipation
- excellent noise immunity
- high parking density
- wide range of power supply
- highest fanout among all logic families

(<http://www.rfwireless-world.com/Terminology/Difference-between-TTL-ECL-CMOS.html>)

2. Simplify the following Boolean equations, ONLY using the LAWS OF BOOLEAN ALGEBRA and DeMORGANS THEOREM. Verify your findings by constructing the logic circuits using NAND gates.

i) $F = A(A + \bar{B})$

$$= A.A + A.\bar{B}$$

$$A.A = A$$

$$= A + A.\bar{B} = A(1 + \bar{B}) = A$$

ii) $F = (A + B)(C + A)$

$$F = AC + AA + BC + BA = AC + A + BC + BA$$

$$F = A(C + 1 + B) + BC = A + BC$$

$$\bar{F} = \overline{A + BC}$$

$$\bar{F} = \bar{A}.\bar{BC}$$

$$F = \overline{\bar{A}.\bar{BC}}$$

Not completed and have not been verified

Part 2 - Using Combinational Logic to Solve Real Problems

(a)

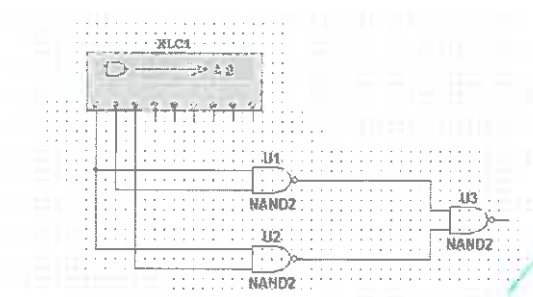
Binary Coded Decimal (BCD) is a 4-bit binary code with the range of numbers 1010 to 1111 not used. Design a circuit that will detect these invalid codes. Construct the circuit and verify that it performs the required task.

Use the following method: State problem $\longrightarrow$ Construct truth table $\longrightarrow$ Extract Boolean expression $\longrightarrow$ Simplify expression $\longrightarrow$ Construct logic diagram.

$$X = \overline{A}\overline{B}\overline{C}\overline{D} + \overline{A}\overline{B}CD + A\overline{B}\overline{C}\overline{D} + A\overline{B}\overline{C}D + ABC\overline{D} + ABCD$$

A	B	C	D	X
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

AB/CD	00	01	11	10
00				
01				
11	1	1	1	1
10			1	1



$$X = A.B + A.C$$

$$\overline{X} = \overline{A.B + A.C}$$

$$\overline{X} = \overline{(A.B) . (A.C)}$$

$$X = \overline{(A.B) . (A.C)}$$

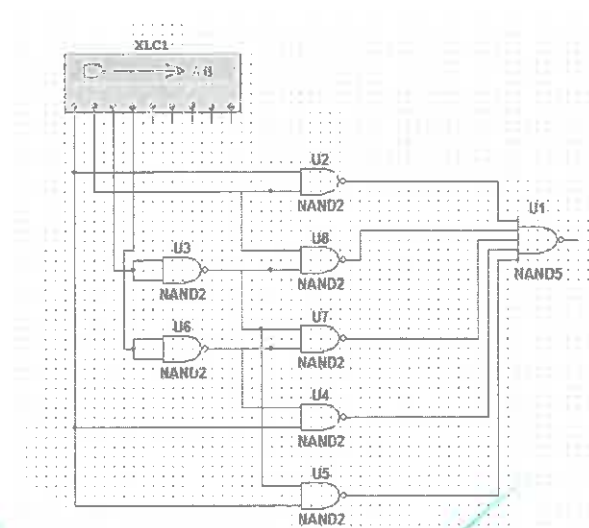
The results obtained matched those of the simulated circuit

(b)

Design a 2-bit comparator whereby the output is HIGH when the one of the two-bit number is equal to or greater than a second two-bit number. Build your comparator and confirm that it operates correctly.

Bit 1		Bit 2		X
A	B	C	D	
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

AB/CD	00	01	11	10
00	1			
01	1	1		
11	1	1	1	1
10	1	1		1



$$X = \overline{C}\overline{D} + A.\overline{D} + A\overline{C} + AB + B\overline{C}$$

$$\overline{X} = \overline{\overline{C}\overline{D} + A.\overline{D} + A\overline{C} + AB + B\overline{C}}$$

$$\overline{X} = (\overline{\overline{C}\overline{D}}) . (\overline{A.\overline{D}}) . (\overline{A\overline{C}}) . (\overline{AB}) . (\overline{B\overline{C}})$$

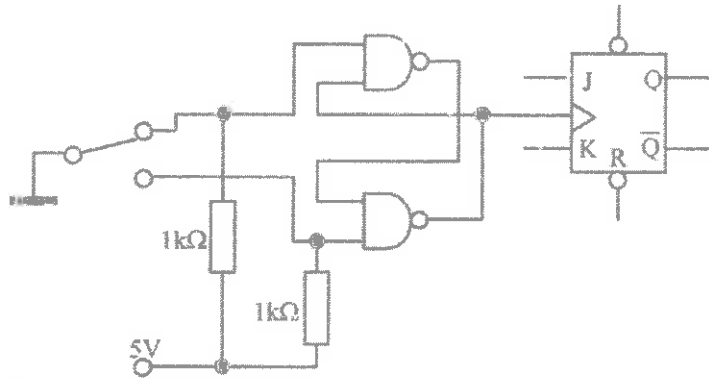
$$X = \overline{(\overline{\overline{C}\overline{D}}) . (\overline{A.\overline{D}}) . (\overline{A\overline{C}}) . (\overline{AB}) . (\overline{B\overline{C}})}$$

The results obtained matched those of the simulated circuit

Part 3 - Sequential Logic

The truth table of the J-K Flip-Flop

- Construct the following circuit on the Logic Tutor, monitoring the clock, Q and $\bar{Q}$ outputs with the on-board LEDs.
- Complete Table 1, entering an x for 'don't care states'.



Inputs					Outputs	
Preset (S)	Clear (R)	Clock	J	K	Q	$\bar{Q}$
0	1	X	X	X	1	0
1	0	X	X	X	0	1
0	0	X	X	X	1	0
1	1		L	L	1	0
1	1		H	L	1	0
1	1		L	H	0	1
1	1		H	H	1	0

- Your observations should enable you to answer the following questions:
 - what is significant about the output state when Preset = Clear = Logic '0'?

This value can be used to test if the JK is functioning correctly

- at what part of the clock pulse is the input data transferred to the device?

Negative edge JK flip-flop triggers on negative edge, transfers data on logic = 0

- at what part of the clock pulse is the output data transferred to the output?

Negative edge

- what clock triggering action does the SN7476 have?

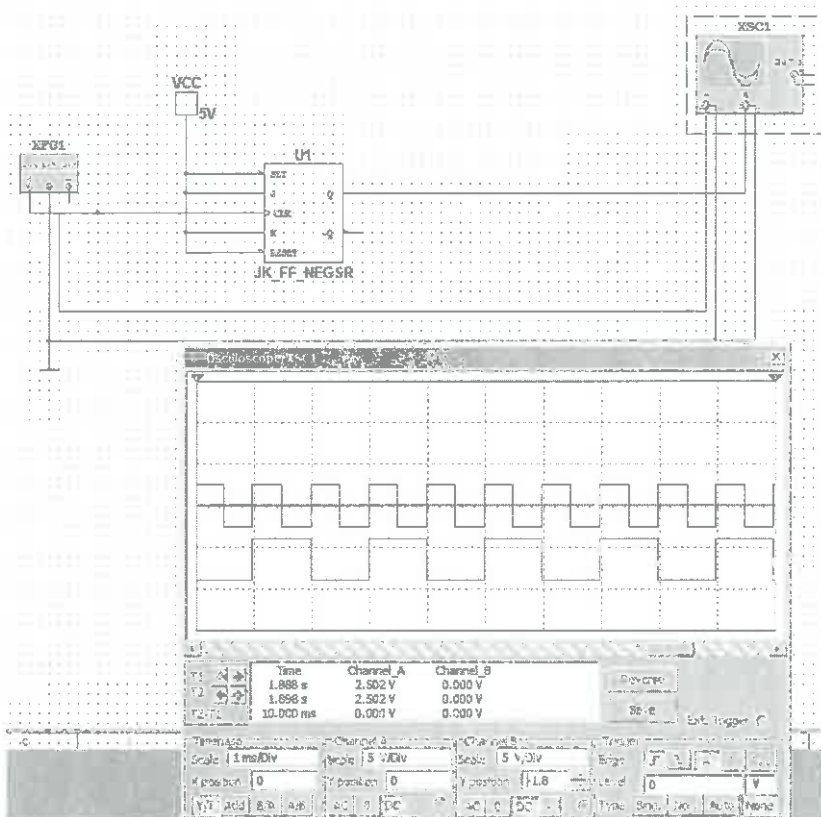
Negative edge

- the cross-coupled NAND gates are for switch debouncing. Why are they needed and how do they work?

Debouncing is necessary because the contacts of switches tend to bounce when connected. This bouncing action causes multiple contacts every time the switch is used, which will register as multiple clock pulses. Debouncing by using a NAND gate solves this by latching the switch's signal for a brief period of time while the switch bounces.

(d) **Frequency division properties of J-K Flip-Flops**

- Replace the existing clock circuit with the TTL output of the signal generator.
- Set the generator to 1kHz and Preset = Clear = J = K = '1'.
- Connect the oscilloscope to both the clock input and Q output and sketch the two observed waveforms above each other on the same time axis.



The waveform shows output Q will toggle when J and K = 1

(e) **Asynchronous Counters**

- Construct the following circuit, with J = K = '1' for both flip-flops.
- Connect the Q outputs to LEDs, and the clock input to the one-shot signal generator on the Logic Tutor.
- Clear the counter and apply successive clock pulses and record the Q outputs in Table 3(a).

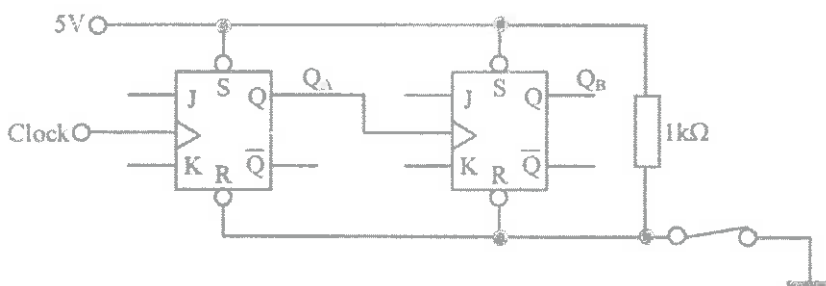
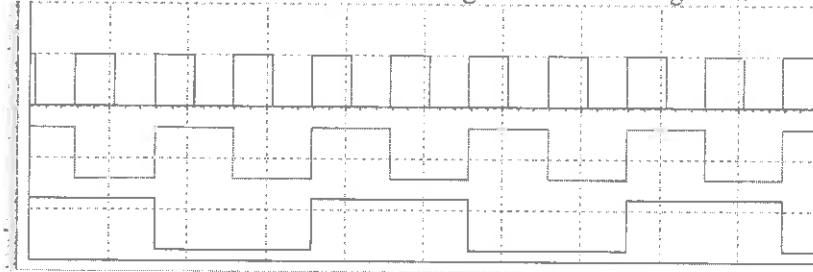


	Table 3(a)		Table 3(b)	
Pulse	QA	QB	QA	QB
Clear	0	0	0	0
1	1	1	1	0
2	0	1	0	1
3	1	0	1	1
4	0	0	0	0
5	1	1	1	0

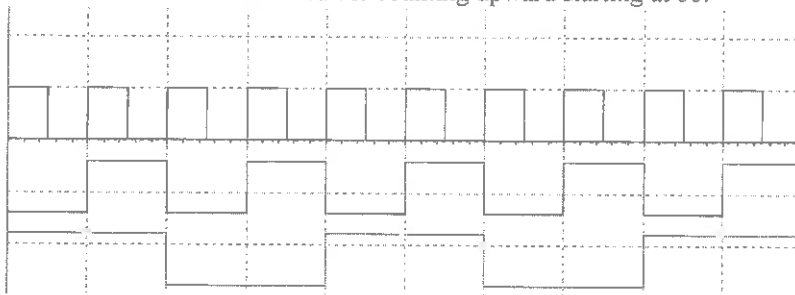
- iv) Now substitute the one-shot clock signal for the low frequency clock on the Logic Tutor and sketch the Clock, QA and QB output waveforms above each other on the same time axis.
- v) Transfer the clock connection from the Q to QBAR output and repeat the above, enter your results in Table 3(b), and sketch the waveforms as before.
- vi) What is the difference between the two circuits?

Should be written in past tense.

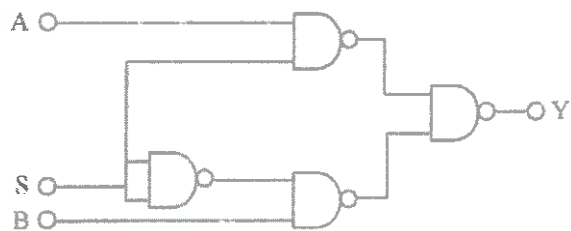
The waveform shows the circuit is counting downward starting at 11.



The waveform shows the circuit is counting upward starting at 00.



(f) *Up / Down Selector*



i) The circuit was constructed for the two input multiplexer circuit shown below.

S=1

a	b	Y
0	0	0
0	1	0
1	0	1
1	1	1

S=0

a	b	Y
0	0	0
0	1	1
1	0	0
1	1	1

When S=1 the circuit will count up, when S=0 the circuit will count down.

Part 4 - Using Sequential Logic to Solve Real Problems

Design and simulate a 3-stage synchronous binary counter that will produce the odd numbers (including zero) in the range 0 to 7.

Excitation table for JK

X = Don't care

Present Q	Next Q	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Part B

Odd numbers 0-7

Present			Next			Input		
Qa	Qb	Qc	Qa	Qb	Qc	Ja Ka	Jb Kb	Jc Kc
0	0	0	0	0	1	0 X	0 X	1 X
0	0	1	0	1	1	0 X	1 X	X 0
0	1	1	1	0	1	1 X	X 1	X 0
1	0	1	1	1	1	X 0	1 X	X 0
1	1	1	0	0	0	X 1	X 1	X 1

QBQC /QA	00	01	11	10
0	0	1	X	X
1	X	X	X	X

$$J_a = Q_c$$

QBQC /QA	00	01	11	10
0	X	X	X	X
1	X	0	1	X

$$K_a = Q_b$$

QBQC /QA	00	01	11	10
0	0	1	X	X
1	X	1	X	X

$$J_b = Q_c$$

QBQC /QA	00	01	11	10
0	X	X	1	X
1	X	X	1	X

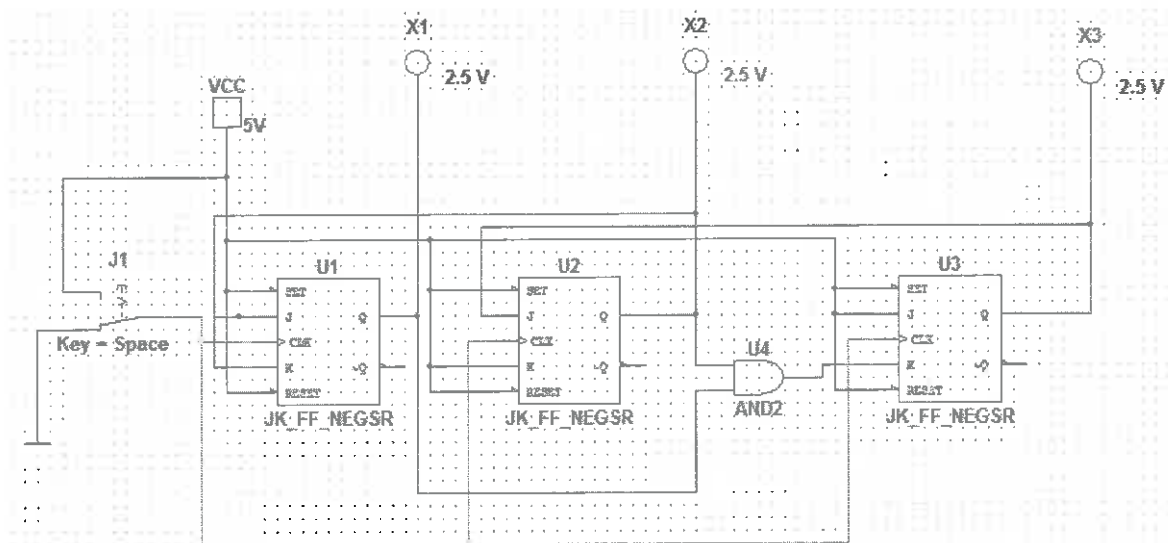
$$K_b = 1$$

QBQC /QA	00	01	11	10
0	1	X	X	X
1	X	X	X	X

$$J_c = 1$$

QBQC /QA	00	01	11	10
0	X	0	0	X
1	X	0	1	X

$$K_c = Q_a \cdot Q_b$$



The circuit was made in Multisim, and its' operation follows the truth table shown above.

Bibliography

Horowitz, P., 2015. *The Art of Electronics*. Cambridge University Press.

R., I., 1988. *Practical Electronics Handbook*. (s.n.).

Unknown, U., 1995. *Principles of Electronics*. (s.n.).

Unknown, U., 2015. *Compare the performance of TTL, CMOS and ECL Logic*.

Available at: <http://www.rfwireless-world.com/Terminology/Difference-between-TTL-ECL-CMOS.html>

You have covered the practical elements
but the comments could have been more
detailed

GUIDANCE FOR STUDENTS IN THE COMPLETION OF TASKS

1. **Research-informed Literature:** You must provide evidence of individual research of the concepts of logic and digital circuits. (10%)
2. **Knowledge and Understanding of Subject:** Must show an understanding of concepts and underlying principles associated with the circuits covered in the assignment. (25%)
3. **Analysis:** Provide analysis of the practical activities. (25%)
4. **Practical Application and Deployment:** Show the ability to perform practical work and be able to verify the operation of the circuits against calculated and theoretical results. (30%)
5. **Skills for Professional Practice:** Your work should be well organised and presented in a professional manner. (10%)

Report Guidance

Your write up should be produced as an engineering report containing the following:

- Front Page
- Summary
- Table of Content
- Introduction & Theory
- Experimental Apparatus and Procedure
- Results and Discussion
- Conclusions - conclude what was discussed in the Results and Discussion section. Think of the conclusion as a short restatement of important points being presented in the report. The conclusion should also make links to the theory discussed earlier in the report.
- References - any direct quotes or images taken from a source material must be referenced using the **Harvard System** in the main body of the report but they should also be listed in a reference section at the end of the report.
- Bibliography - a list of the books or other sources of information that you consulted when writing the report.

MARKING CRITERIA AND STUDENT FEEDBACK

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4. Practical Application and Deployment Deployment of methods, materials, tools and techniques; application of concepts; formulation of innovative and creative solutions to solve problems	30	
5. Skills for Professional Practice Attributes in professional practice: individual and collaborative working; deployment of appropriate media; presentation and organisation	10	

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Up to one weeks late

First Attempt?

%

FdSc & HN COMMON ASSESSMENT AND MARKING CRITERIA

Assessment Criteria	OUTRIGHT FAIL REFER (equivalent to 0-29%)	UNSATISFACTORY REFER (equivalent to 30-39%)	SATISFACTORY PASS (equivalent to 40-49%)	GOOD PASS (equivalent to 50-59%)	VERY GOOD MERIT (equivalent to 60-69%)	EXCELLENT DISTINCTION (equivalent to 70-79%)	EXCEPTIONAL DISTINCTION (equivalent to 80-100%)
1. Research-informed Literature Extent of research and/or own reading, selection of credible sources, application of appropriate referencing conventions	Little or no evidence of reading. Views and findings unsupported and non-authoritative. Referencing conventions largely ignored.	Poor evidence of reading and/or of reliance on inappropriate sources, and/or indiscriminate use of sources. Referencing conventions used inconsistently.	References to a limited range of mostly relevant sources. Some omissions and minor errors. Referencing conventions evident though not always applied consistently.	Inclusion of a range of research-informed literature, including sources retrieved independently. Referencing conventions mostly consistently applied.	Inclusion of a wide range of research-informed literature, including sources retrieved independently. Selection of relevant and credible sources. Very good use of referencing conventions, consistently applied.	A comprehensive range of research-informed literature embedded in the work. Excellent selection of relevant and credible sources. High-level referencing skills, consistently applied.	Outstanding knowledge of research-informed literature embedded in the work. Outstanding selection of relevant and credible sources. High-level referencing skills consistently and professionally applied.
2. Knowledge and Understanding of Subject Extent of knowledge and understanding of concepts and underlying principles associated with the discipline.	Major gaps in knowledge and understanding of material at this level. Substantial inaccuracies.	Gaps in knowledge, with only superficial understanding. Some significant inaccuracies.	Evidence of basic knowledge and understanding of the relevant concepts and underlying principles.	Knowledge is accurate with a good understanding of the field of study.	Knowledge is extensive. Exhibits understanding of the breadth and depth of established views.	Excellent knowledge and understanding of the main concepts and key theories. Clear awareness of challenges to established views and the limitations of the knowledge base.	Highly detailed knowledge and understanding of the main theories/concepts, and a critical awareness of the ambiguities and limitations of knowledge.
3. Analysis Analysis, evaluation and synthesis; logic, argument and judgement; analytical reflection; organisation of ideas and evidence	Unsubstantiated generalisations, made without use of any credible evidence. Lack of logic, leading to unsupported/missing conclusions. Lack of any attempt to analyse, synthesise or evaluate.	Some evidence of analytical intellectual skills, but for the most part descriptive. Ideas/findings sometimes illogical and contradictory. Generalised statements made with scant evidence. Conclusions lack relevance.	Evidence of some logical, analytical thinking and some attempts to synthesise, albeit with some weaknesses. Some evidence to support findings/views, but evidence not consistently interpreted. Some relevant conclusions and recommendations, where relevant	Evidence of some logical, analytical thinking and synthesis. Can analyse new and/or abstract data and situations without guidance. An emerging awareness of different stances and ability to use evidence to support the argument. Valid conclusions and recommendations, where relevant	Sound, logical, analytical thinking; synthesis and evaluation. Ability to devise and sustain persuasive arguments, and to review the reliability, validity & significance of evidence. Ability to communicate ideas and evidence accurately and convincingly. Sound, convincing conclusions / recommendations.	Thoroughly logical work, supported by evaluated evidence. High quality analysis, developed independently or through effective collaboration. Ability to investigate contradictory information and identify reasons for contradictions. Strong, persuasive, conclusions, justifiable recommendations.	Exceptional work; judiciously selected and evaluated evidence. Very high quality analysis, developed independently or through effective collaboration. Ability to investigate contradictory information and identify reasons for contradictions. Highly persuasive conclusions
4. Practical Application and Deployment Effective deployment of appropriate methods, materials, tools and techniques; extent of skill demonstrated in the application of concepts to a variety of processes and/or contexts; formulation of innovative and creative solutions to solve problems.	Limited or no use of methods, materials, tools and/or techniques. Little or no appreciation of the context of the application.	Rudimentary application of methods, materials, tools and/or techniques but without consideration and competence. Flawed appreciation of the context of the application.	An adequate awareness and mostly appropriate application of well-established methods, materials, tools and/or techniques. Basic appreciation of the context of the application.	A good and appropriate application of standard methods, materials, tools and/or techniques. Good appreciation of the context of the application, with some use of examples, where relevant.	A very good application of a range of methods, materials, tools and/or techniques. Very good consideration of the context of the application, with perceptive use of examples, where relevant. Evidence of some innovation and creativity.	An advanced application of a range of methods, materials, tools and/or techniques. The context of the application is well considered, with extensive use of relevant examples. Application and deployment extend beyond established conventions. Innovation and creativity evident throughout.	Outstanding levels of application and deployment skills. Assimilation and development of cutting edge processes and techniques.
5. Skills for Professional Practice Demonstrates attributes expected in professional practice including: individual initiative and collaborative working; deployment of appropriate media to communicate (including written and oral); clarity and effectiveness in presentation and organisation.	Communication media is inappropriate or misapplied. Little or no evidence of autonomy in the completion of tasks. Work is poorly structured and/or largely incoherent.	Media is poorly designed and/or not suitable for the audience. Poor independent or collaborative initiative. Work lacks structure, organisation, and/or coherence	Can communicate in a suitable format but with some room for improvement. Can work as part of a team, but with limited involvement in group activities. Work lacks coherence in places and could be better structured.	Can communicate effectively in a suitable format, but may have minor errors. Can work effectively as part of a team, with clear contribution to group activities. Mostly coherent work and is in a suitable structure.	Can communicate well, confidently and consistently in a suitable format. Can work very well as part of a team, with very good contribution to group activities. Work is coherent and fluent and is well structured and organised.	Can communicate professionally and, confidently in a suitable format. Can work professionally within a team, showing leadership skills as appropriate, managing conflict and meeting obligations. Work is coherent, very fluent and is presented professionally.	Can communicate with an exceptionally high level of professionalism. Can work exceptionally well and professionally within a team, showing advanced leadership skills. Work is exceptionally coherent, very fluent and is presented professionally.



Prifysgol Cymru
Y Drindod Dewi Sant
University of Wales
Trinity Saint David

Cyfadran Dylunio Cymhwysol a Pheirianeg
Faculty of Applied Design and Engineering

Taflen Cyflwyno Aseiniad Assignment Hand in Sheet

MANYLION Y MYFYRIWR STUDENT'S DETAILS			
ENW: NAME:		RHIF P Y MYFYRIWR: STUDENT P NUMBER:	P
CWRS: COURSE:	HND Electrical/Electronic Engineering	LEFEL Y CWRS: LEVEL OF COURSE:	4
MODIWL: MODULE:	PSDE 4004 - Electronic 1		
TEITL YR ASEINIAD: ASSIGNMENT TITLE:	Digital Circuits		
DARLITHIWR/WYR: LECTURER/S:	Jason Pointer	DYDDIAD: DATE:	
Staff Llyfrgell YN UNIG / Library Staff ONLY			
Derbynwyd gan / Accepted by: _____ Dyddiad Cyflwyno: Date Submitted: _____ Amsod / Time: _____			

DERBYNNEB / RECEIPT			
ENW / NAME:		RHIF P Y MYFYRIWR: STUDENT P NUMBER:	P
CWRS / COURSE:	HND Electrical/Electronic Engineering	LEFEL Y CWRS: LEVEL OF COURSE:	4
MODIWL / MODULE:	PSDE 4004 - Electronic 1		
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