



Complete, fold and seal
(see note 2 below)

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Examination Answer Books

12 Pages

Instructions to Candidates

1. Please give the information requested in the boxes.
2. Enter your name in the space provided to the right, fold over and seal down (using the label provided) to hide your name.
3. The answers must be legibly written. The Examiners cannot read illegible script or have it typed and the expense of typing charged to the candidate.
4. Write your answers in ink.
5. Begin each answer on a fresh page. Do all rough work in the answer book and cross it through.
6. No part of this book is to be torn out; it must be handed in complete.
7. If more books than one are used, fasten them together using the tags available from the invigilator(s).
8. Every book must be handed in. In no circumstances may answer books, used or unused, be taken out of the examination venue.

1	Student Number	2308342
2	Title of Examination Paper	MICROS PERIPHERALS and INTERFACES
3	Module Code	ACDA4004
4	Date and Time of Examination	09:00 08/01/2025
5	Examination Venue	310
6	Seat Number	023
7	Number of Answer Books handed in	

List the numbers of the questions you have attempted	Office Use
Q1	5 1/2
Q2	5
Q3	3
Q5	10
Q4	0
Q6	4 1/2
	28
	x 2
Total	56%

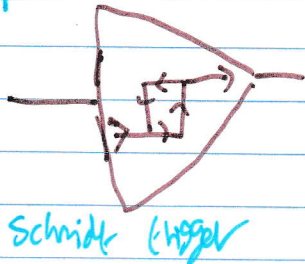
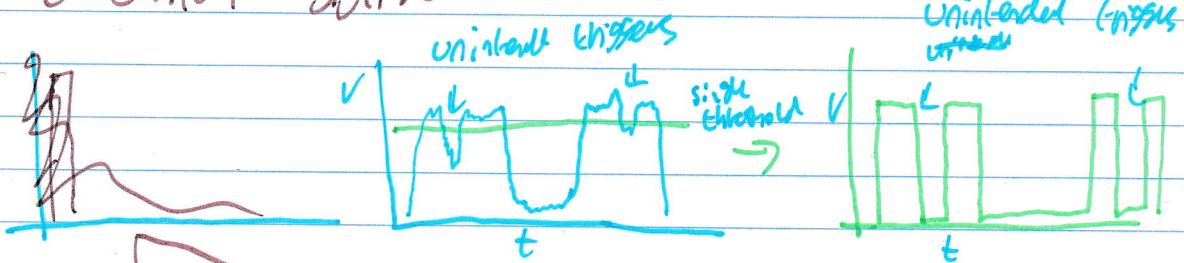
5 1/2
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4 1/2

28

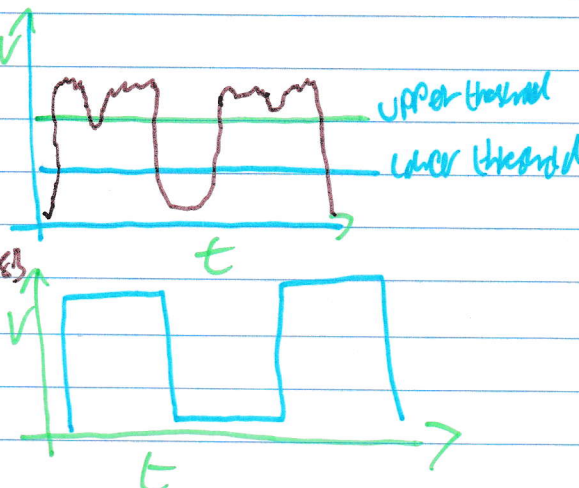
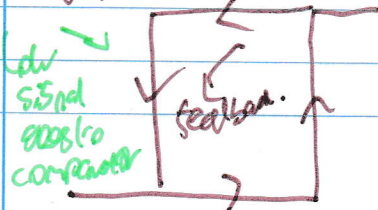
- Q1) ~~RETURN~~ RETURN $\rightarrow$ Return from Subroutine
 BRMS Program back to main stack from esp previous Subroutine $1\frac{1}{2}$ $1\frac{1}{2}$
- b) SLEEP $\rightarrow$ Enters Standby mode
 WDT Watchdog timer and oscillator paused, CPU set to sleep $1\frac{1}{2}$ $1\frac{1}{2}$
- c) ADDLW $\rightarrow$ ~~perform~~ Add W to (W) Literal.
 Add the contents of the Literal (R) and the W register. $1\frac{1}{2}$ $1\frac{1}{2}$
- d) BCF $\rightarrow$ Bit Check f register $\times$
 Check the contents of the f register if result bit b=0 stored in the W register if 1 stored in f register $\times$
- e) DECF Decrement F
 Decrement the contents of the f register, if 0 stored in W register if 1 stored in the f register. 1

2) Hardware: 1 Schmidt trigger -

A smick trigger essentially has two Voltage thresholds and the circuit is a feedback loop that checks that both of these have been triggered before sending the Switch signal.



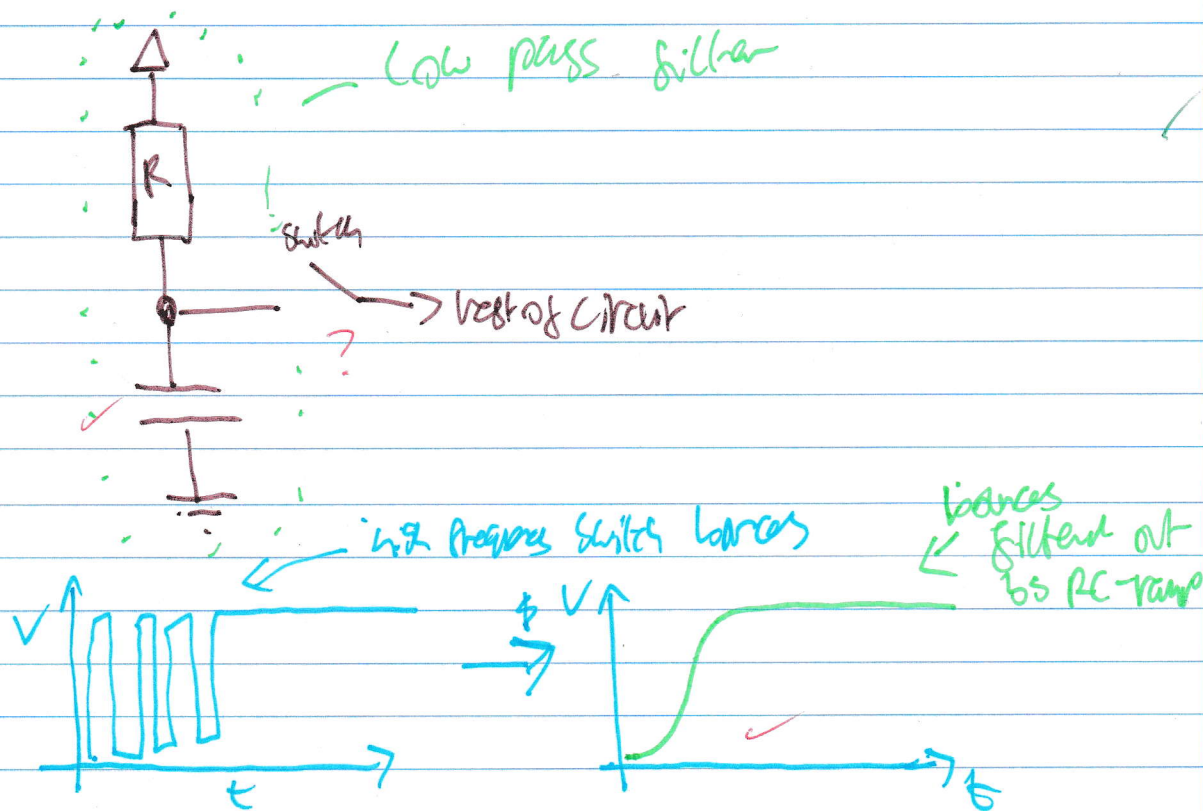
Writes on the hysteresis curve



When both threshold conditions are met, Switch coil is sent, prevents unintended triggers when switch has been nullified.

2) Hardware 2: RC-Low pass filter

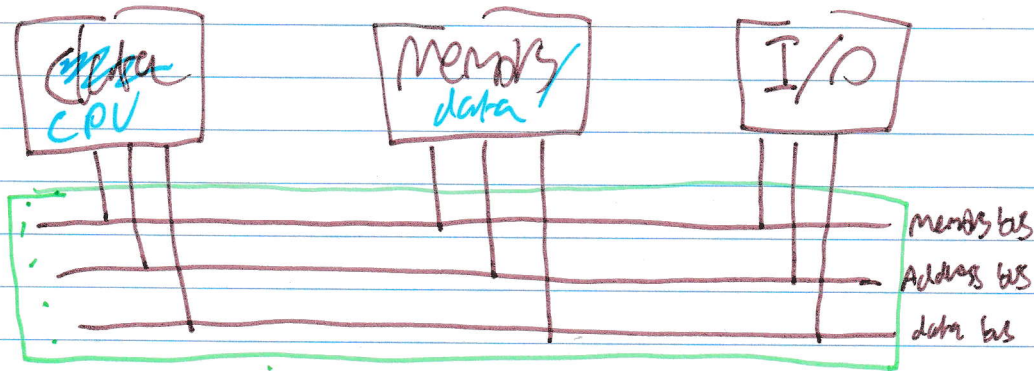
- By attaching a resistor from power and a capacitor to ground with the switch in the middle, the high frequency bounces are removed for a smoothed RC-ramp up or down depending on logic



3) AND = $A \cdot B$ (also D)

A	B	$A \cdot B$
0	0	0
1	0	0
0	1	0
1	1	1

Q5 Von Neumann processor



'share' bus for all components

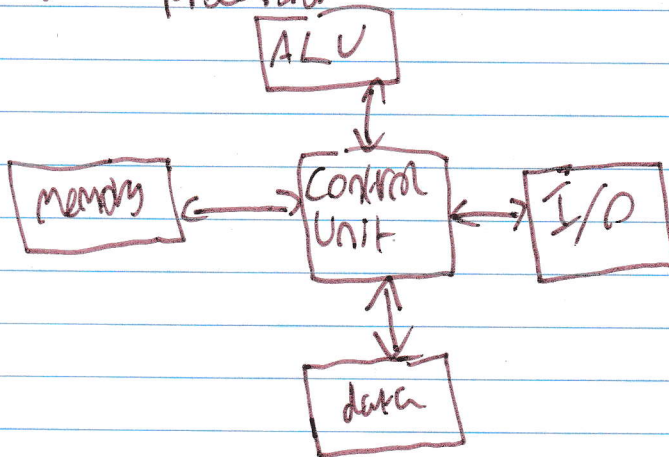
Von Neumann have

- Single memory for data feed
- Single address bus for fetch/read/write
- Serialised processes

Advantages:

- Hardware requirements are less complex than for Harvard
- More generalist machines

Harvard processor



- Independent buses for ALU/Memory/data/Input output
- Allows parallel processing of tasks
- More complex hardware requirements
- Can execute fetch instructions and read/write simultaneously

Advantage :

parallel processing can conduct simultaneous data processes (allows for independent buses).

$$Q = ((\text{NOT } A) \text{ XOR } (B \text{ NOR } C)) \text{ AND } (B \text{ NOR } C)$$

Question No.

Examiner Only

Q4)

~~| A | $\bar{A}$ |
|---|-----------|
| 0 | 1 |
| 1 | 0 |~~

A	$\bar{A}$
0	1
1	0

XOR =

A	B	A XOR B
0	0	0
1	0	1
0	1	1
1	1	0

NOR =

A	B	A NOR B
0	0	1
1	0	0
0	1	0
1	1	0

~~A~~

~~A~~ ~~A~~ B C

XOR =

A	B	A XOR B
0	0	0
1	0	1
0	1	1
1	1	0

A	B	C	$\bar{A}$	$\bar{B}$	$\bar{C}$	B NOR C
0	0	0	1	1	1	1
1	0	0	0	1	1	0
0	1	0	1	0	1	0
1	1	0	0	0	1	0
0	0	1	1	1	0	0
1	0	1	0	1	0	0
0	1	1	1	0	0	0
1	1	1	0	0	0	0

before And

A ((NOT A) XOR (B NOR C))

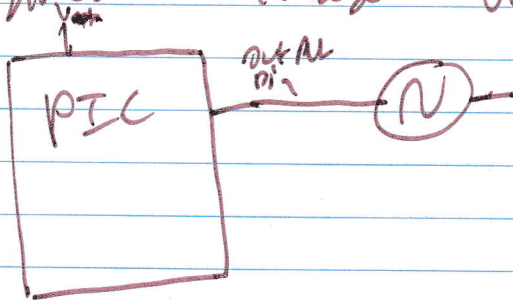
A	$\bar{A}$	B	C	B NOR C	$\bar{A}$ XOR B NOR C	$(\bar{A} \text{ XOR } (B \text{ NOR } C)) \text{ AND } C$
0	1	0	0	1	0	0
1	0	1	0	0	0	0
0	1	0	1	0	1	1
1	0	1	1	0	0	0
0	1	1	0	0	1	0
1	0	1	1	0	0	0

b) simpler solution is an exclusive Nor OR gate

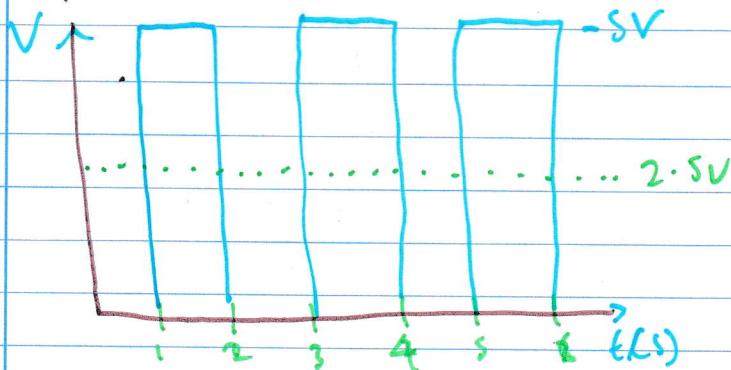
DAC

Q6) Using a single pin?

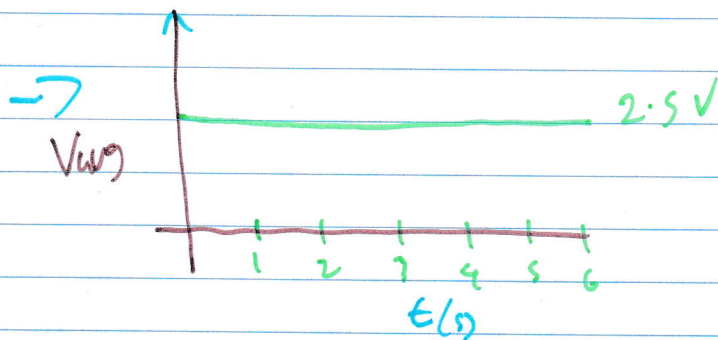
You will have to vary the duty cycle of the output PWM signal to simulate a required analogue voltage. ✓



Need to drive analogue voltage of say 2.5V
pic output maximum voltage is 5V in this example



by ~~output~~ then modulating the width of the output pulses the average voltage across time put out is 2.5V. ✓



By varying the pulses that is pulse width modulation you can output an analogue voltage between the maximum output and zero.