

LEVEL 4 ASSESSMENT SPECIFICATION

Student name:	Camron Thomas	Student ID number:	
Programme:	HNC Electrical/Electronic Engineering		
Module:	Electronics		
Module code:	PCEE4006	Contribution to Overall Module Assessment (%):	50%
Lecturer:	Jason Pointer	Internal Verifier:	Nigel Richards
Assignment Title:	Digital Systems	Word count (or equivalent):	2000
Submission deadline:	11/05/23	Return date of provisional marks & written feedback:	25/05/23
Submission method:	All written assessments, where practical and possible, must be submitted via Turnitin unless otherwise instructed by the Lecturer. (Please DO NOT put this assessment specification into Turnitin or it will match many similarities with other students' submissions.) Alternative submission method (if applicable): Late submission of the assessment will result in a late penalty mark. Penalties for late submission: Up to one week late, maximum mark of 40%. Over one week late, 0%. Only the Extenuating Circumstances Panel may approve a change to submission dates.		
Academic honesty / referencing:	Academic honesty is required. In the main body of your submission you must give credit to authors on whose research and ideas your work is based. Append to your submission a reference list that indicates the books, articles, etc. that you have used, cited or quoted in order to complete this assessment.		

Module Learning Outcomes (from module syllabus)

1. Demonstrate an understanding of semi-conductor components and characteristics and their application in analogue and **digital** electronic circuits.
2. To design, simulate, build, test and evaluate analogue and **digital** electronic circuits using information gained from datasheets.

STUDENT FEEDBACK FORM

This section details the *extent* to which the assessment criteria are demonstrated by you, which in turn determines your mark. The marks available for each category of skill are shown. Lecturers will use the space provided to comment on the achievement of the task(s), including those areas in which you have performed well and areas that would benefit from development/improvement.

Generic Assessment Criteria	Marks available	Marks awarded
1. Engagement with Literature Skills	10	5.5
Engagement with a good range of literature sources but could include some text books. Generally sound referencing, with very few inaccuracies.		
2. Knowledge and Understanding Skills	45	31.5
Task 1 & 2 achieved 68%. Task 3 & 4 achieved 72%. Excellent knowledge and understanding of the basic underlying concepts and principles of digital systems. Showed excellent understanding the logic gates, Boolean algebra, Karnaugh maps and counter design work.		
3. Cognitive and Intellectual Skills	10	4.7
Some evidence to support emerging arguments and judgements but in some places they are underdeveloped.		
4. Practical Application Skills	25	19.6
Task 1 & 2 achieved 80%. Task 3 & 4 achieved 77%. An excellent application of practical work for all tasks, very good use of the test equipment and Multisim to obtain the required test results.		
5. Transferable Skills for Life and Professional Practice	10	6.5
Work is accurate, coherent, fluent, well-structured and organised.		

Assessment Mark (Assessment marks are subject to ratification at the Exam Board. These comments and marks are to give feedback on module work and are for guidance only until they are confirmed.)	Late Submission Penalties (tick if appropriate)		68%
	Up to 1 week late (40% Max)		
	Over 1 week late (0%)		

Pembrokeshire College

Electronics Assignment 2

2023

Camron Thomas

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TASK DESCRIPTION

Task 1 - Combinational Logic

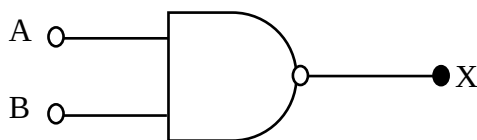
Using Multisim construct and test the following circuits. For each circuit complete a truth table and measure the logic value at each point indicated in the truth table. Write down the simplified Boolean expression and check that the measured values agree with the expected values.

Introduction Task 1

In this task there are a series of combinational logic circuits, these types of circuits are often made up from basic logic NOR, NAND and NOT gates. For each section of this task a truth table and Boolean expression are required. When the gates stated above are combined, they produce much more challenging circuits. 'As combinational logic circuits are made up from individual logic gates only, they can also be considered as "decision making circuits" and combinational logic is about combining logic gates together to process two or more signals in order to produce at least one output signal according to the logical function of each logic gate.'

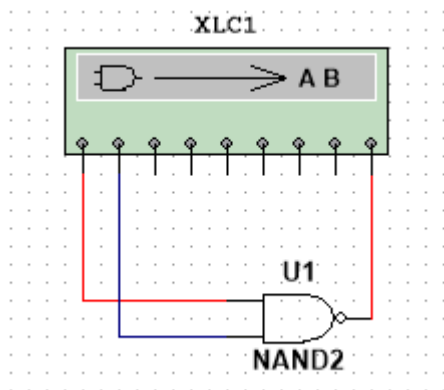
(Tutorials, 2021)

(a)



A	B	X
0	0	1
0	1	1
1	0	1
1	1	0

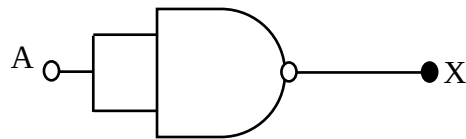
$$X = \overline{A \cdot B}$$



A screenshot of the Multisim logic converter interface. It displays a truth table with columns A, B, C, D, E, F, G, H and rows 000, 001, 002, 003. The output column shows values 1, 1, 1, 0. To the right, there is a 'Conversions' section with various logic gate symbols and their corresponding Boolean expressions. The output expression is shown as $(AB)'$.

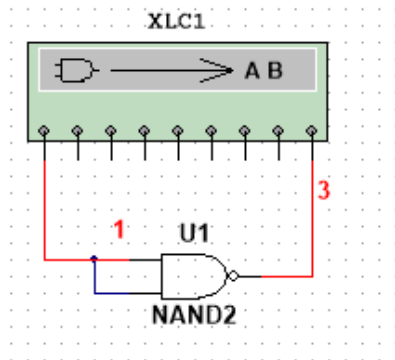
The screenshots above show that the Boolean Expression and Truth Table measured values and expected values are both correct.

(b)



A	X
0	1
1	0

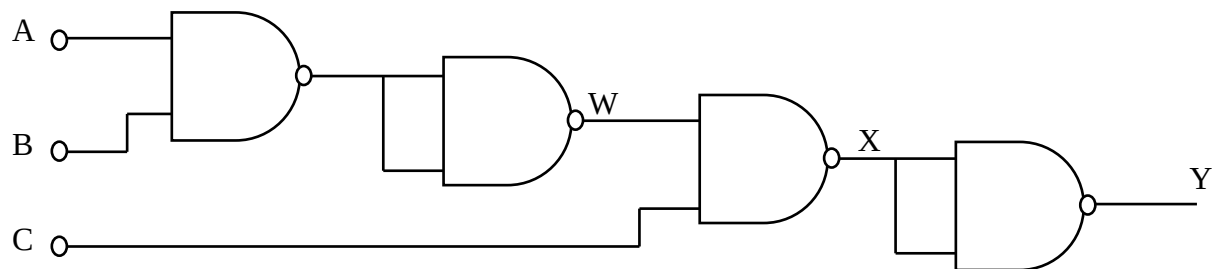
$$X = \bar{A}$$



	A	B	C	D	E	F	G	H	
000	0								1
001	1								0

The screenshots above show that the Boolean Expression and Truth Table measured values and expected values are both correct. ✓

(c)

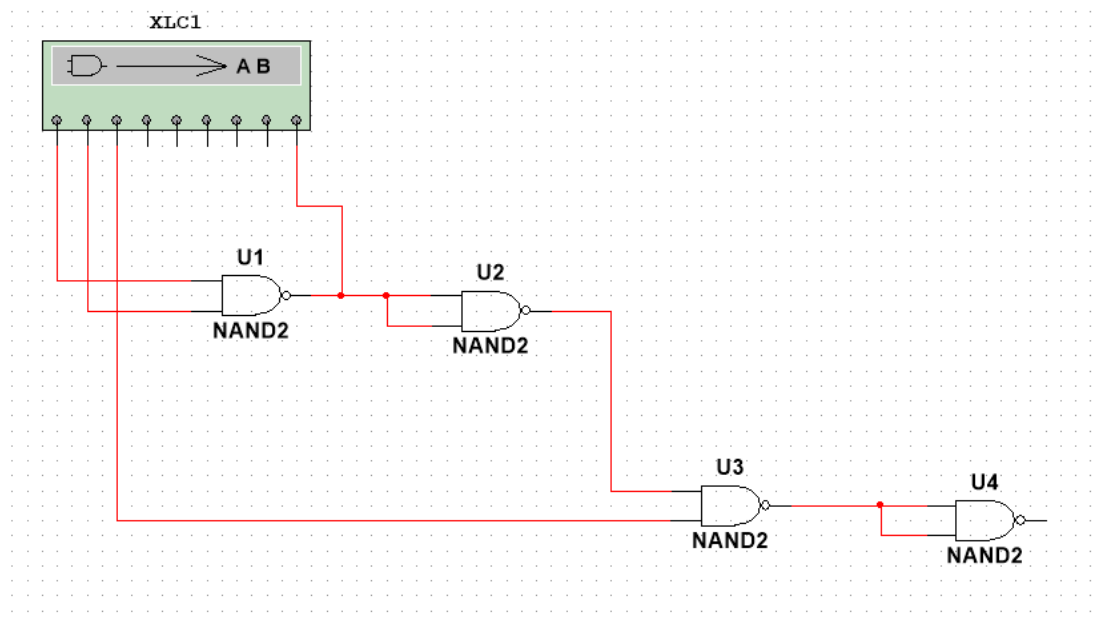


Truth table for Part C

A	B	C	W	X	Y
0	0	0	0	1	0
0	0	1	0	1	0
0	1	0	0	1	0
0	1	1	0	1	0
1	0	0	0	1	0
1	0	1	0	1	0
1	1	0	1	1	0
1	1	1	1	0	1

State the logic function for W, X and Y and simplify.

- W



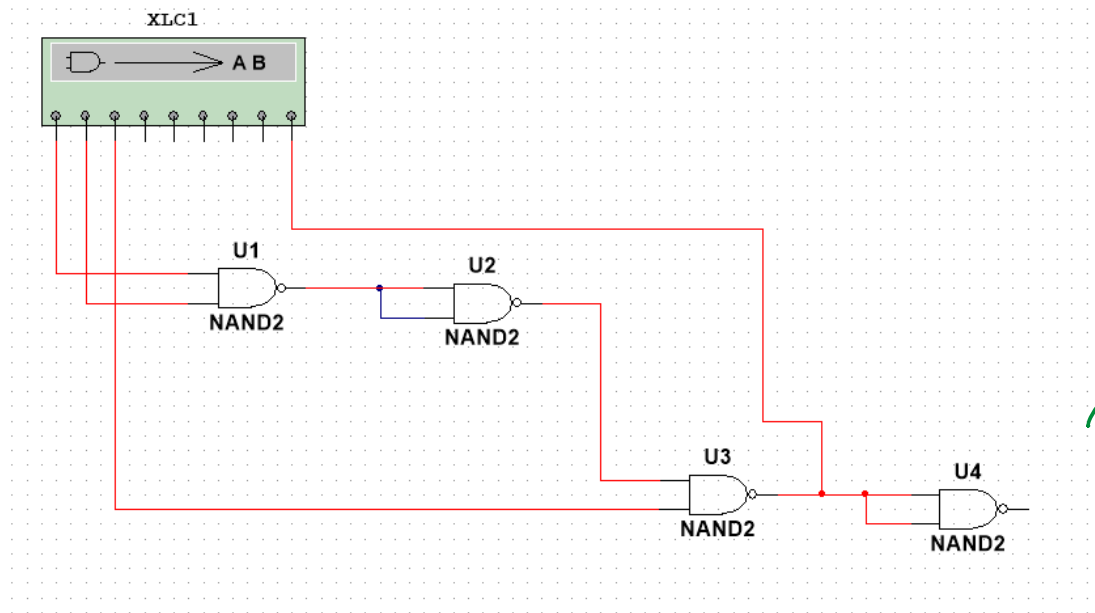
	A	B	C	D	E	F	G	H	Out
000	0	0	0						0
001	0	0	1						0
002	0	1	0						0
003	0	1	1						0
004	1	0	0						0
005	1	0	1						0
006	1	1	0						1
007	1	1	1						1

Simplified Boolean Expression:

$$W = A \cdot B$$

The logic function for this circuit would be a Two Input AND gate.

- X



	A	B	C	D	E	F	G	H	Out
000	0	0	0						1
001	0	0	1						1
002	0	1	0						1
003	0	1	1						1
004	1	0	0						1
005	1	0	1						1
006	1	1	0						1
007	1	1	1						0

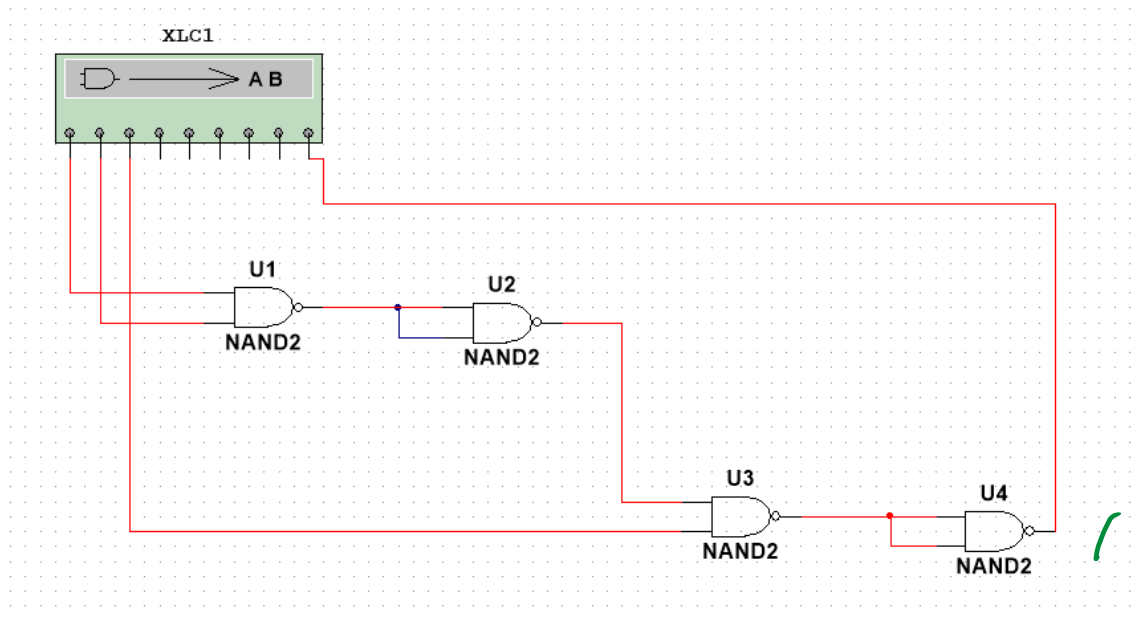
A' + B' + C'									
--------------	--	--	--	--	--	--	--	--	--

Simplified Boolean Expression:

$$X = \overline{A.B.C}$$

The logic function for this circuit would be a Three Input NAND Gate.

- Y



	A	B	C	D	E	F	G	H	Out
000	0	0	0						0
001	0	0	1						0
002	0	1	0						0
003	0	1	1						0
004	1	0	0						0
005	1	0	1						0
006	1	1	0						0
007	1	1	1						1

Conversions

- $\Rightarrow$ $\rightarrow \overline{101}$
- $\overline{101} \rightarrow A|B$
- $\overline{101} \xrightarrow{\text{SIMP}} A|B$
- $A|B \rightarrow \overline{101}$
- $A|B \rightarrow \Rightarrow$
- $A|B \rightarrow \text{NAND}$

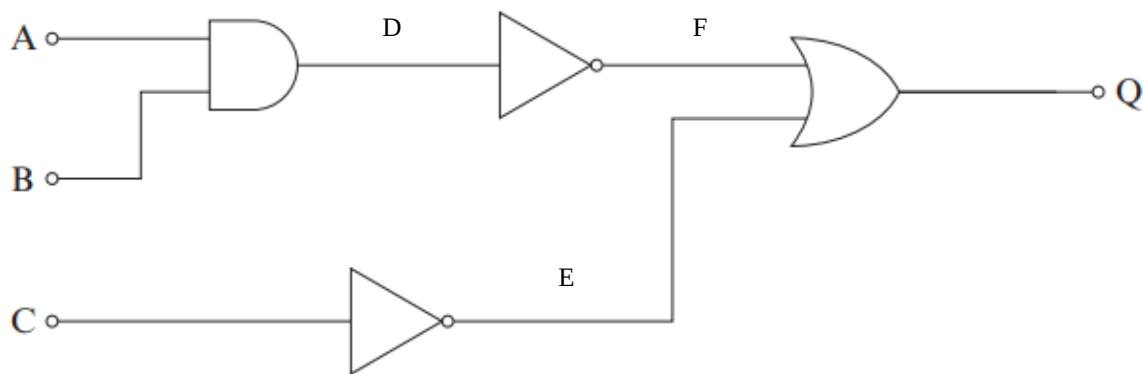
ABC

Simplified Boolean Expression:

$$Y = A \cdot B \cdot C$$

The logic function for this circuit would be a Three Input AND Gate.

(d) Produce the truth table and Boolean expression for the circuit shown below.



Truth table:

A	B	C	D	E	F	Q
0	0	0	0	1	1	1
0	0	1	0	0	1	1
0	1	0	0	1	1	1
0	1	1	0	0	1	1
1	0	0	0	1	1	1
1	0	1	0	0	1	1
1	1	0	1	1	0	1
1	1	1	1	0	0	0

Boolean Expression:

$$Q = \bar{A}.\bar{B}.\bar{C} + \bar{A}.\bar{B}.C + \bar{A}.B.\bar{C} + \bar{A}.B.C + A.\bar{B}.\bar{C} + A.\bar{B}.C + A.B.\bar{C}$$

Karnaugh Map:

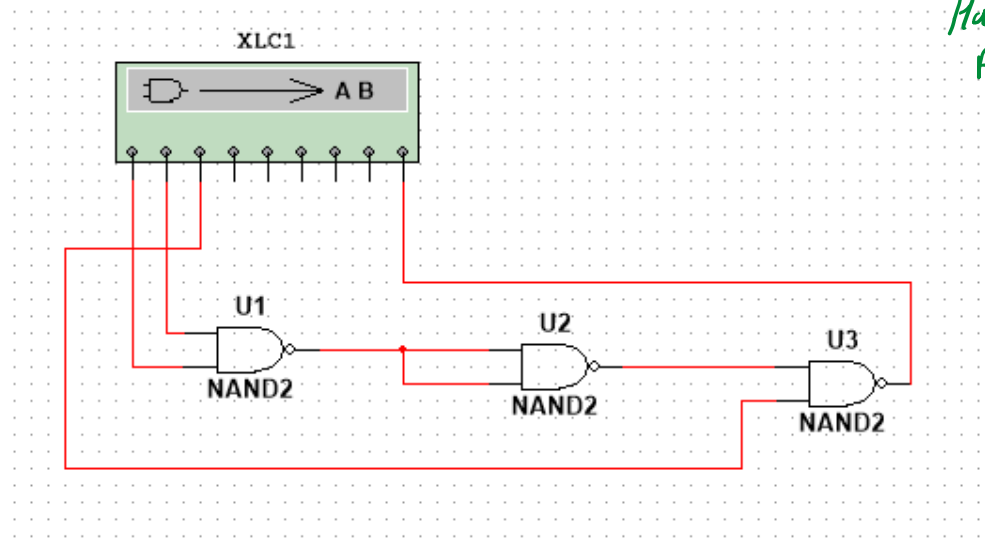
		BC			
A		00	01	11	10
	0	1	1	1	1
	1	1	1	0	1

As seen in the Karnaugh map above there are four groups, 3x groups of 4 and 1x group of 2.

Simplified Boolean Expression:

$$Q = \bar{A}.\bar{B}.\bar{C} \text{ or } Q = \bar{A} + \bar{B} + \bar{C}$$

Draw the NAND gate equivalent circuit for the circuit shown above using only 2-input NAND gates, show how it can be simplified and use Multisim to confirm its results.



Have not drawn the full circuit.

	A	B	C	D	E	F	G	H
000	0	0	0					1
001	0	0	1					1
002	0	1	0					1
003	0	1	1					1
004	1	0	0					1
005	1	0	1					1
006	1	1	0					1
007	1	1	1					0

Conversions			
$\overline{A} \overline{B}$	$\rightarrow$	$\overline{A \cdot B}$	
$\overline{A \cdot B}$	$\rightarrow$	$A \cdot B$	
$\overline{A \cdot B}$	$\xrightarrow{\text{SIMP}}$	$A \cdot B$	
$A \cdot B$	$\rightarrow$	$\overline{A \cdot B}$	
$A \cdot B$	$\rightarrow$	$\overline{A} \overline{B}$	
$A \cdot B$	$\rightarrow$	NAND	

$A' + B' + C'$

Explain the benefit of using the NAND gate equivalent circuit.

‘The popularity of the NAND gate is derived from the fact that it is the easiest of the digital logical operators to implement using transistor technology’ (Devices, 2023)

Benefits of NAND gates

- NAND gates are cost-effective devices, and they have more storage capacities as per their size.
- This gate offers good replaceability which means that when the flash memory gets damaged, then it can be replaced with a suitable component.
- The memory ability of NAND can substitute huge files like USB drives, digital cameras, and tablets.
- High endurance and durability.

(WatElectronics, 2022)

You have not discussed why you would use NAND gate circuits.

- (e) Simplify the following Boolean equations, ONLY using the LAWS OF BOOLEAN ALGEBRA and DeMORGANS THEOREM. Verify your findings by using Multisim constructing the logic circuits using NAND gates.

i) $Q = (A+B)(A + \bar{B})(\bar{A} + C)$

Boolean Algebra

$$Q = (A.A + A.\bar{B} + B.A + B.\bar{B})(\bar{A} + C) \quad \checkmark$$

$$Q = (A + A.\bar{B} + A.B)(\bar{A} + C)$$

$$Q = A.(1 + \bar{B} + B)(\bar{A} + C) \quad \checkmark$$

$$Q = A.1.(\bar{A} + C) \quad \checkmark$$

$$Q = A.(\bar{A} + C)$$

$$Q = A.\bar{A} + A.C \quad \checkmark$$

$$Q = A.C \quad \checkmark$$

	A	B	C	D	E	F	G	H	Out
000	0	0	0						0
001	0	0	1						0
002	0	1	0						0
003	0	1	1						0
004	1	0	0						0
005	1	0	1						1
006	1	1	0						0
007	1	1	1						1

Conversions

$\Rightarrow \rightarrow \overline{10|1}$

$\overline{10|1} \rightarrow A|B$

$\overline{10|1} \rightarrow \overline{10|1} A|B$

$A|B \rightarrow \overline{10|1}$

$A|B \rightarrow \Rightarrow$

$A|B \rightarrow \text{NAND}$

$(A+B)(A+\bar{B})(\bar{A}+C)$

	A	B	C	D	E	F	G	H	Out
000	0	0	0						0
001	0	0	1						0
002	0	1	0						0
003	0	1	1						0
004	1	0	0						0
005	1	0	1						1
006	1	1	0						0
007	1	1	1						1

Conversions

$\Rightarrow \rightarrow \overline{10|1}$

$\overline{10|1} \rightarrow A|B$

$\overline{10|1} \rightarrow \overline{10|1} A|B$

$A|B \rightarrow \overline{10|1}$

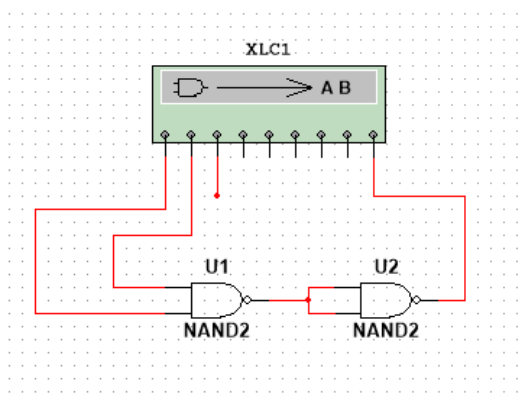
$A|B \rightarrow \Rightarrow$

$A|B \rightarrow \text{NAND}$

AC

The two images above show the Boolean Equation converted into a truth table and the simplified version of the equation. The simplified value on Multisim corresponds with the calculated results proving it is correct. ✓

Use DeMORGANS Theory to turn it into NAND Gates:



The above circuit shows the NAND gate equivalent. ✓

$$\text{ii) } Q = A.B.\bar{C} + A.\bar{C} + \bar{A}.\bar{C}.D + \bar{A}.\bar{C}.\bar{D}$$

Boolean Algebra:

$$Q = \bar{C}.(A.B + A + \bar{A}.D + \bar{A}.\bar{D})$$

$$Q = \bar{C}.(A.(B + 1) + \bar{A}.(D + \bar{D}))$$

$$Q = \bar{C}.(A + \bar{A})$$

$$Q = \bar{C}$$

	A	B	C	D	E	F	G	H	Out
000	0	0	0	0					1
001	0	0	0	1					1
002	0	0	1	0					0
003	0	0	1	1					0
004	0	1	0	0					1
005	0	1	0	1					1
006	0	1	1	0					0
007	0	1	1	1					1
008	1	0	0	0					1
009	1	0	0	1					1
010	1	0	1	0					0
011	1	0	1	1					0
012	1	1	0	0					1
013	1	1	0	1					1

ABC' + AC' + A'CD + A'CD'

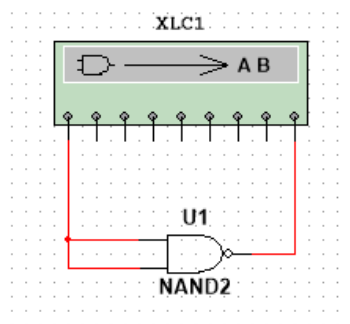
C'

	A	B	C	D	E	F	G	H	Out
000	0	0	0	0					1
001	0	0	0	1					1
002	0	0	1	0					0
003	0	0	1	1					0
004	0	1	0	0					1
005	0	1	0	1					1
006	0	1	1	0					0
007	0	1	1	1					1
008	1	0	0	0					1
009	1	0	0	1					1
010	1	0	1	0					0
011	1	0	1	1					0
012	1	1	0	0					1
013	1	1	0	1					1

C'

The two images above show the Boolean Equation converted into a truth table and the simplified version of the equation. The simplified value on Multisim corresponds with the calculated results proving it is correct.

Use DeMORGANS Theory to turn it into NAND Gates:



The above circuit shows the NAND gate equivalent.

- (f) Binary Coded Decimal (BCD) is a 4-bit binary code with the range of numbers 1010 to 1111 not used. Design a circuit that will detect these invalid codes. Construct the circuit and verify that it performs the required task.

Truth table for Binary Code:

A	B	C	D	Q
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0

0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

BOTTOM SIX IS INVALID CODE

Boolean expression:

$$Q = A.\bar{B}.C.\bar{D} + A.\bar{B}.C.D + A.B.\bar{C}.\bar{D} + A.B.\bar{C}.D + A.B.C.\bar{D} + A.B.C.D$$

Karnaugh Map:

CD \ AB	00	01	11	10
00				
01				
11	1	1	1	1
10			1	1

In the Karnaugh Map above there are two groups of four.

$$Q = A.B + A.C$$

$$Q = A.B + A.C$$

DeMORGANS Theorem:

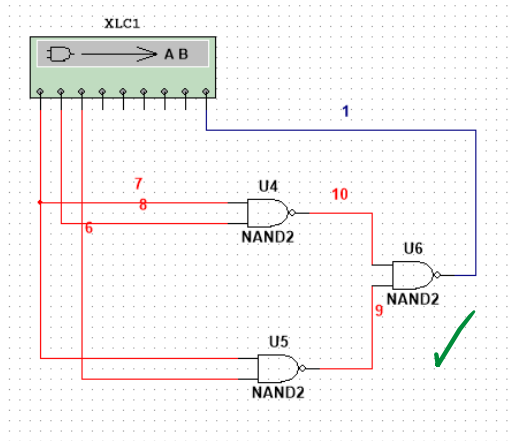
$$Q = A.B + A.C$$

$$\bar{Q} = \overline{A.B + A.C}$$

$$\bar{Q} = \overline{A.B.A.C}$$

$$Q = \overline{A.B.A.C}$$

Nand Gate Equivalent:



☐
☐
☐
☒
☐
☐
☐
☐

Out ☐

	A	B	C	D	E	F	G	H	
000	0	0	0						0
001	0	0	1						0
002	0	1	0						0
003	0	1	1						0
004	1	0	0						0
005	1	0	1						1
006	1	1	0						1
007	1	1	1						1

Conversions

→
 $\overline{A \cdot B}$

$\overline{A \cdot B}$
→
 $A \vee B$

$\overline{A \cdot B}$
 $\xrightarrow{\text{SIMP}}$
 $A \vee B$

$A \vee B$
→
 $\overline{A \cdot B}$

$A \vee B$
→

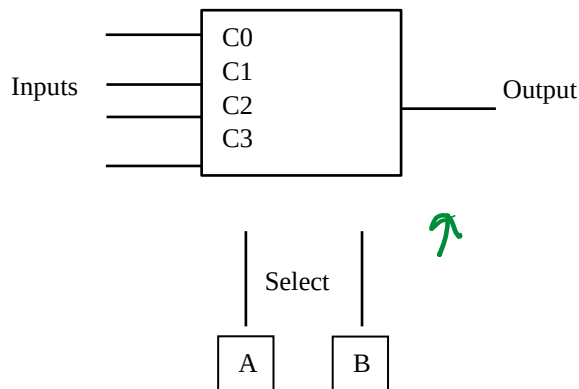
$A \vee B$
→
NAND

$AB + AC$

Well done.

Task 2 - Multiplexer

An arrangement where several inputs can be connected but only one input, under the influence of a select input, will have access to the output. The block diagram below shows a 4-to-1 multiplexer, produce a truth table and the Boolean equation to representation the multiplexer. Use this information to design the 4-to-1 multiplexer using logic gates and test its function using Multisim.



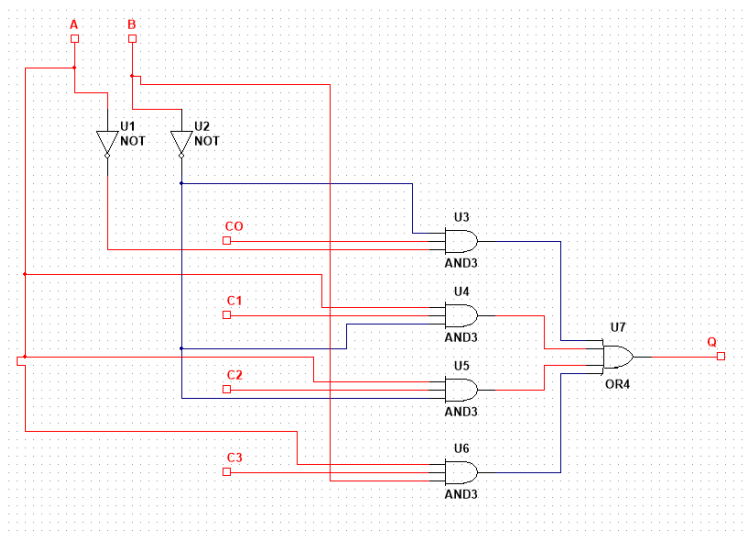
Truth Table for Multiplexer:

Input	Selector switch (A)	Selector Switch (B)	Output (Q)
C ₀	0	0	C ₀
C ₁	0	1	C ₁
C ₂	1	0	C ₂
C ₃	1	1	C ₃

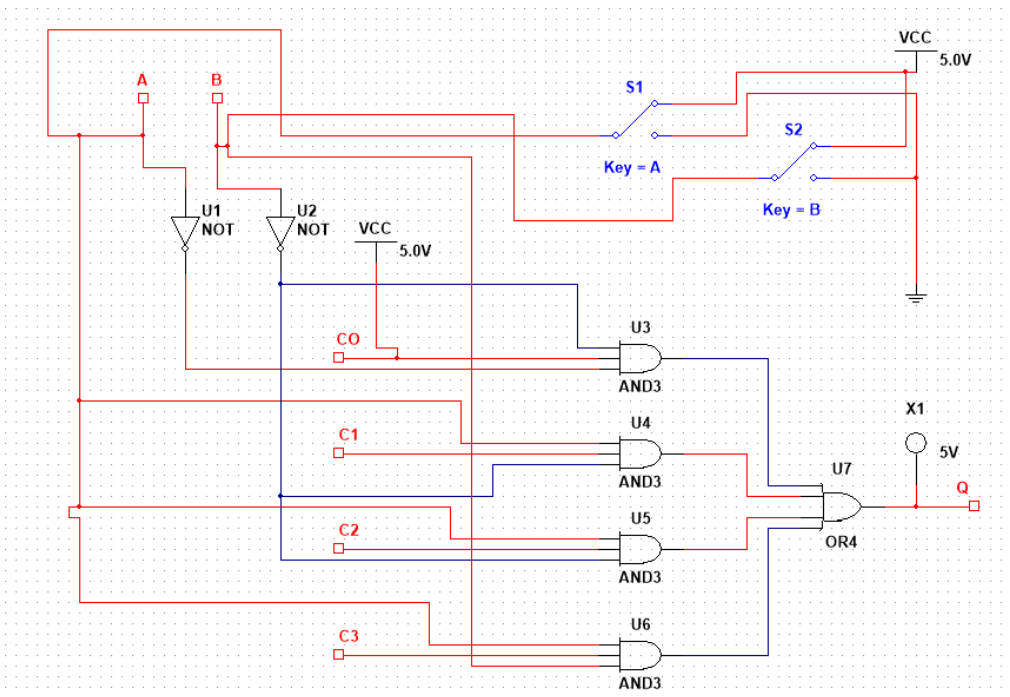
Boolean Expression of 4-1 Multiplexer:

$$Q = C_0 \cdot \bar{A} \cdot \bar{B} + C_1 \cdot \bar{A} \cdot B + C_2 \cdot A \cdot \bar{B} + C_3 \cdot A \cdot B$$

Multisim Design:

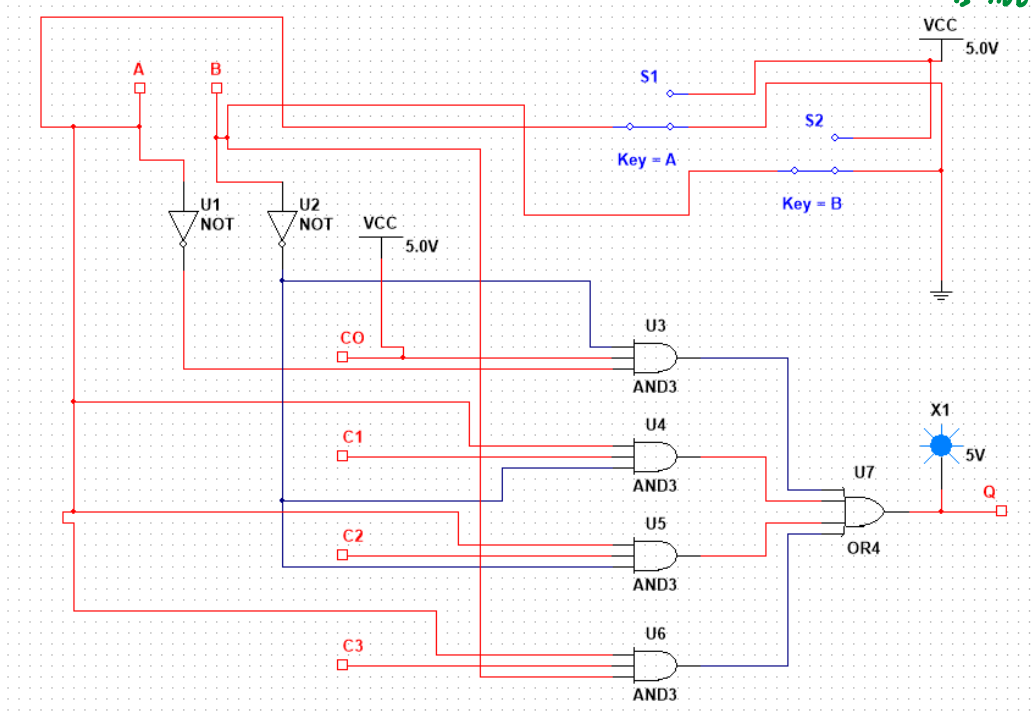


Multisim Design – proof of testing:



The screenshot above shows that Two Single Pole Double Throw switches have been added to the circuit for proving functionality. A 5V VCC has also been added along with a 5V blue probe acting as an output. ✓

As seen in the screenshot above when both switches are output 1 the probe isn't activated. *is not*



The screenshot above shows the working of C_0 , when both switches are giving an output 0 the blue probe gives an output 1. Using the table above it clearly shows that the multisim design and multiplexer truth table match one another. ✓

Task 3 - Sequential Logic

The truth table of the D-type and J-K Flip-Flop

- Construct the following debouncing circuit, and connect the clock of a D-type flip-flop to the output. Monitoring the clock, Q and $\overline{Q}$ outputs with LEDs and complete Table 1.
- Now connect the clock of J-K flip-flop to the output. Monitoring the clock, Q and $\overline{Q}$ outputs with LEDs and complete Table 2.

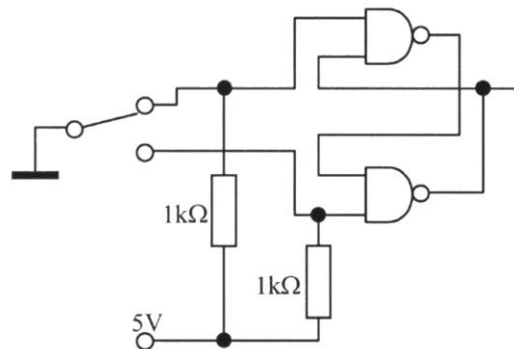
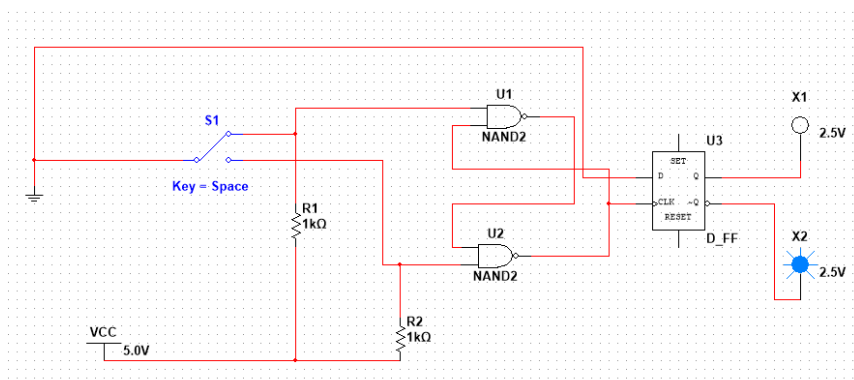


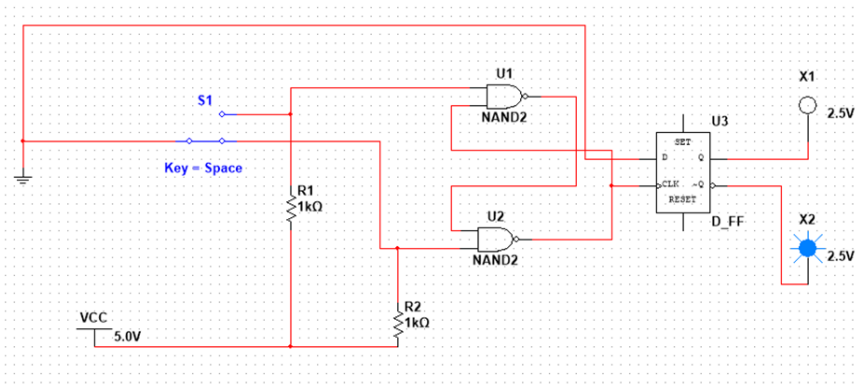
Table 1 - D-type truth table:

Input	Outputs	
D	Q	$\overline{Q}$
0	0	1
1	1	0



Debouncing circuit D Type:





The first circuit above shows a debouncing D Type circuit, D has been connected to ground. As seen in the circuit above probe X2 has been activated when S1 is giving an output 1. The second circuit shows that the switched to output 0, but the probe is still activated, this is because the D type flip flop stores and holds data.

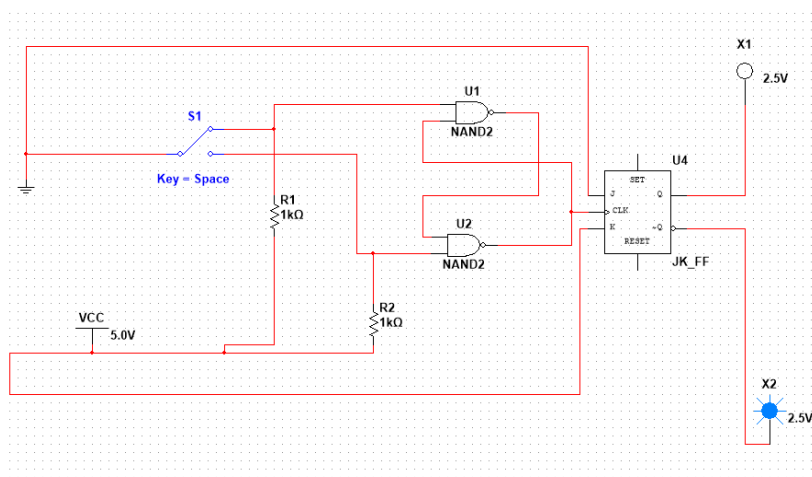
D Type:

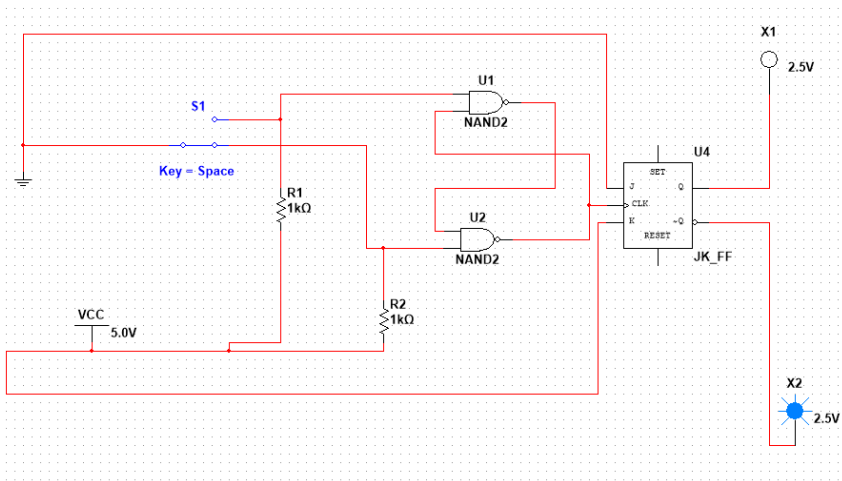
The D Type flip flop is so called because it is a data storage element. The D type flip flop is the most widely used of the three basic flip flop types. It is used in shift registers, storage registers, register files and wherever data are stored or buffered. (Hughes, 2016)

Table 2 – J-K truth table:

Input		Outputs		
J	K	Q	$\overline{Q}$	
0	0	No change.		
0	1	0	1	Reset.
1	0	1	0	Set.
1	1	Toggle.		

Debouncing circuit for Inputs J = 0 and K = 1:





In the two screenshots above it shows the debouncing circuit for the JK Flip Flop – J Input = 0, K Input = 1, the circuits show that when the switch is 0 or 1 the $\bar{Q}$ output is just resetting itself constantly.

What is JK Type flip flop:

‘The JK Flip flop is a clocked bistable latch with inputs J and K which perform a similar function to the S and R inputs of a clocked SR bistable latch. The purpose in doing this is to avoid the indeterminate state when both J and K are logic 1. With the additional feedback only one of the two input gates is opened at a time, since Q and $\bar{Q}$ are never logic 1 at the same time. The effect of the feedback is that, when J and K are both logic 1 and the flip flop is clocked, the output will change state.’ (Hughes, 2016)

The statement above basically how the circuit above is working and why JK flip flops are widely used in industries.

c) The cross-coupled NAND gates are for switch debouncing. Why are they needed and how do they work?

The main reason why these NAND gates are used for debouncing is because ‘when a common mechanical push button switch is pressed two electrical contacts are forced together forming a low impedance path for current to flow. The problem that arises is that the contacts do not go from a state of no contact to contact cleanly. The contacts rub against each other and bounce off each other several times before coming to rest against each other. Switch debouncing is an electronic design ensures that the device that is sampling the switch waveform does not misinterpret a single button press.’ (Burge, 2013)

Have not explained how it works.

Task 4 - Using Sequential Logic to Solve Real Problems

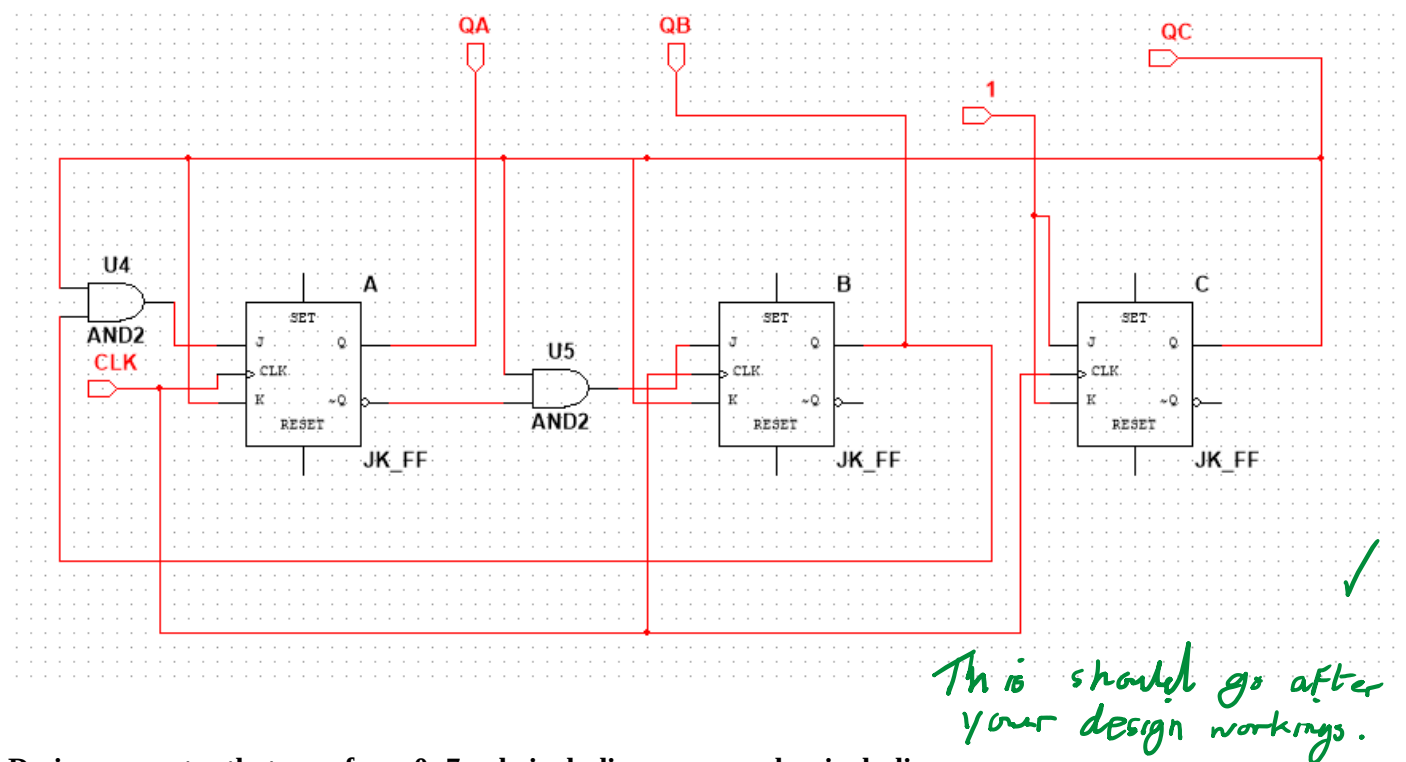
Design and simulate a 3-stage synchronous binary counter using JK flip-flops that will produce the even numbers (including zero) in the range 0 to 7.

Excitation table example:

Designing a counter – x = 'don't care'

Present Q	Next Q	J Value	K Value
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

Multisim Design:



Design a counter that goes from 0 -7 only including even number including zero:

	Present			Next								
	Q _A	Q _B	Q _C	Q _A	Q _B	Q _C	J _A	K _A	J _B	K _B	J _C	K _C
0	0	0	0	0	1	0	0	x	1	x	0	x
2	0	1	0	1	0	0	1	x	x	1	0	x
4	1	0	0	1	1	0	x	0	1	x	0	x
6	1	1	0	0	0	0	x	1	x	1	0	x

Karnaugh Maps for Table above:

• $J_A = Q_B$ ✓

$Q_B Q_C$		00	01	11	10
Q_A	0	0	x	x	1
	1	x	x	x	x

You have not grouped the logic "1" for J_A and K_A .

• $K_A = Q_B$ ✓

$Q_B Q_C$		00	01	11	10
Q_A	0	x	x	x	x
	1	0	x	x	1

• $J_B = 1$ ✓

$Q_B Q_C$		00	01	11	10
Q_A	0	1	x	x	x
	1	1	x	x	x

Again have not shown the grouping.

• $K_B = 1$ ✓

$Q_B Q_C$		00	01	11	10
Q_A	0	x	x	x	1
	1	x	x	x	1

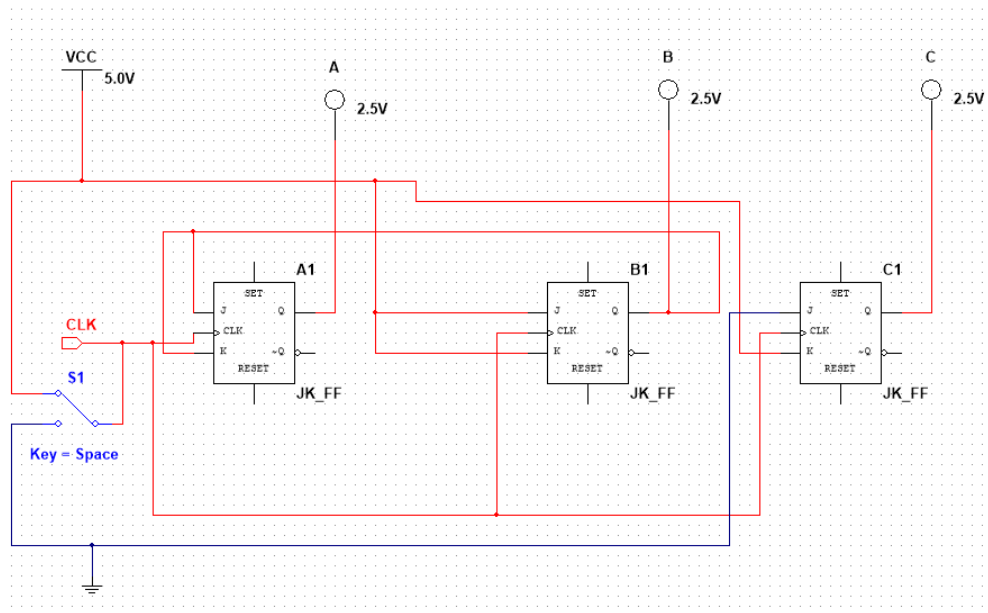
• $J_C = 0$ ✓

$Q_B Q_C$		00	01	11	10
Q_A	0	0	x	x	0
	1	0	x	x	0

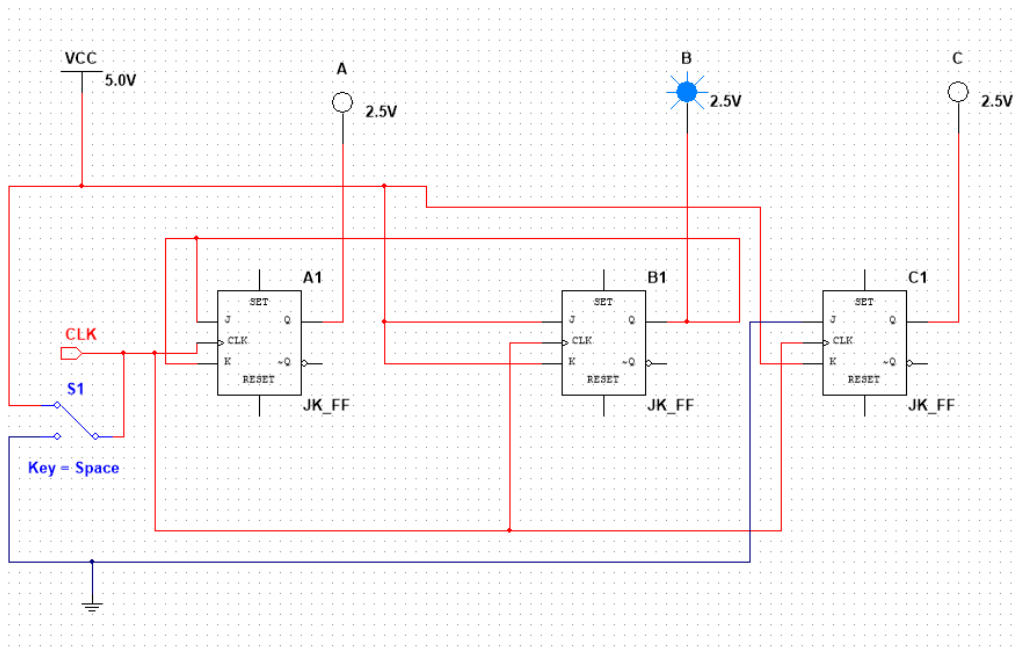
• $K_C = 1$ ✓

$Q_B Q_C$		00	01	11	10
Q_A	0	x	x	x	x
	1	x	x	x	x

Multisim Design for binary code 0:

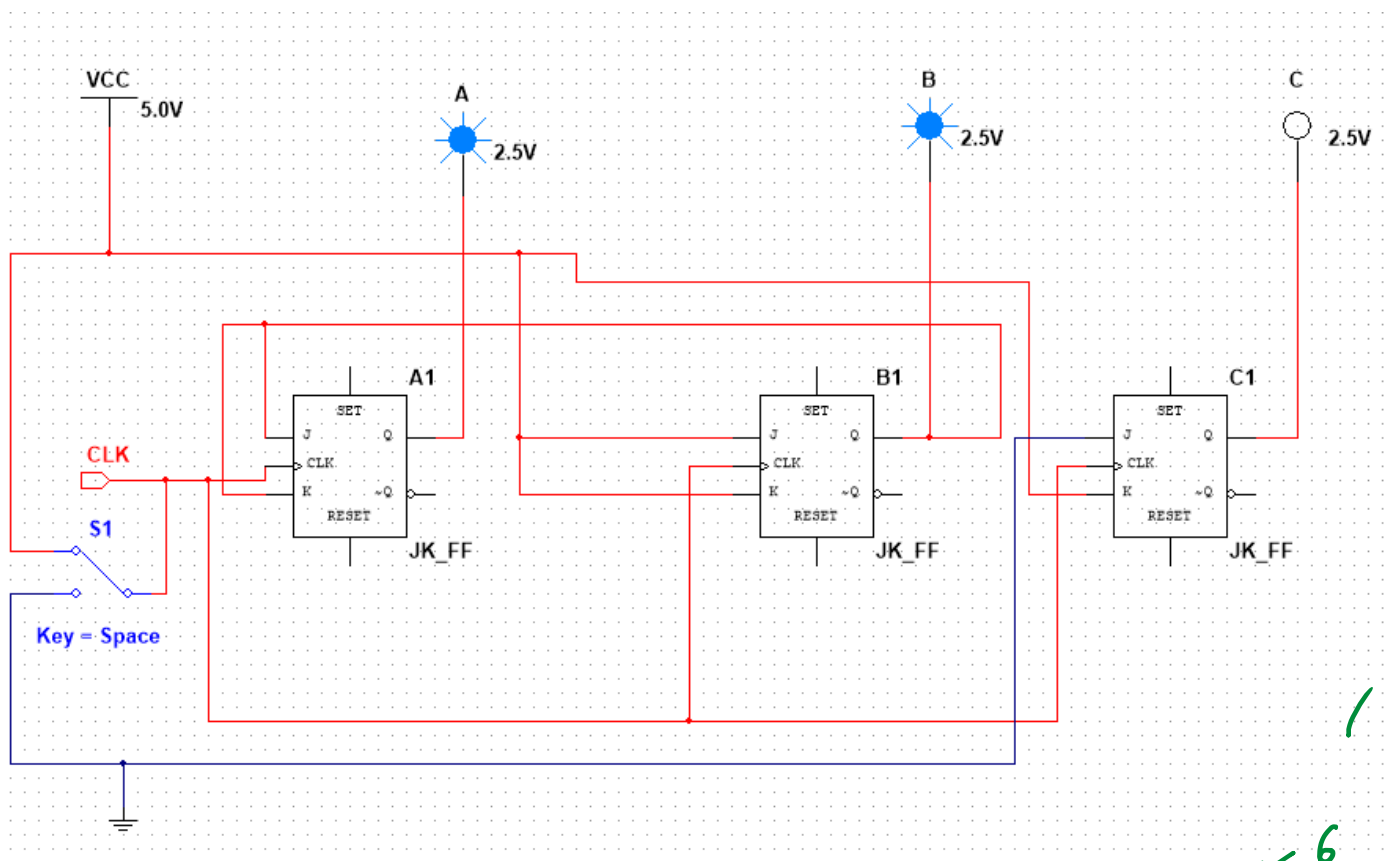


Design for binary code 2:



The screenshot above shows that when the switch is pressed once Probe B is activated, this is proving that the binary counter is corresponding with table above.

Design for binary code 6:



The screenshot above shows that when the switch is pressed three times Probe A which is representing 4 and Probe B which is representing 2 are activated, this is proving that the binary counter is corresponding with table above.

References

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