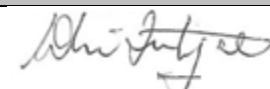


EXAMINATION INTERNAL VERIFICATION FORM (2017-2018)

MODULE :	PSDE 6018 Production and Test			LEVEL:	6
PROGRAMME :	BSc Electrical and Electronic Engineering			TERM OF EXAM: (SPRING OR SUMMER)	Spring
LEARNING OUTCOME(S) BEING ASSESSED:	All	EXAM PAPER:	Main	EXAMINATION AUTHOR :	R Jenkins

VERSION:	DATE SUBMITTED FOR VERIFICATION:	INTERNAL VERIFIER COMMENTS (Approval or detail of amendments required):	DATE:
1.	19/03/2018	Conforms to the assessment pattern described in the module syllabus Tests the module learning outcomes appropriately	20/03/18
2.			

INTERNAL VERIFIER PLEASE TICK TO INDICATE THAT THE EXAMINATION:	
☒	Conforms to the assessment pattern described in the module syllabus
☒	Tests the module learning outcome(s) appropriately

SIGNATURES OF FINAL APPROVAL:	SIGNATURE	DATE
INTERNAL VERIFIER: I confirm that this version of the exam paper is ready to be sent to the external examiner		20/03/18
EXAM AUTHOR: I confirm that internal verifier and external examiner approval have been received and that this version of the exam paper is ready for printing.		

**UNIVERSITY OF WALES:
TRINITY SAINT DAVID**



**PRIFYSGOL CYMRU:
Y DRINDOD DEWI SANT**

LOCATION: COLEG SIR

LLEOLIAD: COLEG SIR GAR

LEVEL 6

LEFEL 6

**EXAMINATION PERIOD
MAY 2018**

**CYFNOD ARHOLIADAU
MAI 2018**

MODULE CODE: PSDE6018

Electronic Production and Test

TIME: 2 1/2 HOURS

ANSWER THREE QUESTIONS

Equipment or materials required – Calculators are permitted

Adnoddau neu ddefnyddiau sydd eu hangen – Caniateir cyfrifiannell

Main Paper

Question 1

- (a) Why is compliance testing of electronic products necessary?

[Marks 6]

- (b) Explain the difference between ‘critical’ and ‘non-critical’ components in terms of compliance testing. Use a Personal Computer as a device to illustrate your answer.

[Marks 6]

- (c) “There is one particular danger to electronic components and assemblies that is present in both the design laboratory and the production environment. This is the damage from electrostatic discharge (ESD)”

Discuss the above statement, outlining:

- (i) How electrostatic charge builds up.

[Marks 4]

- (ii) How an electrostatic discharge occurs.

[Marks 3]

- (iii) The problems and types of damage this may cause to components.

[Marks 3]

- (iv) The preventative static protection that could be implemented.

[Marks 6]

- (d) Explain with an example why the decibel notation is convenient for EMC engineers.

[Marks 6]

[Total Marks = 34]

Question 2

- a) If a manufacturing process is producing steel pins and the mean value for the length of the pin is 15mm.

If the upper and lower specification ranges are $\pm 0.05\text{mm}$:

- (i) What would be the standard deviation (sigma) if 2 sigma on either side of the mean were used (2 sigma level). Show using a chart diagram. [Marks 8]
- (ii) Determine if this process is capable using the 6 sigma process capability method. [Marks 6]
- (iii) What does it mean if the process is said to be capable or not? [Marks 4]

- b) If the example of a steel pin machine is used here with a 4 sigma level capability:

If the mean value was 15mm which has now shifted to 15.02mm and the range is still $\pm 0.05\text{mm}$:

- (i) What is the standard deviation and limits for the 4 sigma level? [Marks 3]
- (ii) Find the capability index value for the shift in the mean. [Marks 6]
- (iii) What does this indicate and why? [Marks 3]
- (iv) If the mean value has drifted due to wear and tear of the machine parts, why is the capability ratio (C_p) not suitable to take this into consideration? [Marks 4]

[Total Marks 34]

Question 3

- a) Explain why fault simulators use the ‘single stuck at’ fault model to describe faults in digital circuits. Derive the single stuck at fault model for a three input ‘AND’ function and a three input ‘OR’ function.

[Marks 8]

- b) Describe the ‘single stuck at’ fault modelling process for the circuit shown in Figure 1.1

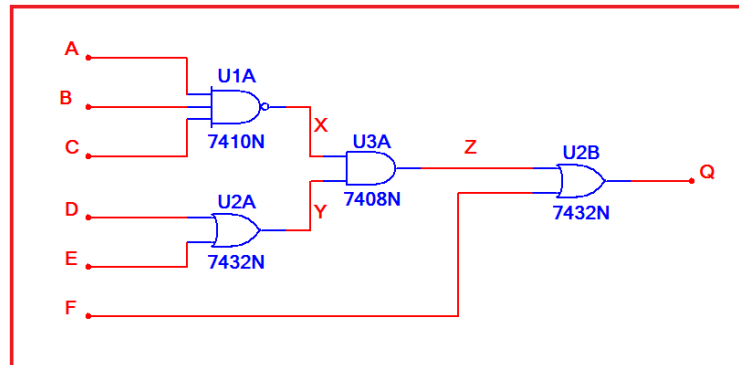


Figure 1.1

[Marks 8]

- c) Table 1.1 relates the ‘minimum number of test vectors’ required to test the circuit shown in Figure 1.1 above which has been reduced from 64 tests to 7.

Test No.	A	B	C	D	E	F	Q	X	Y	Z	Hex	Faults Detected
1	1	1	1	1	1	0	0	0	1	0	7C	A, B, or C SA0 X SA1
2	0	1	1	1	0	0	1	1	1	1	39	A SA1; D SA0
3	1	0	1	0	1	0	1	1	1	1	55	B SA1; E SA0
4	1	1	0	1	1	0	1	1	1	1	6D	C SA1; X or Y SA0 Z SA0
5	0	0	0	0	0	0	0	1	0	0	00	D or E SA1 Y SA1
6	1	1	1	0	0	0	0	0	0	0	70	F or Z SA1
7	1	1	1	0	0	1	1	0	0	0	73	F SA0

Table 1.1

- i) Design a 'pattern generator' (PG) that will output the test vectors using D type flip flops (f/f's), and derive Boolean expressions for the 'next state' of the f/f's (DA to DF).

[Marks 16]

- ii) What 'seed' value would you apply to the circuit to enable the PG to operate?

[Marks 2]

[Total Marks 34]

Question 4

- a) A traditional application for linear feedback shift registers is in cyclic redundancy check (CRC) calculations. This can be used to detect errors in data communication.

Explain how CRC applications are used to detect errors in the data stream being transmitted and received at another station.

[Marks 4]

- b) Provide a block diagram for a LFSR with polynomial $(1 + x^3 + x^4)$ and why a 4 – bit CRC calculator would not be considered to provide sufficient integrity.

[Marks 6]

- c) Explain the equation linking a serial input sequence $G(x)$ is input serially into a 4 – bit LFSR based CRC redundancy check with a characteristic polynomial $P(x)$.

[Marks 3]

- d) The following data stream (1010110010101111) is input serially into a 4 – bit LFSR based signature analyser with a characteristic polynomial.

$$G(x) = 1 + x^2 + x^4 + x^5 + x^8 + x^{10} + x^{12} + x^{13} + x^{14} + x^{15}$$

$$P(x) = 1 + x^3 + x^4$$

Show how the output checksum is derived using a Truth table of division.

[Marks 9]

- e) Show how the input stream $G(x^2)$ below, fed into the same CRC as above can produce the same checksum.

$$G(x^2) = 1 + x^2 + x^5 + x^7 + x^{10} + x^{12} + x^{13} + x^{14} + x^{15}$$

[Marks 9]

- f) As shown in (e) above, the 4 bit device could mask errors in the data stream being transmitted. Explain the measures needed to be taken to minimise these errors.

[Marks 3]

Total Marks 34

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LEVEL 6

**EXAMINATION PERIOD
MAY 2018**

LLEOLIAD: COLEG SIR GAR

LEFEL 6

**CYFNOD ARHOLIADAU
MAI 2018**

MODULE CODE: PSDE6018

Electronic Production and Test

ANSWER THREE QUESTIONS

Equipment or materials required – Calculators are permitted

Adnoddau neu ddefnyddiau sydd eu hangen – Caniateir cyfrifiannell

Main paper Solutions

Question 1

a)

Compliance test for electronic devices include emissions tests, immunity tests, and safety tests. Emissions tests ensure that a product will not emit harmful electromagnetic interference in communication and power lines. Immunity tests ensure that a product is immune to common electrical signals and Electromagnetic interference (EMI) that will be found in its operating environment, such as electromagnetic radiation from a local radio station or interference from nearby products. Safety tests ensure that a product will not create a safety risk from situations such as a failed or shorted power supply, blocked cooling vent, and power line voltage spikes and dips.

Compliance testing of Electrical and Electronic products is necessary for access into worldwide markets.

They give awareness to potential customers & users that the product complies with applicable standards for safety and performance.

Certification Marks are required to satisfy market requirements.

[6]

b)

The student should list the following items and explain what the difference between critical and non-critical means.

Critical Components

1. PC Case
2. Power Supply Unit
3. Main Board/CPU

Non Critical

1. Add-on cards
2. Hard Drive
3. Floppy Drive
4. CD Drive
5. Memory
6. Monitors
7. Keyboard & Mouse

[6]

c)

(i)

ESD first requires a build-up of an electrostatic charge. This occurs when two different materials rub together. One of the materials becomes positively charged; the other becomes negatively charged. The positively-charged material now has an electrostatic charge.

[4]

(ii)

When that charge comes into contact with the right material, it is transferred and we have an ESD event. When the charge is released onto an electronic device such as an expansion card, the intense heat from the charge can melt or vaporize the tiny parts in the card causing the device to fail.

[3]

(iii)

Sometimes an ESD event can damage a device, but it continues to function. This is called a latent defect, which is hard to detect and significantly shortens the life of the device.

[3]

(iv)

Many electronic devices are susceptible to low volts ESD events. For example, computer HD components are sensitive to only 10 volts. For this reason, manufacturers of electronic devices incorporate measures to prevent ESD events throughout the manufacturing, testing, shipping, and handling processes. E.g, an employee may wear a wrist strap when working with devices or may wear ESD control footwear and work on an ESD floor mat that causes the electrostatic charge to go into the ground instead of into the device. Sensitive devices can be packaged with materials that shield the product from a charge.

[6]

(d)

Decibel notation is important because it is a way of expressing ratios that may or not may span orders of magnitude.

It offers scale compression and is not dependant on units.

It is also used to express the amplitude of various signal parameters such as voltage or current relative to a given reference level.

For example: A power ratio, $P_2 : P_1$, in dB is calculated as,

$$\text{Power ratio in dB} = 10 \log (P_2 / P_1)$$

If the power received is 10W compared to a 5W specification, then the power received is double the specification.

$$\text{i.e. } 10 \log (10W / 5W) = 3\text{dB}$$

As opposed to:

If the power received is 5W compared to a 10W specification, then the power is half which is -3dB

$$\text{i.e. } 10 \log (5W / 10W) = -3\text{Db}$$

The scale is just of the ratios and is a compression.

[6]

[34 marks]

Question 2

(a)

(i) Mean = 15mm range = $\pm 0.05\text{mm}$, therefore for a 2 sigma level, the standard deviation is:

$$0.05 / 2 = 0.025$$

Draw a chart showing the STD scale either side of the mean.

[8]

(ii) STD = 0.025

$$C_p = \text{Upper spec} - \text{Lower spec} / 6\sigma$$

$$C_p = 15.05 - 14.95 / 6\sigma$$

$$C_p = (15.05 - 14.95) / (6 * 0.025) = 0.6$$

Therefore $C_p < 1$ and is not capable.

3 sigma process:

$$\text{STD} = 0.0166$$

$$C_p = 15.05 - 14.95 / 6\sigma$$

$$C_p = 0.1 / 6 (0.0166) = 1.004$$

This proves that this system is not capable when operating at 2 sigma level because the capability value is <1 .

At the 3 sigma level it shows that the process is just about capable where $C_p = 1$.

A recommendation would be to increase the sigma level of operation to increase the C_p value above the minimum.

[6]

(iii) This means:

Six Sigma is basically a process quality goal, where sigma is a statistical measure of variability in a process where Six Sigma requires the process standard deviation be no more than one-twelfth of the total allowable spread.

That is 6 times the standard deviation either side of the mean.

If 6σ fits into the upper and lower limits either side of the mean then it is said to be 'capable', if not then it is said to be 'not capable'

Draw a chart to illustrate this.

[4]

(b)

(i) This is where 4 standard deviations can fit on either side of the mean and can be calculated :

$$4\sigma (\text{std}) = \text{range} / 4 = 0.005 / 4 = 0.0125$$

Therefore the limits will be:

Upper limits - 15.025, 15.05

Lower limits – 14.975, 14.95

[3]

(ii) Cpk is an index (a simple number) which measures how close a process is running to its specification limits, relative to the natural variability of the process. The larger the index, the less likely it is that any item will be outside the specs.

$$Cpk \text{ (Capability Index)} = \min (\text{Mean} - L_{\text{spec}} / 3\sigma, U_{\text{spec}} - \text{mean} / 3\sigma)$$

$$Cpk = \min (15.02 - 14.95 / (3 \times 0.0125), 15.05 - 15.02 / (3 \times 0.0125))$$

$$Cpk = \min (1.86, 0.8)$$

$$Cpk = 0.8 \quad [6]$$

(iii) The process can no longer operate at the 4 sigma level. This is because according to the 3σ rule, 3σ will fit only 0.8 times above the mean and 1.86 times below the mean. Either side of the mean must be > 1 to be capable.

[3]

(iv) The Cp (Capability Ratio) will remain the same because the std deviation remains the same. None of the attributes in the Cp calculation will change due to a change in the mean value.

The Cpk calculation takes into account the shift in the mean and compares the result with the 3sigma rule i.e. 3 standard deviations either side of the mean. If the result of any side being < 1 it is said to be "not capable".

[4]

[34 marks]

Question 3.

1(a)

The single stuck at fault model is used predominantly because of its simplicity. It can be shown that if all single faults are detected then a very high percentage of multiple faults will be detected. The single stuck at fault model applies a single fault to each node of the circuit in turn. The faults are defined as stuck at 0 (a short circuit to ground) and stuck at 1 (a short circuit to the supply rail). The total number of faulty circuits that must be simulated using the single stuck at model is $n + 1$ where n is the number of circuit nodes. If a multiple stuck at fault model is used then each node can have any one of three states which are good, SA1 or SA0. The total number of faulty circuits that need to be simulated is $3^n - 1$. This is impractical for large circuits due to the very large number of faulty circuits.

The use of the fault modelling process can simplify the number of tests needed compared the exhaustive testing by typically a factor of 5 to 10.

AND Model

1111
0111
1011
1101
1110

Or Model

0000
1000
0100
0010
0001

[8]

1(b)

Step 1

Insert fault models for each gate at the inputs of the gates. The number of tests required for each gate is $m+1$ where m = the Number of inputs.
Identify the fault that each test locates.

Step 2

Determine the propagation path to an observable node and enter the propagation vector. This can be determined as follows. If the gate that the fault must be propagated through is a AND or NAND function all other inputs except that carrying the fault must be set to 1.
If the gate that the fault must be propagated through is a OR or NOR function all other inputs except that carrying the fault must be set to 0.

Step 3

Trace back through the circuit determining what gate inputs must be set to implement steps 1 and 2. Note any conditions where a number of combinations of inputs can be used to achieve the desired aim. An example of this would be setting the output of an OR gate to 1, 01, 10 and 11 would all achieve this and are equally valid.

Step 4

Use a HEX mapping of all inputs and the output to determine repeated tests. Delete the duplicates moving the fault identifier to the retained test.

Step 5

Using the conditions where a number of inputs are valid, look for valid input conditions that will create duplicate tests.

[8]

1(c)

(i)

A	B	C	D	E	F	A+	B+	C+	D+	E+	F+	Fault Detected
1	1	1	1	1	0	0	1	1	1	0	0	A, B, or C SA0: X SA1
0	1	1	1	0	0	1	0	1	0	1	0	A SA1; D SA0
1	0	1	0	1	0	1	1	0	1	1	0	B SA1; E SA0
1	1	0	1	1	0	0	0	0	0	0	0	C SA1; X or Y SA0: Z SA0
0	0	0	0	0	0	1	1	1	0	0	0	D or E SA1: Y SA1
1	1	1	0	0	0	1	1	1	0	0	1	F or Z SA1
1	1	1	0	0	1	1	1	1	1	1	0	F SA0

$$\begin{aligned}
 A+ &= DA = A.B.C.ND.NE + \\
 &A.NB.C.ND.E.NF + \\
 &NA.B.C.D.NE.NF + \\
 &NA.NB.NC.ND.NE.NF
 \end{aligned}$$

$$\begin{aligned}
 B+ &= DB = A.B.C.ND.NE + \\
 &A.NB.C.ND.E.NF + \\
 &NA.NB.NC.ND.NE.NF + \\
 &A.B.C.D.E.NF
 \end{aligned}$$

$$\begin{aligned}
 C+ &= DC = A.B.C.ND.NE + \\
 &A.B.C.D.E.NF + \\
 &NA.B.C.D.NE.NF + \\
 &NA.NB.NC.ND.NE.NF
 \end{aligned}$$

$$D+ = DD = A.B.C.ND.NE.F +$$

$$A.B.C.D.E.NF +$$

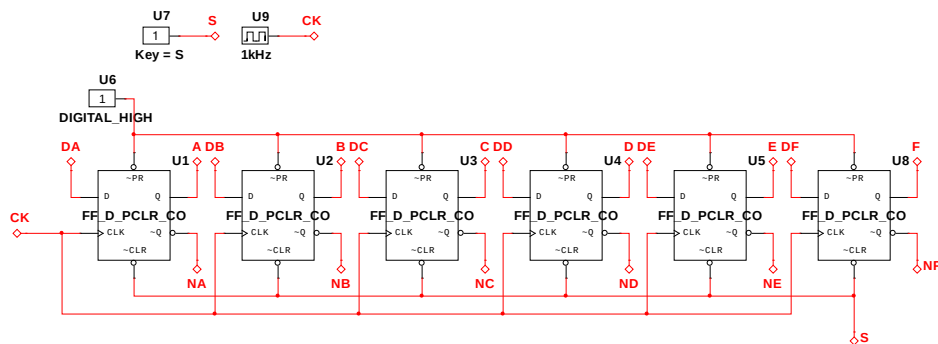
$$A.NB.C.ND.E.NF$$

$$E+ = DE = A.B.C.ND.NE.F +$$

$$A.NB.C.ND.E.NF +$$

$$NA.B.C.D.NE.NF$$

$$F+ = DF = A.B.C.ND.NE.NF$$



[16]

(ii)

Apply a 'seed' value S of '000000' via a high to low signal transition on the 'CLR' inputs of the f/f's.

[2]

[34 marks]

Question 4

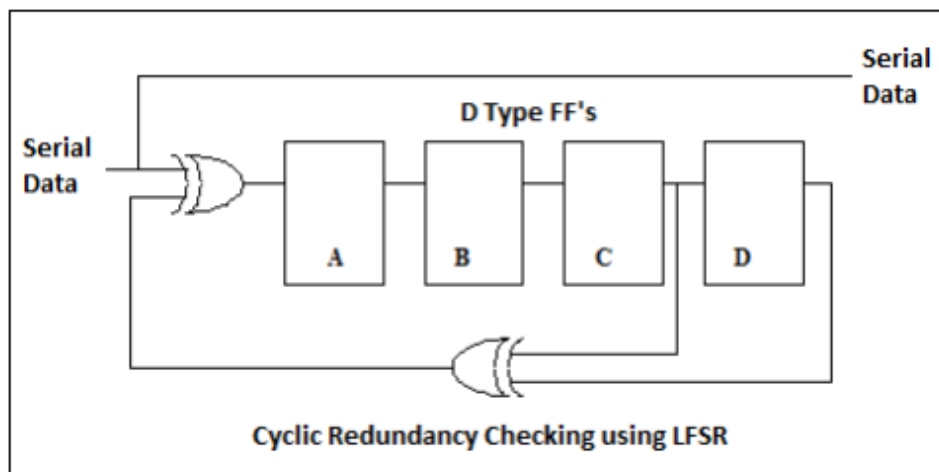
(a)

- The stream of bits being transmitted is used to modify the values fed back into an LFSR.
- The final CRC value stored in the LFSR is known as a checksum and is dependent on every bit in the data stream.
- After all of the data bits have been transmitted, the transmitter sends its own checksum value to the receiver.
- The receiver contains an identical CRC because it runs it through the same LFSR setup and generates the checksum.
- The checksum from the transmitter and receiver are compared for errors which determine corruption of data during transmission.
- This form of error detection is very efficient in terms of the small number of bits that have to be transmitted in addition to the data.

[4]

(b)

Block diagram of LFSR with given polynomial $(1 + x^3 + x^4)$



In the real world, a 4-bit CRC calculator would not be considered to provide sufficient confidence in the integrity of the transmitted data.

This is due to the fact that a 4-bit LFSR can only represent 16 unique values, which means that there is a significant probability that multiple errors in the data stream could result in the two checksum values being identical.

However, as the number of bits in a CRC calculator increases, the probability that multiple errors will cause identical checksum values approaches zero. For this reason, CRC calculators typically use a minimum of 16-bits providing 65,536 unique values.

[6]

(c)

$$G(x) = 1 + x^2 + x^4 + x^5 + x^8 + x^{10} + x^{12} + x^{13} + x^{14} + x^{15}$$

$$P(x) = 1 + x^3 + x^4$$

$$G(x) / P(x) = Q(x) + R(x) / P(x)$$

$$G(x) = Q(x) \cdot P(x) + R(x)$$

An LFSR carries out polynomial division on the input stream by the characteristic polynomial, producing an output stream corresponding to the quotient $Q(x)$ and a remainder $R(x)$.

This can be illustrated using the MODULO – 2 division of a bit stream (i.e. X-OR instead of subtraction) by a number representing the characteristic polynomial.

[3]

(d)

The operation of the circuit is shown in table 1 with an initial state of 0000.

Input Data	Input to Register	New State of Register ABCD	Output
		0000	
1	1	1000	0
0	0	0100	0
1	1	1010	0
0	1	1101	0
1	0	0110	1
1	0	0011	0
0	0	0001	1
0	1	1000	1
1	1	1100	0
0	0	0110	0
1	0	0011	0
0	0	0001	1
1	0	0000	1
1	1	1000	0
1	1	1100	0
1	1	1110	0

Table1

The two bits which are XOR'ed together are designated by __.

Q is the checksum output which can be compared to a similar checksum for error analysis.

[9]

(e)

$$\text{New } G(x) = 1 + x^2 + x^5 + x^7 + x^{10} + x^{12} + x^{13} + x^{14} + x^{15}$$

Input Data	Input to Register	New State of Register ABCD	Output
1	1	0000	
0	0	1000	0
1	1	0100	0
0	1	1010	0
(0E)	(1E)	1101	0
1	0	(1E)110	1
0	0	0(1E)11	0
(1E2)	(1E2)	00(1E)1	1
(0E3)	(1E3)	(1E2)00(1E)	1
0	0	(1E3)(1E2)00	(1E)
1	0	0(1E3)(1E2)0	0
0	0	00(1E3)(1E2)	0
1	0	000(1E3)	(1E2)
1	0	0000	(1E3)
1	1	1000	0
1	1	1100	0
1	1	1110	0

The results show with error masking it is possible to get the same CRC checksum.

[9]

(f)

If any single bit error occurs within the data stream it will always result in the error being detected by an incorrect signature in the register. Multiple errors can occasionally resulting in error masking with the correct signature being attained for an erroneous bit stream. This can be minimised by increasing the size of the LFSR. Typically CRC calculators typically use a minimum number of 16 bits.

[3]

[34 MARKS]