

Tyler Lloyd PSDE 4004 ASSIGNMENT 2

by Tyler Lloyd

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Assignment 2

Digital Circuit Design

HNC Electrical and Electronic Engineering

Tyler Lloyd
3-19-2018

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1. Introduction, aims and objectives

The objective of this assignment is to investigate and research combinational and sequential logic, comparing any differences and creating a brief write up on how they work. The assignment requires investigation into using a Finite State Machine as a design tool and also stating the benefits of FPGA's and ASIC's again writing up a summary of what they do and how they work.

The assignment requires a design phase, where a digital stopwatch will be designed. The stopwatch will count to 59 then reset to 0, being displayed over two different segment displays. This stopwatch circuit will ideally have a stop and reset function. The stopwatch design will involve state allocation, state diagrams, state tables, Karnaugh maps and equations formed from the Karnaugh maps.

Once the stopwatch has been designed it will then be simulated using MultiSim (design software). Here, it will be designed in various stages and then combined to create the required design. The same simulation will be then created in MultiSim but in PLD mode which will allow the created simulation circuit to be transferred to a programable board, in this case it will be the Digilent Nexys 4 test board. From here the circuit can be tested and testing can be carried out. The results of the test will be analysed and compared to the specification. Any different outcomes will be explained.

2. Research

Combinational and sequential logic

Combinational logic circuits contain logic gates that are put together to make a switching circuit. The logic gates can consist of NAND, NOR and NOT gates. This logic can be analysed using truth tables, logic diagrams and Boolean expressions/algebra.

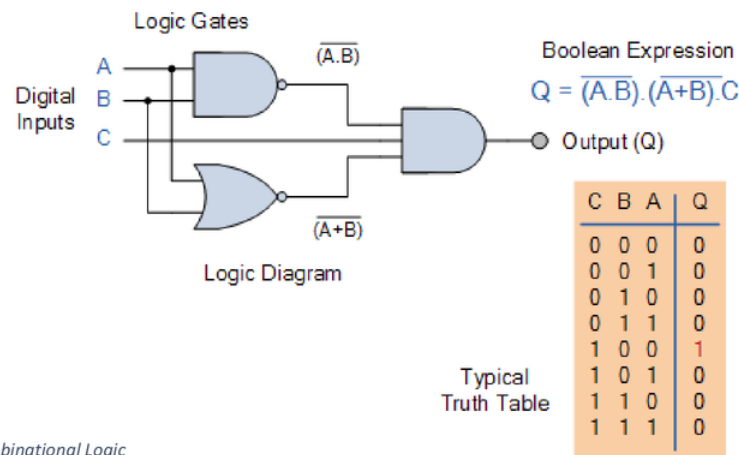


Figure 1: Combinational Logic

(Tutorials, n.d.)

Godse states "logic gates are connected to produce a specified output for certain combinations of input variables. There is no storage involved with combinational logic. Combinational logic variables are determined by the combination of input variables. Combinational circuits consist of input variables, logic gates and output variables. The logic gates accept signals from the input variables and generate output signals". (Godse, 2009)

Sequential logic is slightly different to combinational logic as it doesn't rely totally on the inputs state. Sequential logic has memory, allowing the circuit to remember previous input/output states as well as the current input state. With this logic, a clock signal will determine what happens next. Sequential logic is commonly separated in different categories: event driven, pulse driven and clock driven. Sequential logic not only has the two logic states (like combinational logic) 1 and 0, but has 3, the third being time.

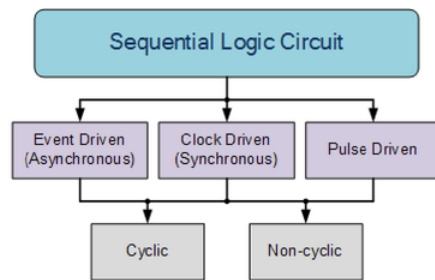


Figure 2: Sequential Logic

(Tutorials, n.d.)

Bogdan states “memory is the difference between combinational and sequential logic. Combinational logic has the output is generated from inputs. Sequential logic design has memory elements. The output is dependent on not only the current inputs but also on the state. This mean that sequential logic needs to know where it was and where it is now in order to determine where it is going with the current set of inputs”. (Wilamowski, 2015)

Combinational logic is well known from Boolean circuits. In these circuits the output is from a present input and nothing else. Sequential logic has an output dependant on the current input as well as the sequence of past inputs. Sequential circuits have a state which tells us that sequential circuits have memory. Combinational logic is based on Boolean functions and the given input.

Finite state machine being used as a design tool

A state machine is basically any device that stores the status of something at a given time and can operate on input to change the status. For example, a computer is basically a state machine, each given instruction can be seen as an input which changes a status and can cause other actions to take place. A finite state machine has a limited, or finite number of states. A finite state machine can be used as a tool for solving problems. Finite state machines can be shown through simple tables and animated illustrations.

Meijer states “a Finite State Machine is a mathematical type of computation to make reactive systems. It uses the different possible states of the system, the transitions between those states, and the events that trigger those transitions. The transitions are labelled with the triggering events”. (Finite State Machines, 2013, p. 2)

Finite State machines are often used to design digital circuits. They can be used in a lot of different software packages and has a simple code structure. They can even be used as a debugging tool.

Ted explains that “the idea behind FSM design is that software problems can be viewed from the perspective of state machines and can be solved using methods borrowed from other disciplines, like digital electronics. The type of software products suited to an FSM model can be categorised as having distinct "modes" or being "control intensive"; as they contain complex logic structures that result in a large number of control blocks, such as case structures and conditional statements. (Carmely, 2009)

FPGA's and ASIC's

ASICs are normally made for a single company for a specific system. They are expensive, time consuming and normally resource-intensive to make. They do however offer high performance and low power consumption. They are made for a specific application and are used for very specific designs.

Field-programmable gate array devices are an array of programmable blocks. These blocks are linked by programmable interconnects. FPGA's can configure any combination of digital functions. They can implement algorithms in parallel, meaning they can perform massive amounts of data processing quickly and efficiently.

FPGA's are faster to make and sell as they don't need any layout or manufacturing. They are re-programmable and design changes can be done to them later on in the process. They do however consume more power than ASIC's because of the programmable design and also have low clock speeds. FPGA's are good for draft designs and making prototypes due to they're cost. ASIC's take longer to design due to the manufacturing steps involved. Once manufactured the ASIC's often need a new chip in case of bugs or potential faults. The ASIC's design is a lot more specific but that helps when it comes down to power and performance statistics. See Figure 3: FPGA ASIC comparison for a summarised comparison.

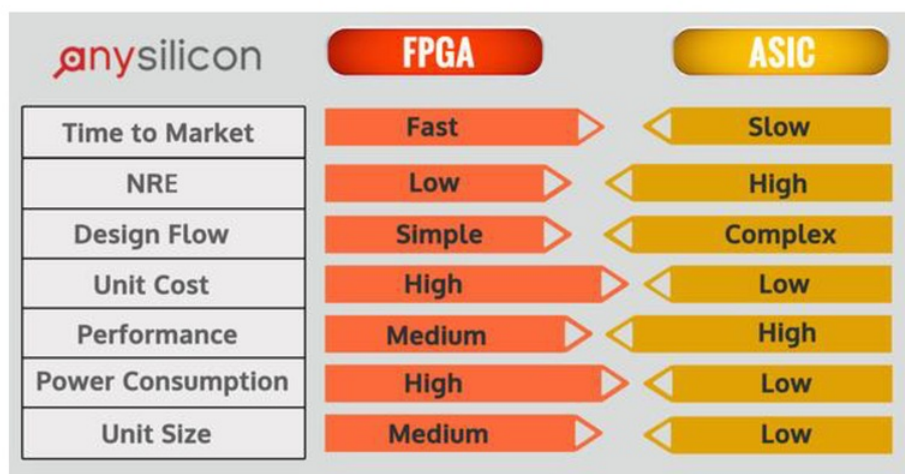


Figure 3: FPGA ASIC comparison

(Any Silicon, 2016)

3. Design Method

The requirement for this assignment is to create a digital stopwatch. The stopwatch needs to count to 59 then reset to 0. To do this the numbers should be split between two displays, where one screen displays the 'tenths' and one displays the 'units'.

The design will be created on MultiSim. It can be tested using the MultiSim software before being created using the PLD mode with later allows the program to be transferred to an FPGA board for manual testing. When creating the displays, the design process involves state allocation, a state diagram, a state table, karnaugh maps and finally the counter design on MultiSim.

Once the individual counter has been tested it will then be combined with the 7 segment display to form the final part of the 'tenths' display for the stopwatch. The same process will then happen for the decade counter and display which will represent the 'units' part of the stopwatch.

Designing the 0-5 Display

The design requirement here is to create the 7 segment display which will represent the 'tenths' units. This will be a 0 to 5 display.

State Allocation

State	Count
State 0 (S0)	Count 0
State 1 (S1)	Count 1
State 2 (S2)	Count 2
State 3 (S3)	Count 3
State 4 (S4)	Count 4
State 5 (S5)	Count 5

Figure 4: State Allocation for 0-5 display

This shows the allocation for all the states.

State Diagram

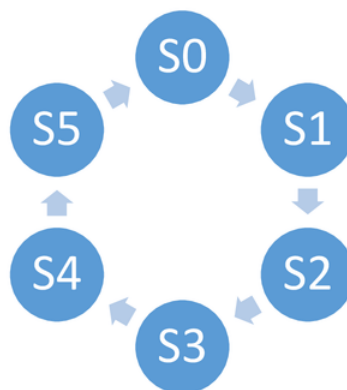


Figure 5: State Diagram for 0-5 display

State Table

Current	Next	Current			Next		
		QA	QB	QC	QA+	QB+	QC+
S0	S1	0	0	0	0	0	1
S1	S2	0	0	1	0	1	0
S2	S3	0	1	0	0	1	1
S3	S4	0	1	1	1	0	0
S4	S5	1	0	0	1	0	1
S5	S0	1	0	1	0	0	0

Figure 6: State Table for 0-5 display

From the state table Karnaugh maps can be formed.

Karnaugh maps

QA+

BC A	0	01	11	10
0	0	0	1	0
1	1	0	X	X

Figure 7: QA+ Karnaugh Map for 0-5 counter

QB+

BC A	0	01	11	10
0	0	1	0	1
1	0	0	X	X

Figure 8: QB+ Karnaugh Map for 0-5 counter

QC+

BC A	0	01	11	10
0	1	0	0	1
1	1	0	X	X

Figure 9: QC+ Karnaugh Map for 0-5 counter

Karnaugh Map Equations

Equations can then be formulated from the maps to create the equations which will later be added to the simulation. The maps are grouped (in red).

$$QA+ = A\bar{C} + B\bar{C}$$

Figure 10: QA+ Karnaugh Equation for 0-5 counter

$$QB+ = B\bar{C} + \bar{A}\bar{B}\bar{C}$$

Figure 11: QB+ Karnaugh Equation for 0-5 counter

$$QC+ = \bar{C}$$

Figure 12: QC+ Karnaugh Equation for 0-5 counter

This can now be added to the simulation.

Simulation for 0-5 Counter and Display

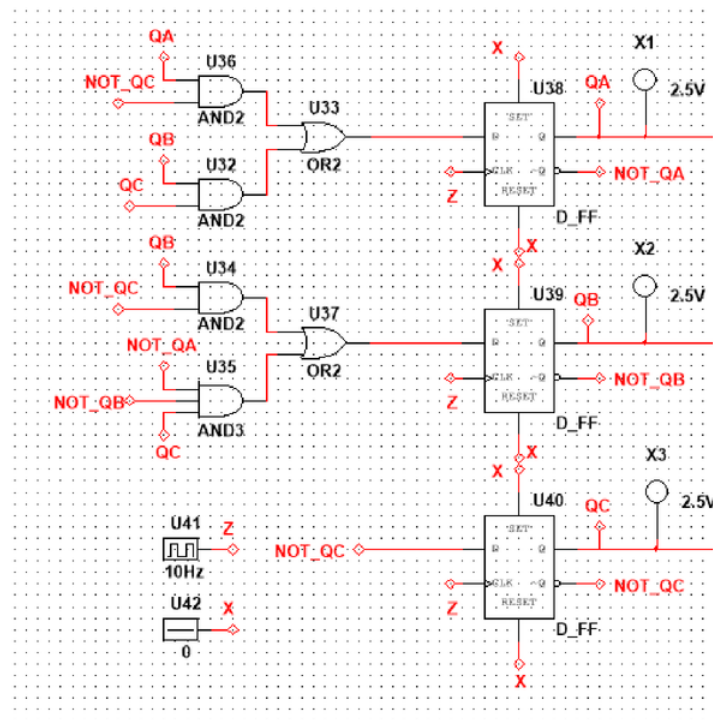


Figure 13: 0-5 Counter Circuit with added LEDs for testing

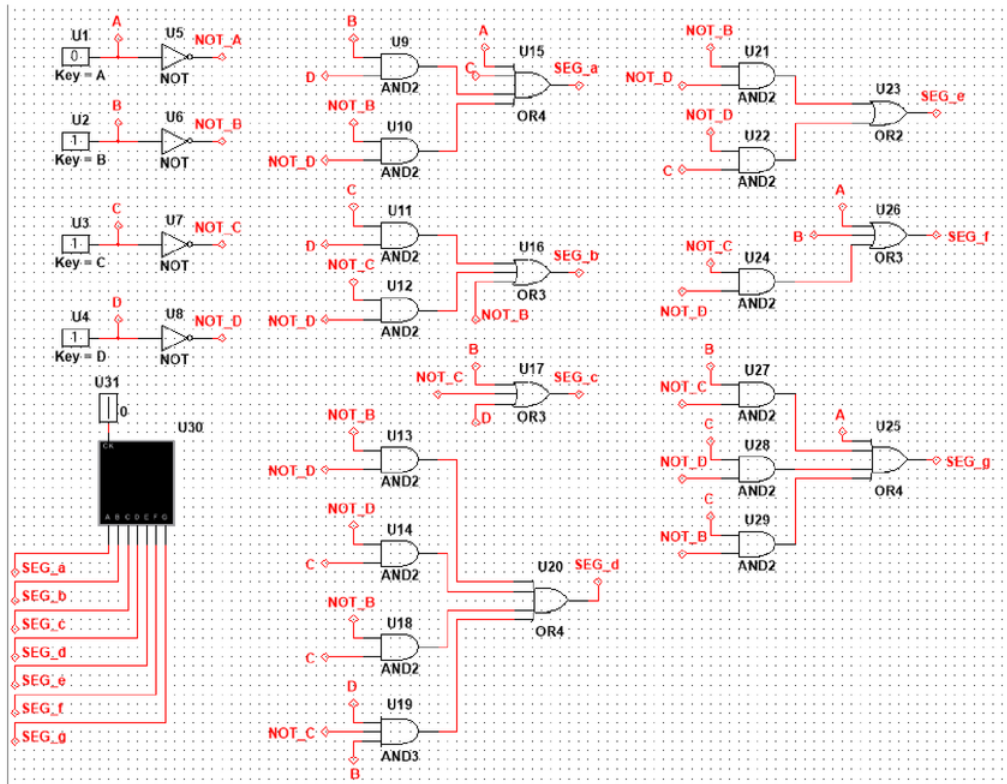


Figure 14: 0-5, clock and 7 segment display circuit with switches for testing



Figure 15: 0-5 Combined Counter and Display

Designing the 0-9 Counter

The design requirement here is to create the 7-segment display which will represent the 'Units' of the stopwatch. This will be a 0 to 9 display.

State Allocation

State	Count
State 0 (S0)	Count 0
State 1 (S1)	Count 1
State 2 (S2)	Count 2
State 3 (S3)	Count 3
State 4 (S4)	Count 4
State 5 (S5)	Count 5
State 6 (S6)	Count 6
State 7 (S7)	Count 7
State 8 (S8)	Count 8
State 9 (S9)	Count 9

Figure 16: State Allocation for 0-9 counter

This shows the allocation for all the counts.

State Diagram

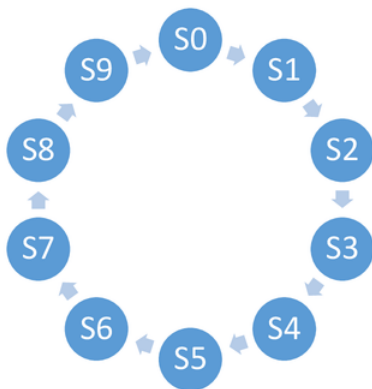


Figure 17: State Diagram for 0-9 counter

State Table

Current	Next	Current				Next			
		QA	QB	QC	QD	QA+	QB+	QC+	QD+
S0	S1	0	0	0	0	0	0	0	1
S1	S2	0	0	0	1	0	0	1	0
S2	S3	0	0	1	0	0	0	1	1
S3	S4	0	0	1	1	0	1	0	0
S4	S5	0	1	0	0	0	1	0	1
S5	S6	0	1	0	1	0	1	1	0
S6	S7	0	1	1	0	0	1	1	1
S7	S8	0	1	1	1	1	0	0	0
S8	S9	1	0	0	0	1	0	0	1
S9	S0	1	0	0	1	0	0	0	0
S10	X	1	0	1	0	X	X	X	X
S11	X	1	0	1	1	X	X	X	X
S12	X	1	1	0	0	X	X	X	X
S13	X	1	1	0	1	X	X	X	X
S14	X	1	1	1	0	X	X	X	X
S15	X	1	1	1	1	X	X	X	X

Figure 18: State Table for 0-9 Counter

From the state table Karnaugh maps can be formed.

Karnaugh maps

QA+

CD \ AB	00	01	11	10
00	0	0	0	0
01	0	0	1	1
11	X	X	X	X
10	1	0	X	X

Figure 19: QA+ Karnaugh Map for 0-9 Counter

QB+

CD \ AB	00	01	11	10
00	0	0	1	0
01	1	1	0	1
11	X	X	X	X
10	0	0	X	X

Figure 20: QB+ Karnaugh Map for 0-9 Counter

QC+

CD \ AB	00	01	11	10
00	0	1	0	1
01	0	1	0	1
11	X	X	X	X
10	0	0	X	X

Figure 21: QC+ Karnaugh Map for 0-9 Counter

QD+

CD \ AB	00	01	11	10
00	1	0	0	1
01	1	0	0	1
11	X	X	X	X
10	1	0	X	X

Figure 22: QD+ Karnaugh Map for 0-9 Counter

Karnaugh Map Equations

$$QA+ = A\bar{D} + BCD$$

Figure 23: QA+ Kanruagh Map Equation for 0-9 Counter

$$QB+ = B\bar{D} + B\bar{C} + \bar{B}CD$$

Figure 24: QB+ Kanruagh Map Equation for 0-9 Counter

$$QC+ = \bar{A}\bar{C}D + C\bar{D}$$

Figure 25: QC+ Kanruagh Map Equation for 0-9 Counter

$$QD+ = \bar{D}$$

Figure 26: QD+ Kanruagh Map Equation for 0-9 Counter

Simulation for 0-9 Counter and Display

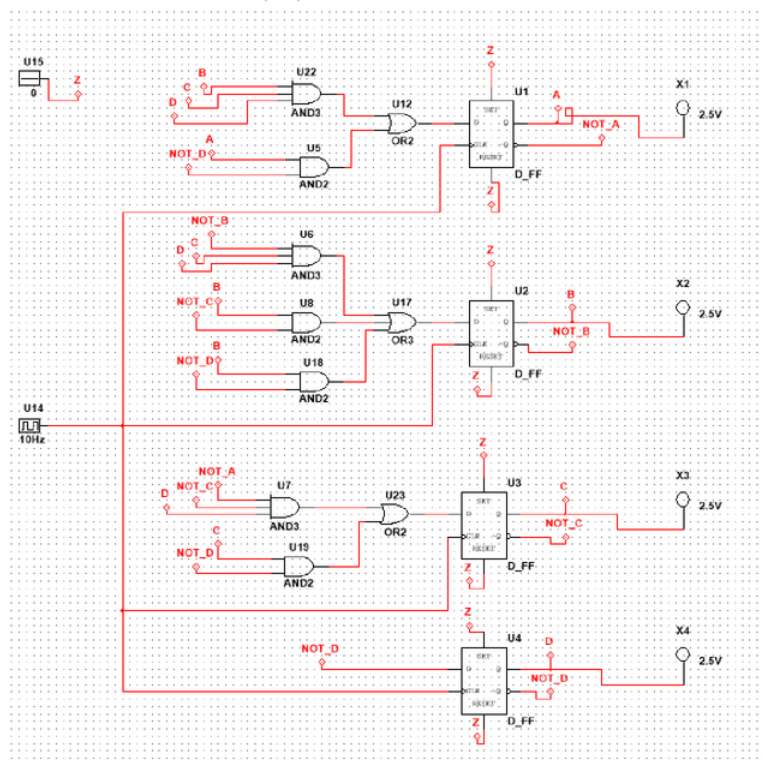


Figure 27: Decade Counter with LED's for testing

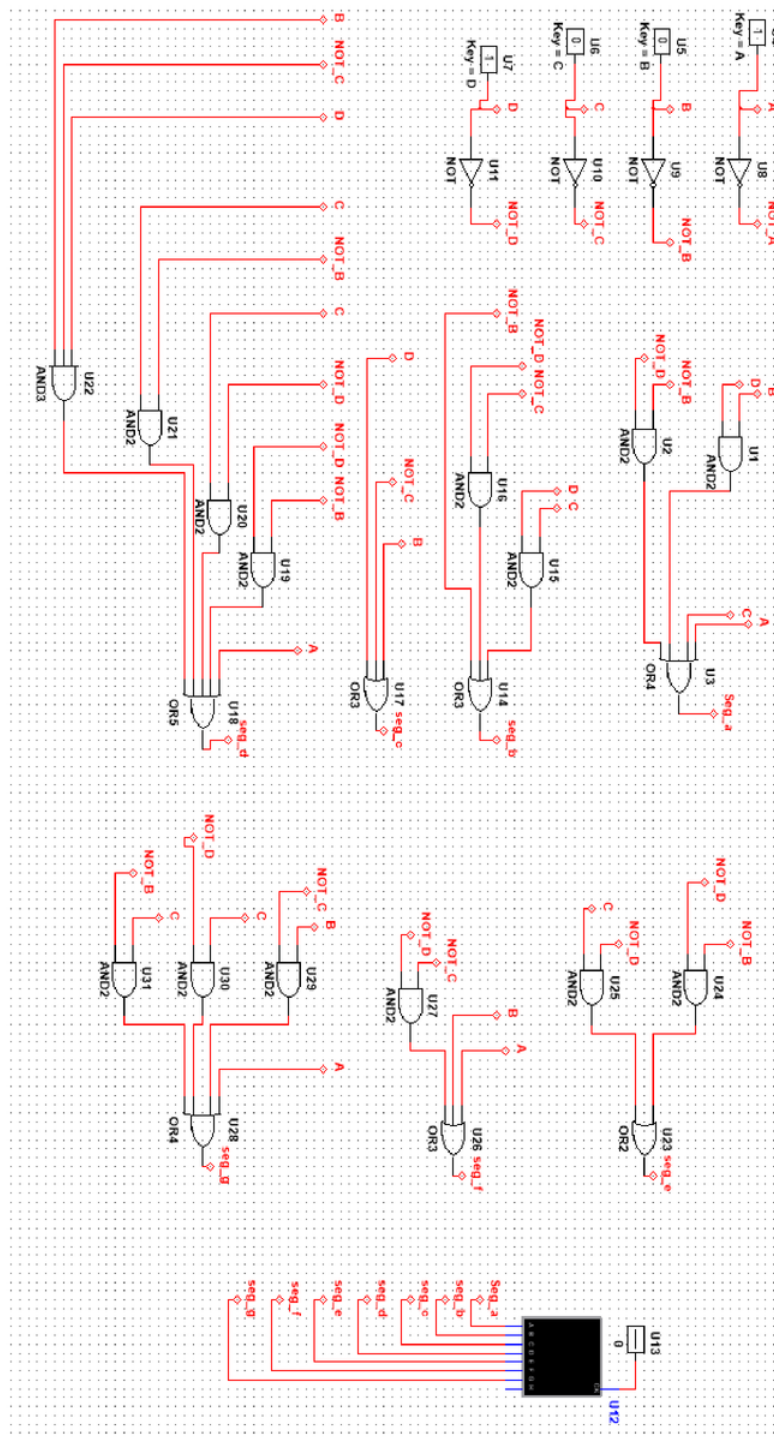


Figure 28: Decade 7 Segment display and clock with switches for testing

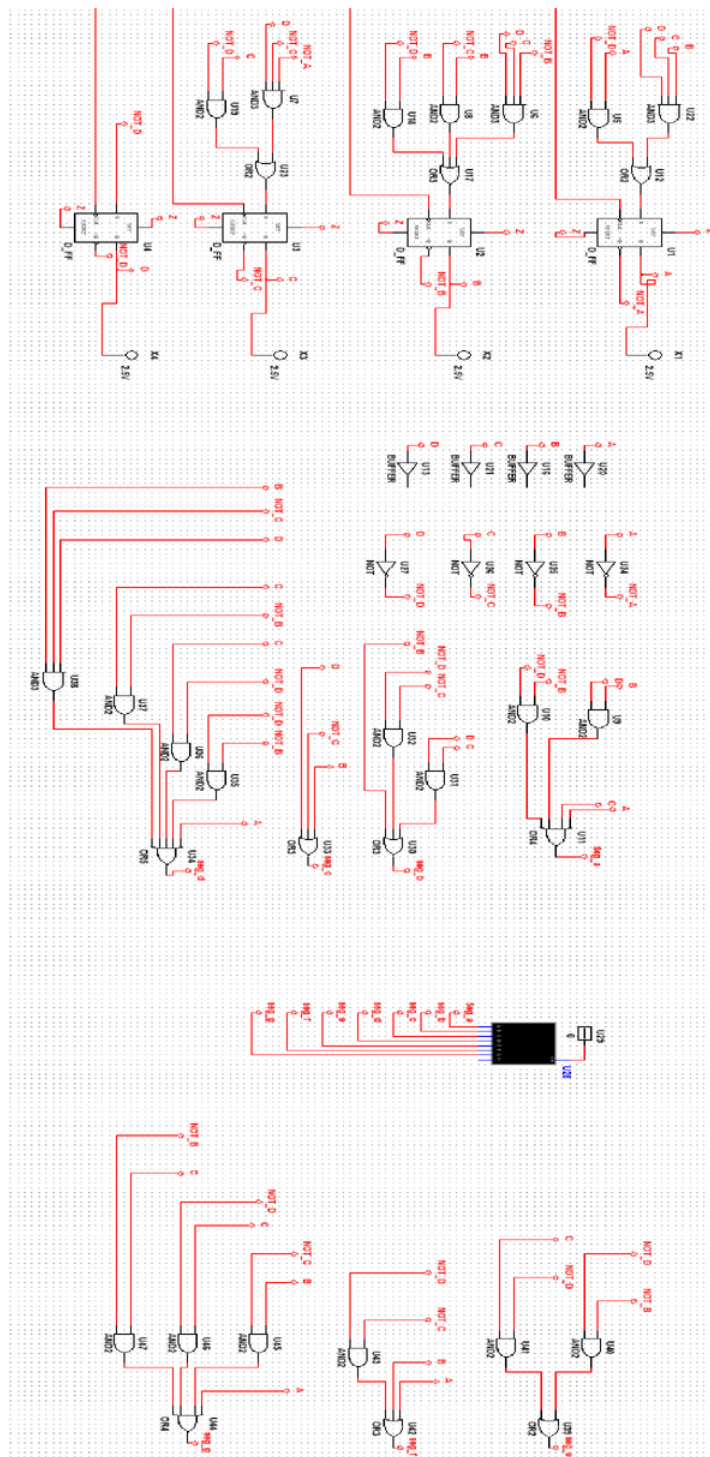


Figure 29: Combined Decade Counter and Decade Display

Decoders

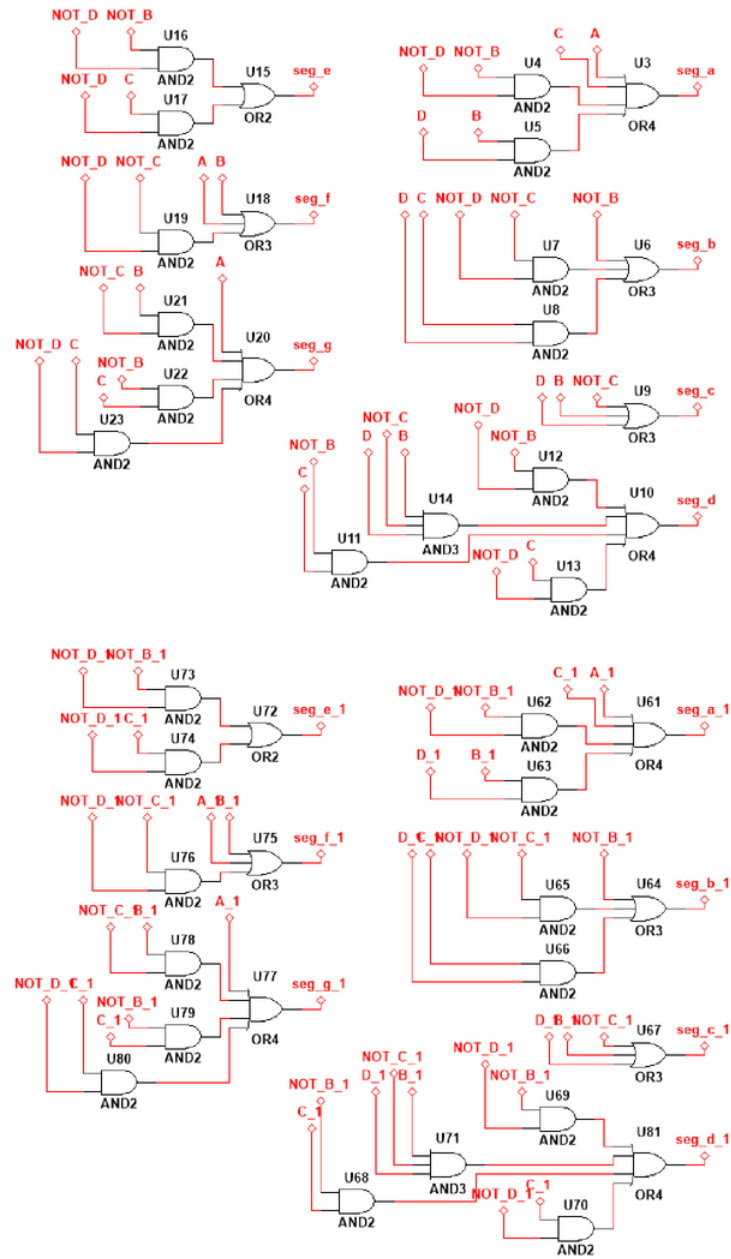


Figure 30: Decoder

Combining the 0-5 counter and the 0-9 counter to make the stopwatch

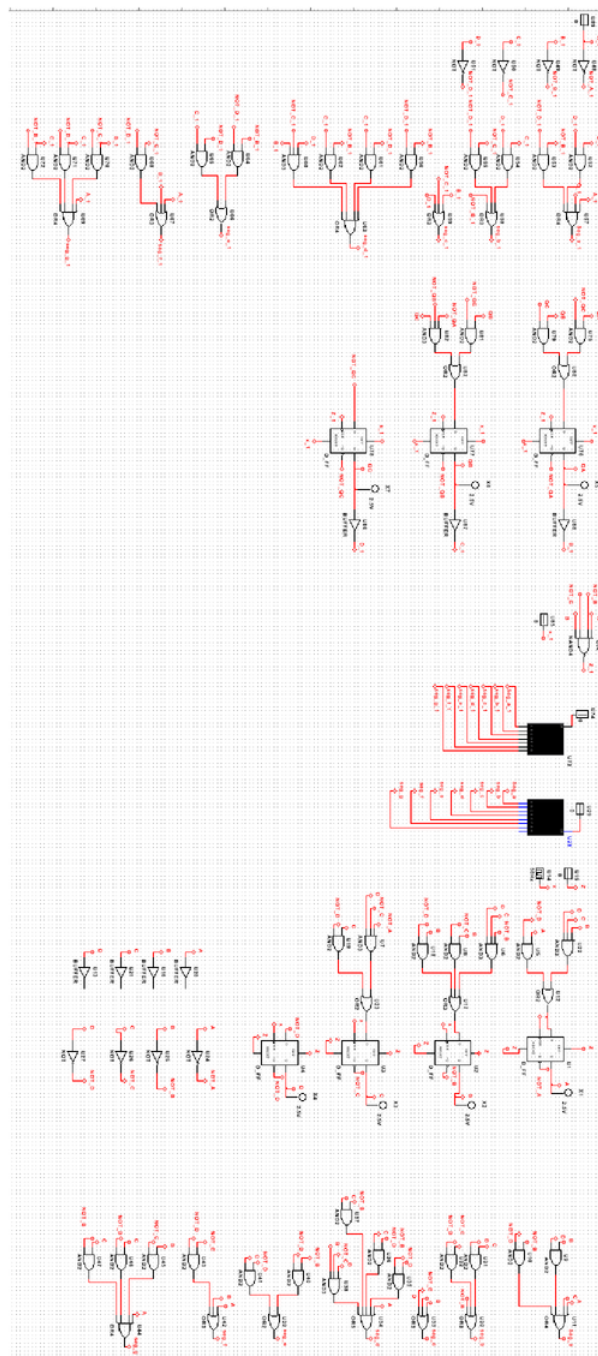


Figure 31: Combined circuit

The above circuits were then created in PLD Mode to allow testing of the individual portions of the circuit or the full circuit on the test board. The counters were created and testing using a logic analyser before combining them into a final combined circuit.

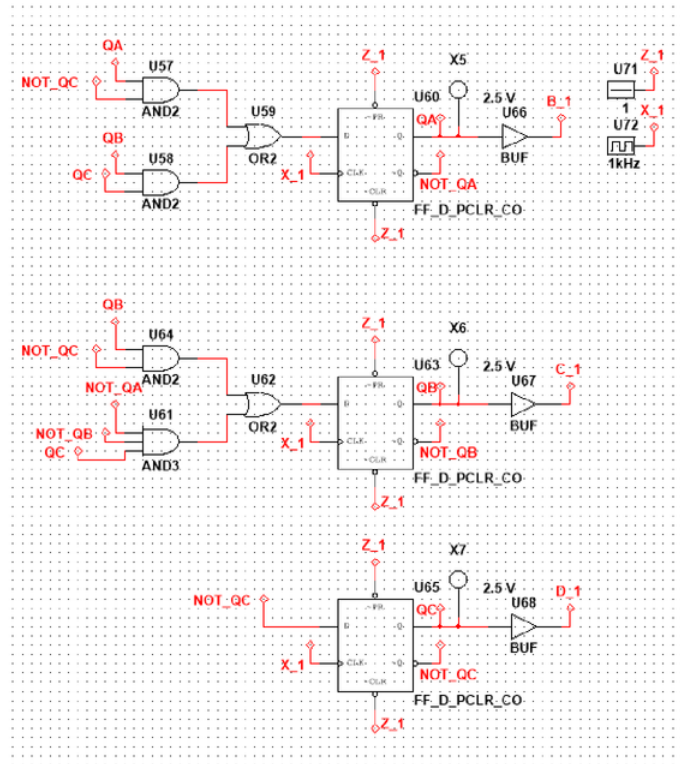


Figure 32: 0-5 Counter in PLD mode

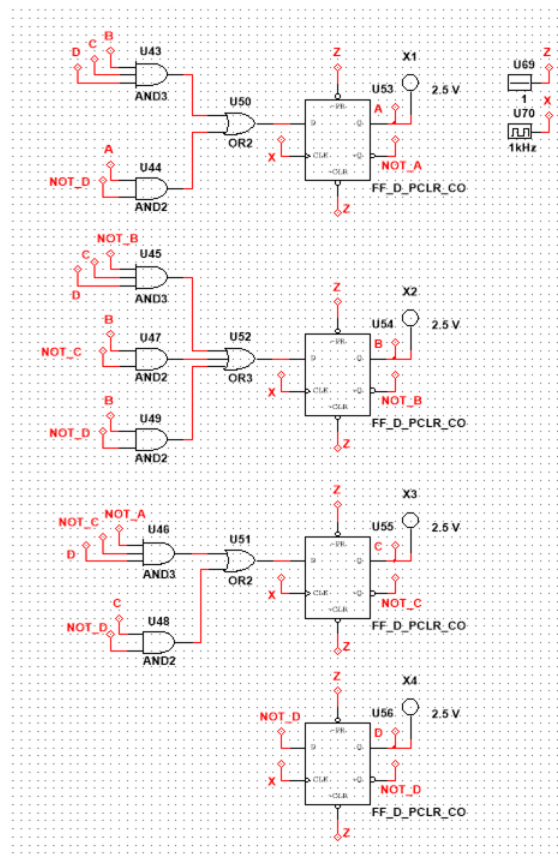


Figure 33: 0-9 counter in PLD mode

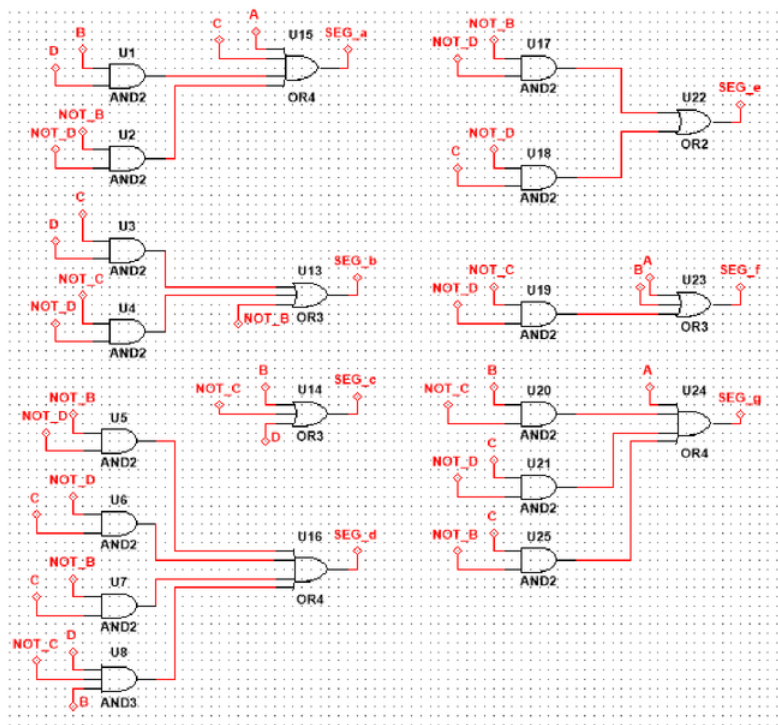


Figure 34: PLD Decoder



Figure 35: PART 1 of combined PLD circuit (split into two parts for screenshot)

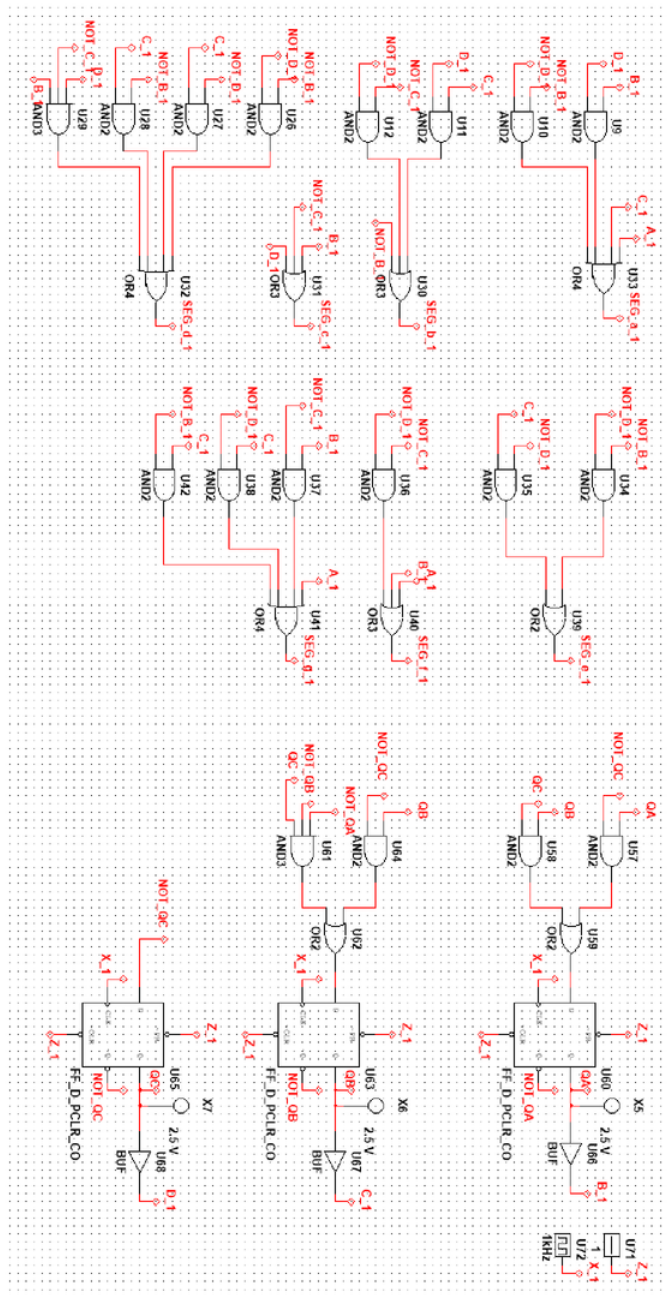


Figure 36: PART 2 of combined PLD circuit (split into two parts for screenshot)

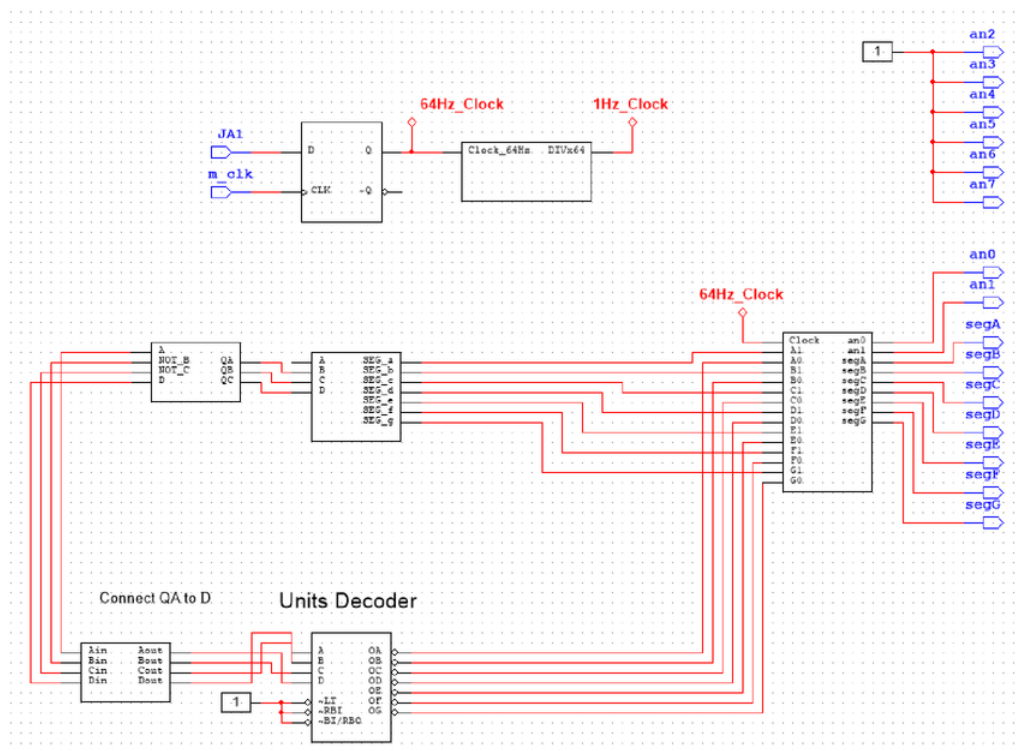


Figure 37: Final Design in PLD mode for Nexys testing board

4. Analysis of results

The MultiSim simulations were tested using the 'Run Simulation' feature in MultiSim.

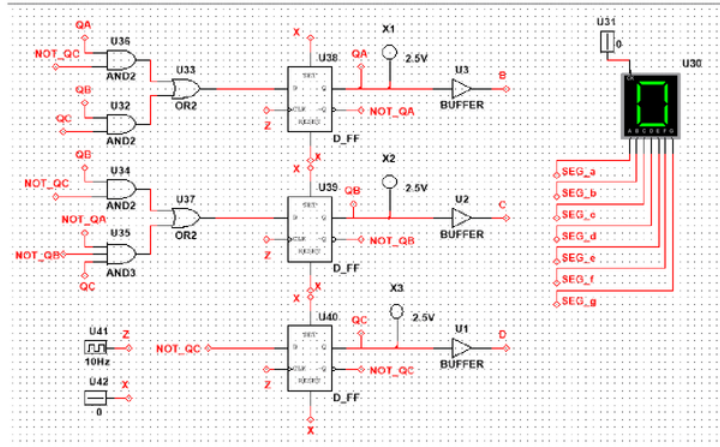


Figure 38: Testing Simulation 0-5 counter

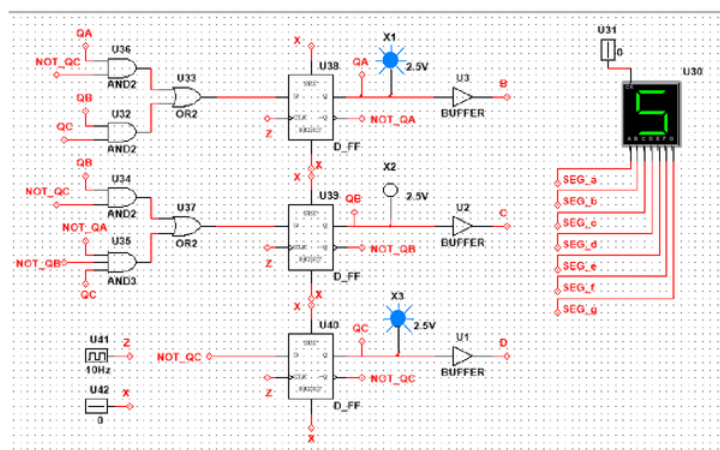


Figure 39: Simulation testing for 0-5 Counter

The above screenshots show evidence of the 0-5 counter working as intended. The reason for testing each section before combining it allows any errors to be corrected before having to fault find on a large circuit.

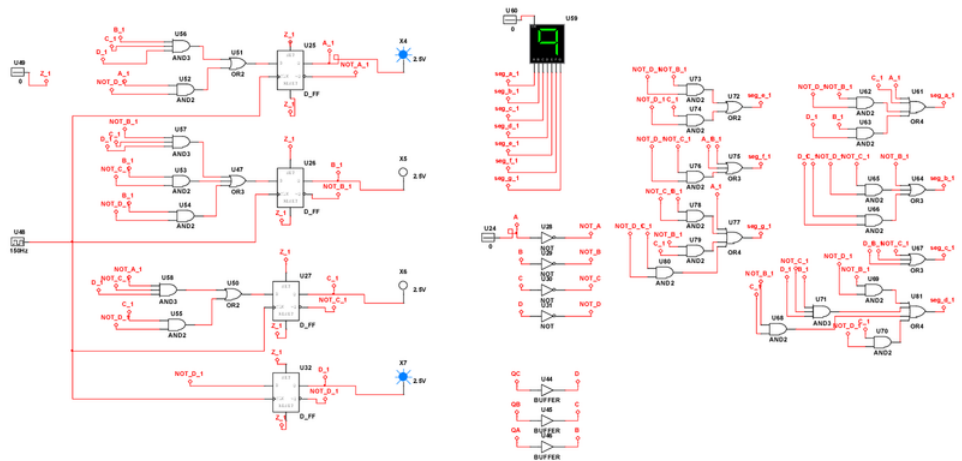


Figure 40: Simulation testing for 0-9 counter

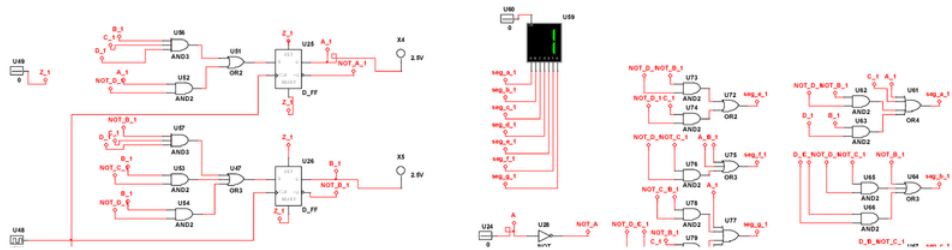


Figure 41: Simulation testing for 0-9 Counter

The same simulation was tested with the 0-9 counter, ensuring the count reaches 9 and then resets to 0.

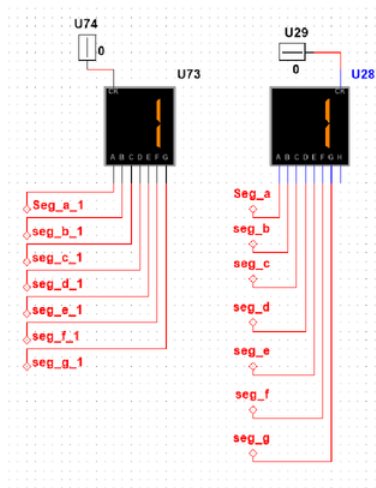


Figure 42: Combined circuit simulation testing

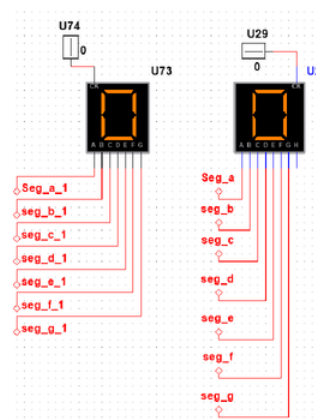


Figure 43: Combined circuit simulation testing

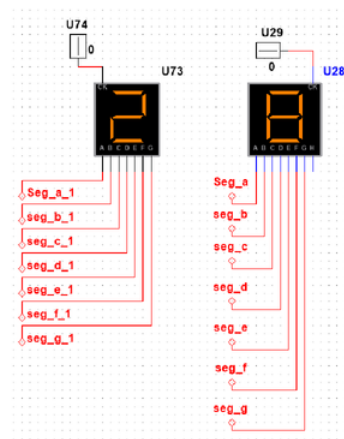


Figure 44: Combined circuit simulation testing

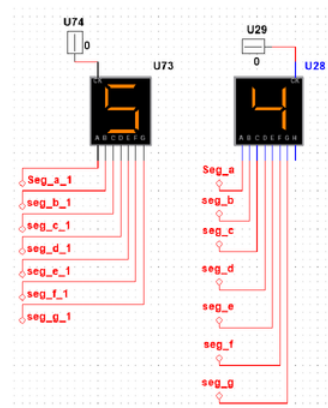


Figure 45: Combined circuit simulation testing

The final combined circuit was then tested. The combined circuit has 2 displays one for the units and one for the tenths. These screenshots are evidence of the stopwatch working as intended. The units count to 9 and every time 9 is produced the 0-5 counter gains a count. This carries on until 59, where the count is then reset to zero (00). Testing covered the full range of count to ensure the reset was carried out.

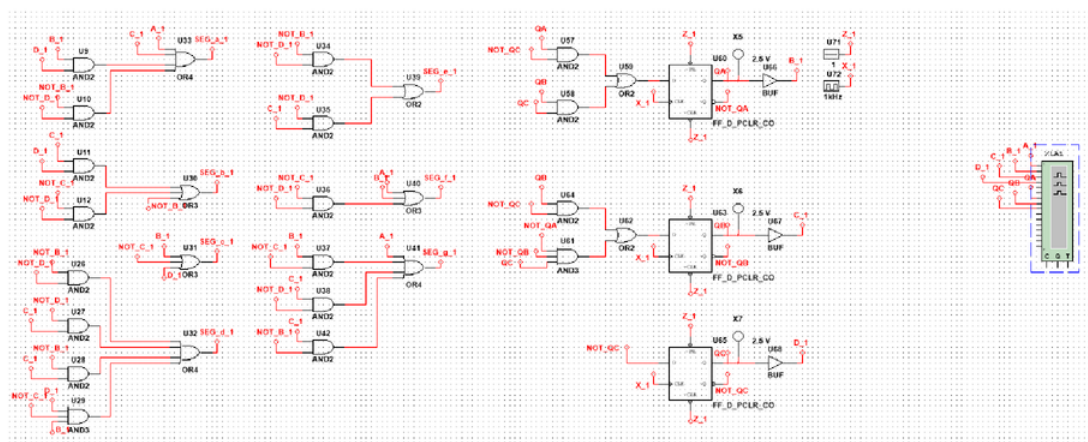


Figure 47: Logic Analyser for 0-5 counter in PLD mode

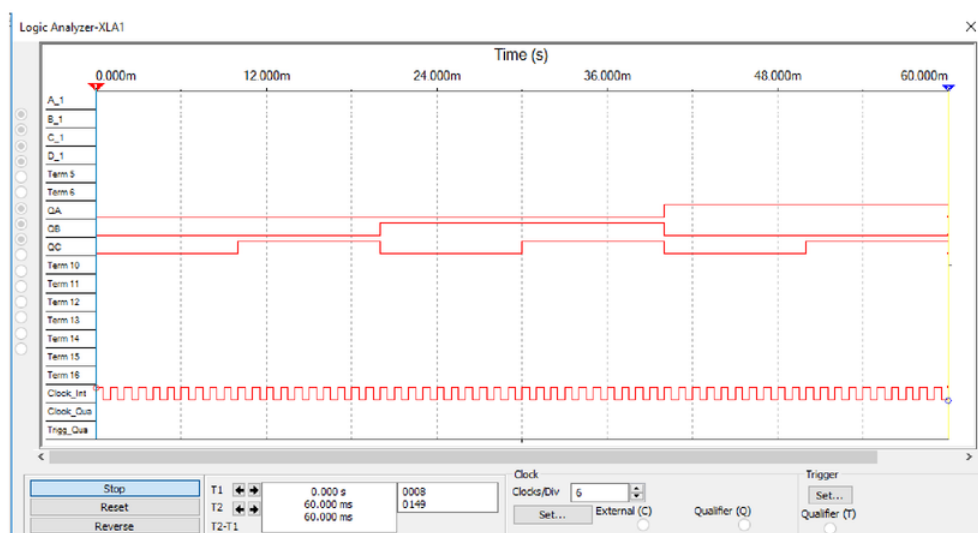


Figure 46: Logic analyser for 0-5 counter in PLD mode

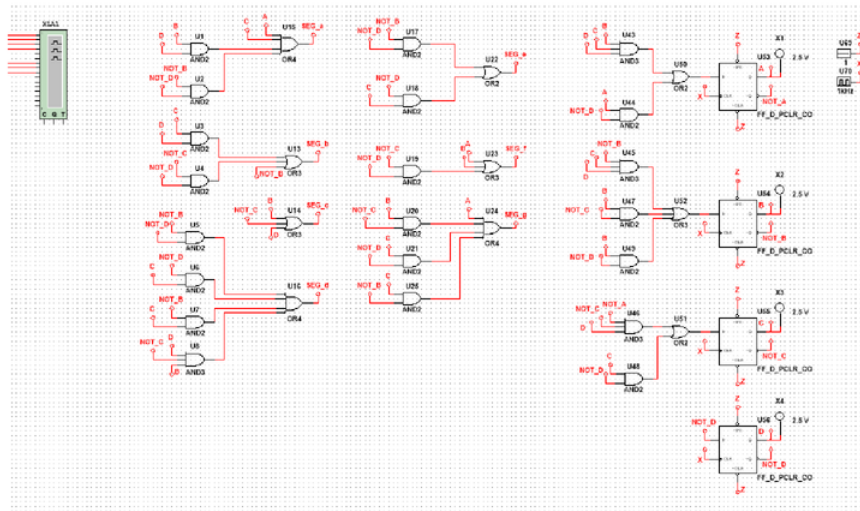


Figure 48: Logic Analyser for 0-9 counter in PLD mode

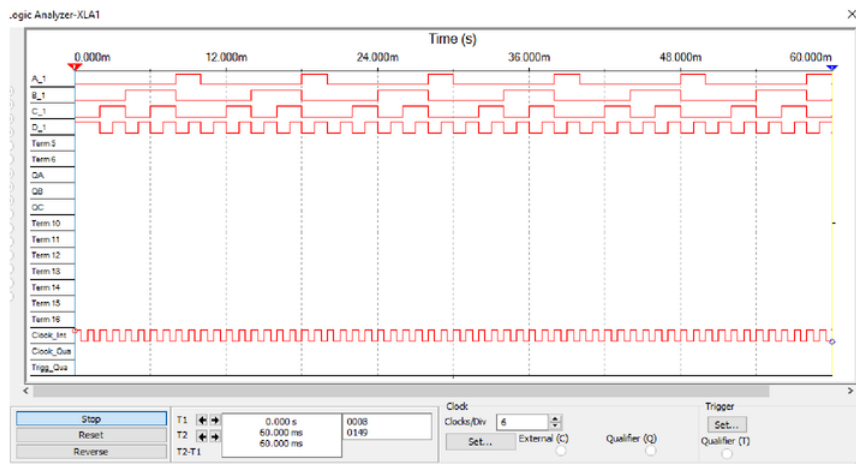


Figure 49: Logic Analyser for 0-9 counter in PLD mode

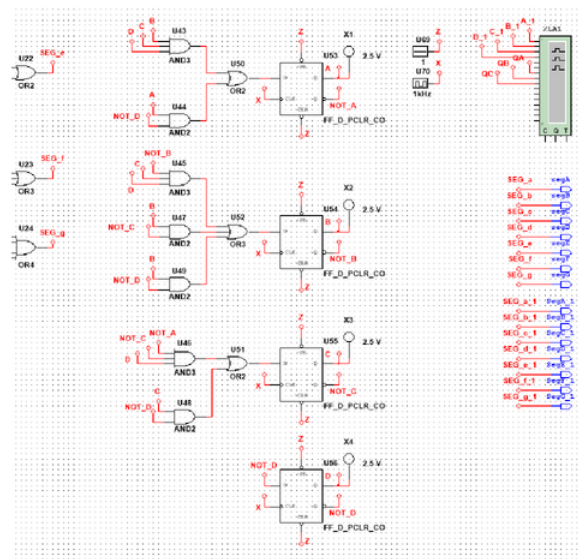


Figure 50: Snippet of final combined circuit with logic analyser configuration (PLD)

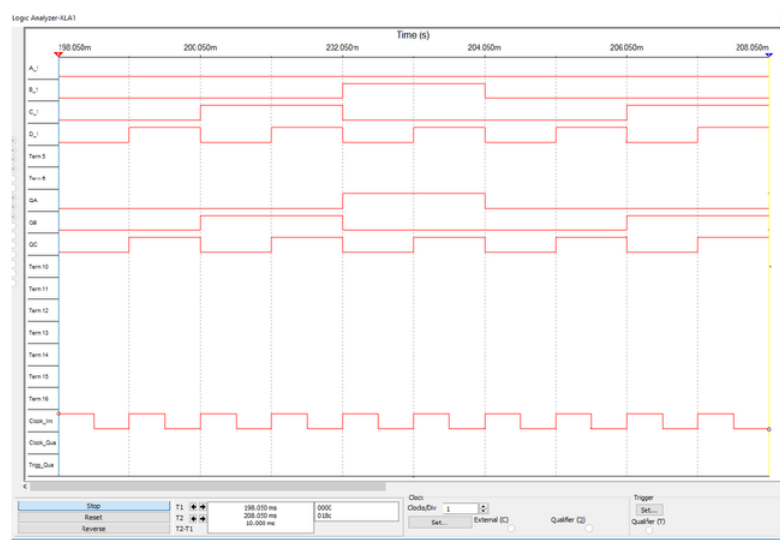


Figure 51: Logic Analyser for combined circuit in PLD mode

Once PLD testing was complete the program was transferred to the FPGA boards for testing. This is downloaded from MultiSim direct to the board. There is also a function generator connected to the test board for the frequency supply. Evidence of the boards operation is shown below. As intended the count reaches 59 then resets to 00.

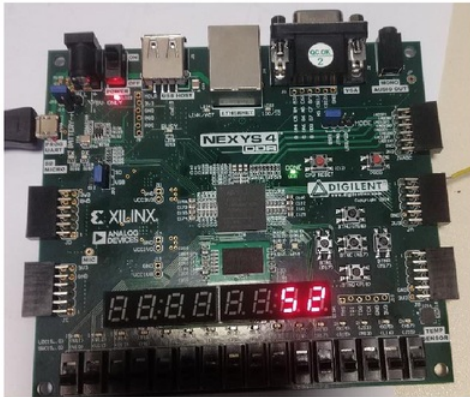


Figure 53: FPGA board testing

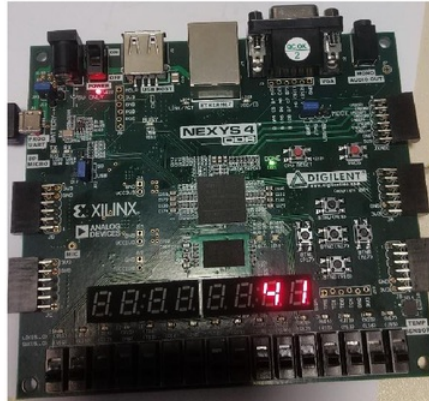


Figure 52: FPGA board testing

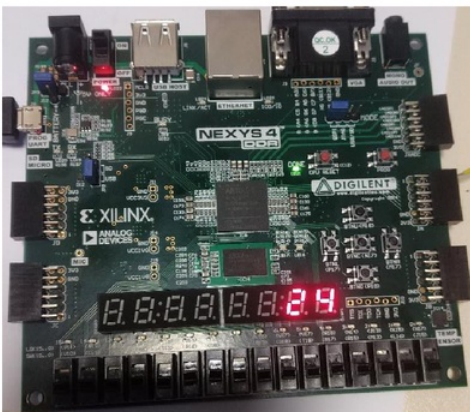


Figure 55: FPGA board testing

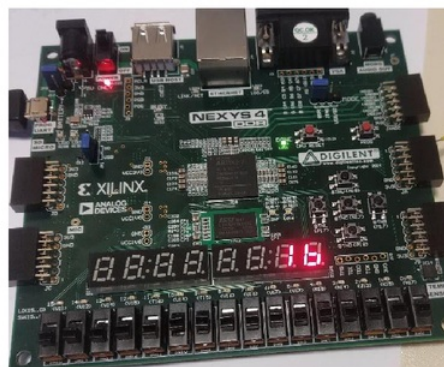


Figure 54: FPGA board testing

5. Conclusions

The assignment criteria was to create a stopwatch that counted to 59 then reset. The criteria was met and the stopwatch was created as proposed in the specification. The counter reaches a count of 59 before resetting to 00. Upon reaching 00, the count starts again and counts toward 59. Both the simulation and the FPGA testing achieved this result. The design portion of the assignment produced accurate information through the use of Karnaugh maps creating a formula for the simulation. The simulation testing provided evidence that the formulas created were correct as the 7 segment display had the correct numbers for both the 0-5 counter and the 0-9 counter. Any problems that arose were repaired and adjusted accordingly until the circuit had met the design criteria.

If there was more time, adding microseconds to the timer would have been a challenging task. There is also room to experiment with adding a minute and hour count which would have really finished off the stopwatch assignment bringing a more realistic real-world design specification in to it.

6. References

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Tyler Lloyd PSDE 4004 ASSIGNMENT 2

GRADEMARK REPORT

FINAL GRADE

GENERAL COMMENTS

Instructor

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GRADING FORM: CSG-RUBIC

TYLER LLOYD

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RESEARCH-INFORMED LITERATURE



There was evidence of extensive further reading and research from credible and reliable sources. Your interpretation and understanding of the additional research was very good and demonstrated a deep underlying appreciation of the subject. Your references were appropriate to the

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task and your reference list was of an appropriate length for this assignment.

KNOWLEDGE AND UNDERSTANDING



The knowledge and understanding of the subject demonstrated by this assignment was generally good. There were very few gaps in your knowledge of the basic principles and your understanding of the higher level concepts was demonstrated to a limited degree - you could have explained in more detail how the circuit evolved. The design process was well explained for the basic counters, but not for the decoder or the overall system.

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ANALYSIS



Your explanation of the design process was good, however the conclusions lacked some detail. You could have evaluated the use of the various components, specified whether the solution met the specification and suggested ways to improve the solution. You have however demonstrated good analytical skills and your approach to the task was logical. Further work – in your conclusion, you should relate the results to the original specification and to accepted theory.

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PRACTICAL APPLICATION AND DEP.



Your application of practical skills for this task was generally very good. You used the resources available in MultiSim appropriately when designing the circuit and you used appropriate options for testing and evaluating the circuit performance. You managed to design an efficient circuit that

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functioned within the specification and achieved this by only asking for assistance when appropriate. Your results were comprehensive and allowed for a good conclusion to be attempted.

SKILLS FOR PROFESSIONAL PRAC.



In this assignment you have demonstrated skills in working individually and also collaboratively. Your written report was very well structured and written in a coherent and logical way. The report was presented in a professional manner using appropriate language and formatting, good diagrams in appropriate places, good sentence/paragraph structure and clear calculations

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