

12 Pages

1. Please give the information requested in the boxes below.
2. Enter your name in the space provided to the right, fold over and seal down (using the label provided) to hide your name.
3. The answers must be legibly written. The Examiners can either ignore illegible script or have it typed and the expense of typing charged to the candidate.
4. Write your answers in ink.
5. Begin each answer on a fresh page. Do all rough work in the answer book and cross it through.
6. No part of this book is to be torn out; it must be handed in complete.
7. If more books than one are used, fasten them together using the tags available from the invigilator(s).
8. **Every book must be handed in. In no circumstances may answer books, used or unused, be taken out of the examination venue.**

1	Student Number	1909752
2	Title of Examination Paper	Elec Prod and test
3	Module Code	SGEE 6002
4	Date and Time of Examination	19/05/23 09:30 - 12:00
5	Examination Venue	
6	Seat Number	
7	Number of Answer Books handed in	

(Gweler yr ochr arall am y fersiwn Cymraeg)

List the numbers of the questions you have attempted	Office Use
2	25
3	5
1	16 1/2
Total	46 1/2

MARK
478 AG REED
470%

SURNAME: Rees

FORENAME(S): Jordan mark

(See the other side for English version)

7	Nifer y Llyfrau Atebion a gyflwynwyd	
6	Rhif Sedd	
5	Lleoliad yr Arholiad	
4	Dyddiad ac Amser yr Archoliad	
3	Cod y Modwl	
2	Titl y Papur Arholiad	
1	Rhif Myfyriwr	

[illegible]

3. Rhaid i'r atebion fod mewn llawysgriften ddarllenadwy. Gall yr Arholwyr naill ai anwybyddu sgript annarllenadwy, neu drefnu iddi gael ei theipio a chael yr ymgeisydd i dalu.
4. Ysgrifennwch eich atebion mewn inc.
5. Dechreuwch bob ateb ar dudalen newydd. Gwnewch unrhyw fras nodiadau yn y llyfr atebion a thynnu llinell drwyddynt.
6. Ni ddylid rhwgo unrhyw ran o'r llyfr hwn; rhaid ei gyflwyno yn gyfan.
7. Os defnyddir mwy nag un llyfr, rhwymwch hwy gyda'i gilydd gan ddefnyddio'r tagiau sydd ar gael oddi wrth y gwyllwyr/gwylywr.
8. Rhaid dychwelyd pob llyfr. Ni chaniateir mynd â llyfrau atebion, wedi eu defnyddio neu heb eu defnyddio, allan o'r lleoliad arholi o dan unrhyw amgylchiadau.

1. Rhwch yr holl wybodaeth y gofynnir amdani yn y blychau isod.
2. Rhwch eich enw yn y lle a ddarparwyd ar y dde, plynwch ef a'i selio i lawr (gan ddefnyddio'r label a ddarparwyd) i guddio'ch enw.

Cyfarwyddiadau i Ymgeiswyr

12 Tudalen

Llyfr Atebion Arholiadau



Prifysgol Cymru
Y Prifodol Dewi Sant
University of Wales
Trinity Saint David

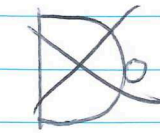
Llenwch, plygwch a seliwch
(gweler nodyn 2 isod)

CYFENN:

ENW(AU) CYNTAF:

2
6

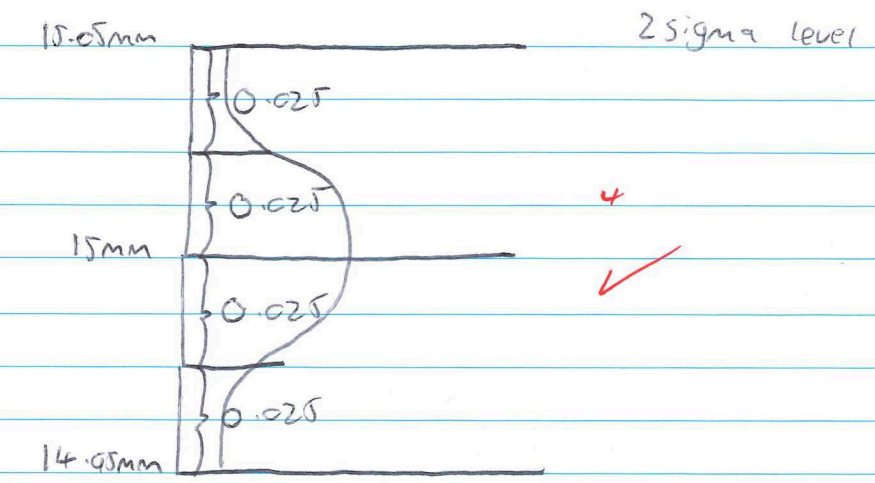
3 input NAND



2

a)

i) $STD = 0.05 \div 2 = 0.025$ ✓ 2



ii)

2 sigma

$STD = 0.025$

$CP = (\text{upper limit} - \text{lower limit}) \div (6\sigma)$

$= (15.05 - 14.95) \div (6 \times 0.025)$

$CP = 0.6$ ✓ 3

CP < 1 therefore not capable

3 sigma

$STD = 0.05 \div 3 = 0.0166$

$CP = (15.05 - 14.95) \div (6 \times 0.0166)$

$CP = 1$

CP = 1 therefore capable ✓ 2

At the 2 sigma level the process is not capable because CP < 1 at sigma level 3 the process is capable because CP = 1

A recommendation would be to increase the sigma level so that the CP increases below the minimum. ✓

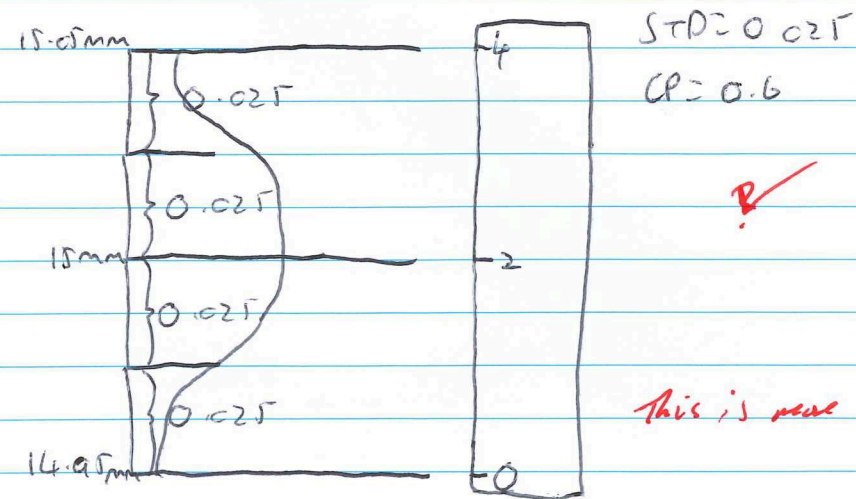
iii) Six sigma is basically a ~~process~~ quality ~~process~~ control process where sigma is the statistical measure of variability in a process and six sigma is the required standard deviation to be at least one-twelfth of the allowable spread. That is six times the standard deviation either side of the mean. ✓

If 6σ fits in the upper and lower side of the mean it is said to be capable if not it is said to be not capable. (3) ✓

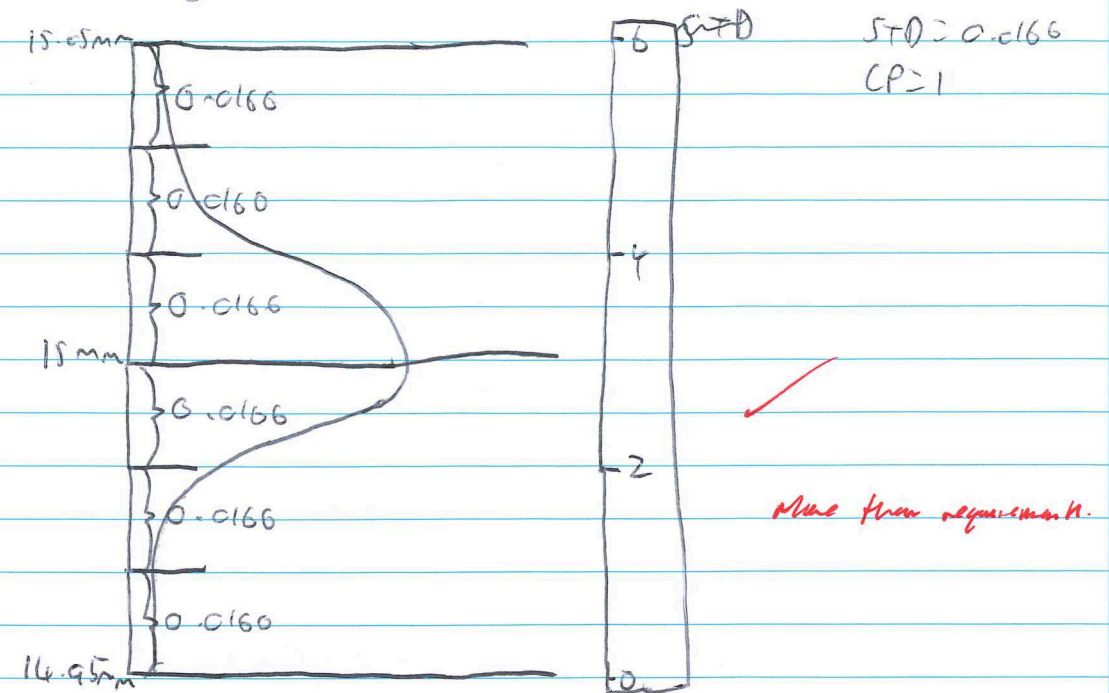
b) ~~4 sigma level~~

i) ~~$STD = 0.05 \div 4 = 0.0125$~~

2 sigma level



3 sigma level



b) 4 sigma level

$STD = 0.05 \div 4 = 0.0125$ ✓

upper limit = 15.05, 15.0375, 15.025, 15.0125 ✓
lower limit = 14.9875, 14.975, 14.9625, 14.95 ✓

ii) $CPK = \min \left(\frac{\text{mean} - \text{lower limit}}{3\sigma}, \frac{\text{upper limit} - \text{mean}}{3\sigma} \right)$ ✓

$= \min \left(\frac{15.02 - 14.95}{3 \times 0.0125}, \frac{15.05 - 15.02}{3 \times 0.0125} \right)$ ✓

$CPK = \min (1.86, 0.8)$ ✓

iii) ~~The CP value does not change because the STD does not change. No attributes in the CP calculation changes when there is a change in the mean.~~

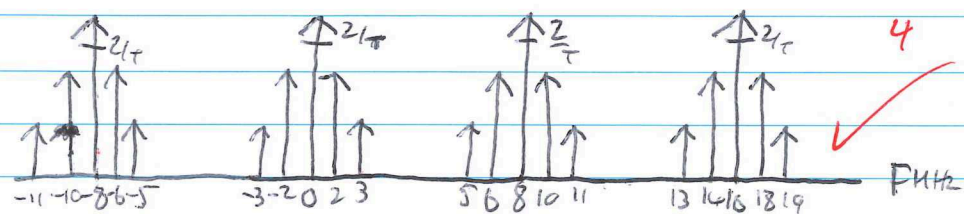
m)

ii) The 4 sigma Process is no longer Capable. According to the 3-sigma rule. the 3σ for the upper spec is 0.8 and the 3σ for the lower spec is 1.86. The 3σ rule either side of the mean must be ≥ 1 to be Capable if it is < 1 it is not Capable. ✓

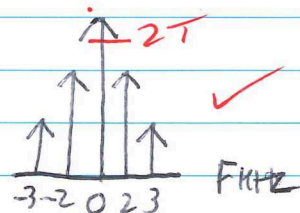
vi) The CP value does not change because the STD does not change. No attributes in the CP calculation changes when there is a change in the mean. ✓

Q3

a) $X(t) = \frac{2}{2} e^{-j\pi t} \times 3000t + \frac{4}{2} e^{-j\pi t} \times 2000t + \frac{2}{2} e^{j\pi t} \times 3000t + \frac{4}{2} e^{j\pi t} \times 2000t$ ✓



ii)



Continued

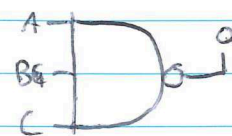
or b) i) The CPK value takes into consideration the change in the mean by comparing the 3σ rule at either side of the mean both sides of the mean must be ≥ 1 to be Capable. ✓

Q2 = 4 marks
Q3 = 5 marks.

Q1

b)

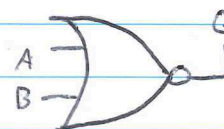
3 input NAND



Test No	A	B	C	Q
1	1	1	1	0
2	0	1	1	1
3	1	0	1	1
4	1	1	0	1

M+1 where M = number of test vectors. NAND gate exclusive output is ~~logic 0~~ logic 1. logic inputs set to logic 1. number of tests are reduced to reduce repeat tests. ✓

2 input NOR



Test No	A	B	Q
1	0	0	1
2	1	0	0
3	0	1	0

NOR gate exclusive output is logic 1 all inputs set to logic 0. ✓

c) Step 1: include ~~reduced~~ amount of test vectors in the Cb. M+1 where M = number of inputs. ✓

Step 2: Set the Propagation Path for the node and set up test vector. ✓

If the Propagation Path that carries the fault is a AND or NAND gate then set all required inputs apart from the one carrying the fault to logic 1. ~~the path that carries the fault~~ If it is a OR or NOR gate then set all inputs to logic 0. From node Z set inputs A, B, C through the NAND gate to logic 1. set inputs D, E through the NOR gate to logic 0. ✓

input F does not affect condition node Z as it goes into output node Qgood. The output for the NAND gate will be logic 0 and the output for the NOR gate becomes logic 1. If one of the inputs for the NAND gate becomes 1, then the condition of Node Z will change. Node X will become logic 1. This shows from the first table where ABC SA0 or Node X SA1. Node Z will follow the condition of node X which will affect the condition of Qgood.

d)
i)

Next st	Present State						Next state					
	A	B	C	D	E	F	A+	B+	C+	D+	E+	F+
	1	1	1	0	0	0	0	1	1	0	0	0
	0	1	1	0	0	0	1	0	1	0	0	0
	1	0	1	0	0	0	1	1	0	0	0	0
	1	1	0	0	0	0	0	0	0	1	0	0
	0	0	0	1	0	0	1	1	1	1	1	0
	1	1	1	1	1	1	1	1	1	1	1	1
	1	1	1	1	1	1	1	1	1	0	0	0

A+	ABC								
DEF	000	001	011	010	100	101	111	110	
000	0	0	1	0	0	1	0	0	
001	0	0	0	0	0	0	0	0	
011	0	0	0	0	0	0	0	0	
010	0	0	0	0	0	0	0	0	
100	1	0	0	0	0	0	0	0	
101	0	0	0	0	0	0	0	0	
111	0	0	0	0	0	0	1	0	
110	0	0	0	0	0	0	1	0	

$$A+ = DA = ABC.D.E + NA.B.C.ND.NE.NF + A.NB.C.ND.NE.NF + NA.NB.NC.D.NE.NF$$

B+

	ABC								
DEF	000	001	011	010	100	101	111	110	
000	0	0	0	0	0	1	0	0	
001	0	0	0	0	0	0	0	0	
011	0	0	0	0	0	0	0	0	
010	0	0	0	0	0	0	0	0	
100	1	0	0	0	0	0	0	0	
101	0	0	0	0	0	0	0	0	
111	0	0	0	0	0	0	1	0	
110	0	0	0	0	0	0	1	0	

$$B+ DB = A.C.ND.NE.NF + A.B.C.D.E + NA.NB.NC.D.NE.NF$$

C+

	ABC								
DEF	000	001	011	010	100	101	111	110	
000	0	0	1	0	0	0	1	0	
001	0	0	0	0	0	0	0	0	
011	0	0	0	0	0	0	0	0	
010	0	0	0	0	0	0	0	0	
100	1	0	0	0	0	0	0	0	
101	0	0	0	0	0	0	0	0	
111	0	0	0	0	0	0	1	0	
110	0	0	0	0	0	0	1	0	

$$C+ DC = A.B.C.D.E + A.B.C.ND.NE.NF + NA.B.C.ND.NE.NF + NA.NB.NC.D.NE.NF$$

Part correct. errors with single bit in tables

D+

	ABC							
DEF	000	001	011	010	100	101	111	110
000	0	0	0	0	0	0	0	1 ✓
001	0	0	0	0	0	0	0	0
011	0	0	0	0	0	0	0	0
010	0	0	0	0	0	0	0	0
100	0	0	0	0	0	0	0	0
101	0	0	0	0	0	0	0	0
111	0	0	0	0	0	0	0	0
110	0	0	0	0	0	0	1 ✓	0

$$D+ = DD = A \cdot B \cdot NC \cdot ND \cdot NE \cdot NF + NA \cdot NB \cdot NC \cdot D \cdot NE \cdot NF$$

$$+ A \cdot B \cdot C \cdot D \cdot E \cdot NF$$

E+

	ABC							
DEF	000	001	011	010	100	101	111	110
000	0	0	0	0	0	0	0	0
001	0	0	0	0	0	0	0	0
011	0	0	0	0	0	0	0	0
010	0	0	0	0	0	0	0	0
100	0	0	0	0	0	0	0	0
101	0	0	0	0	0	0	0	0
111	0	0	0	0	0	0	0	0
110	0	0	0	0	0	0	1 ✓	0

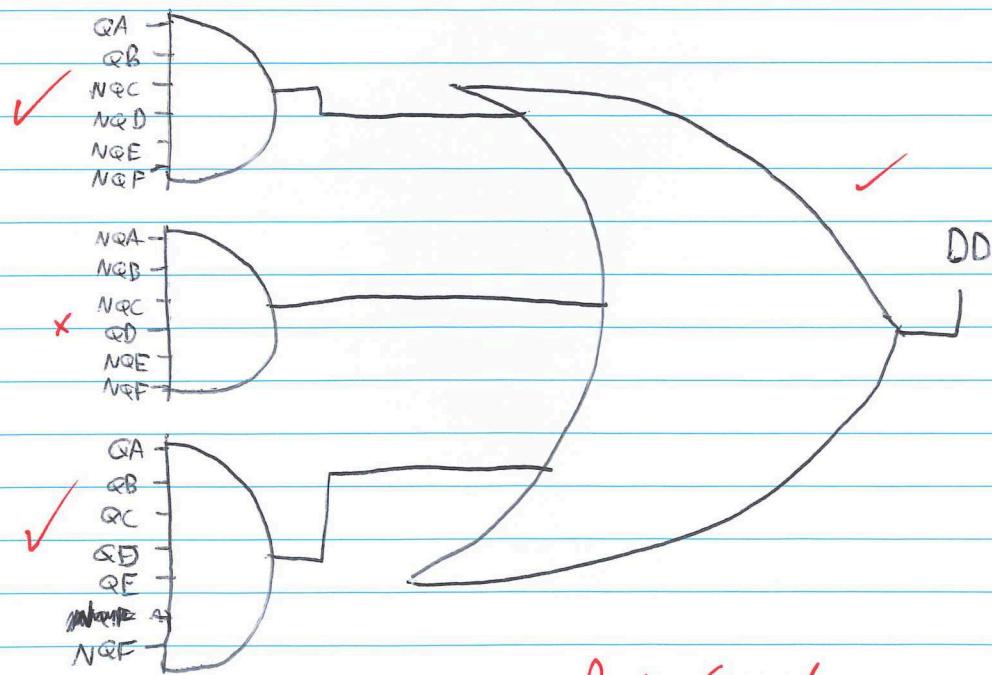
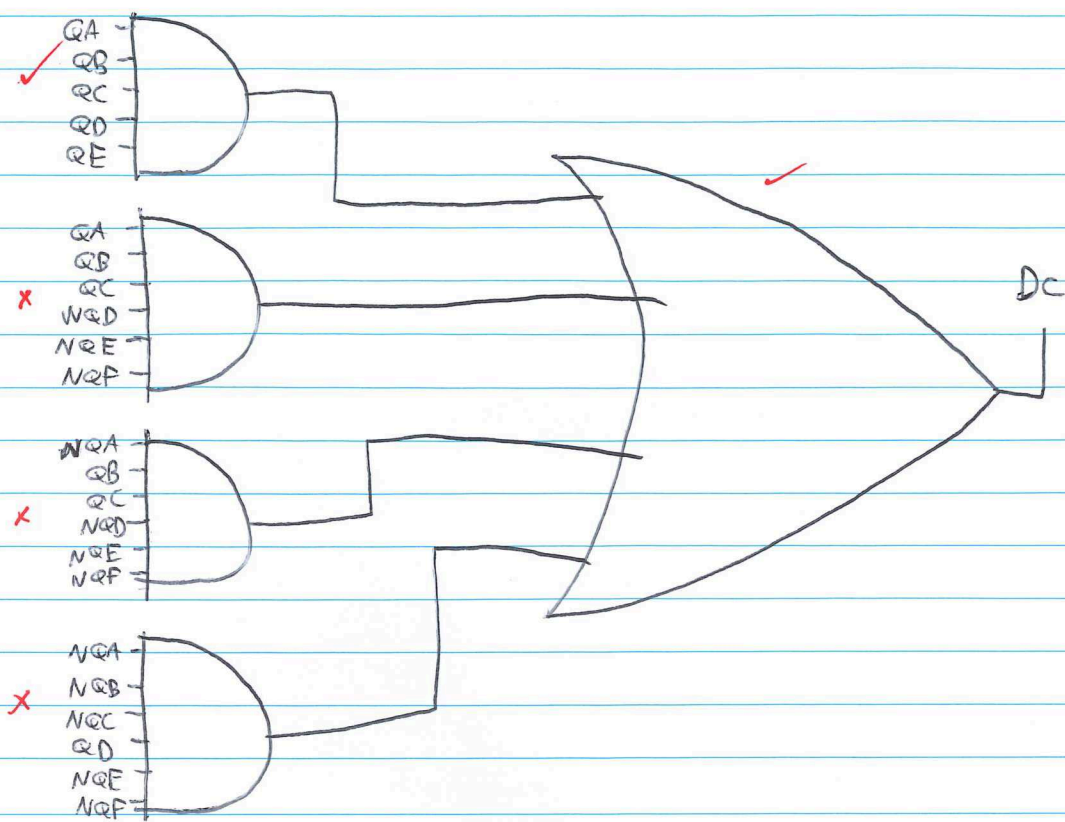
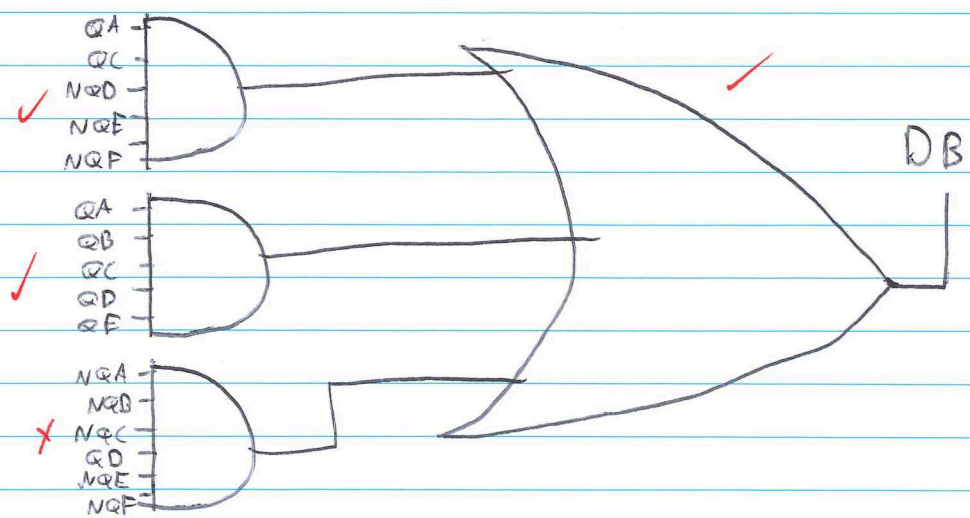
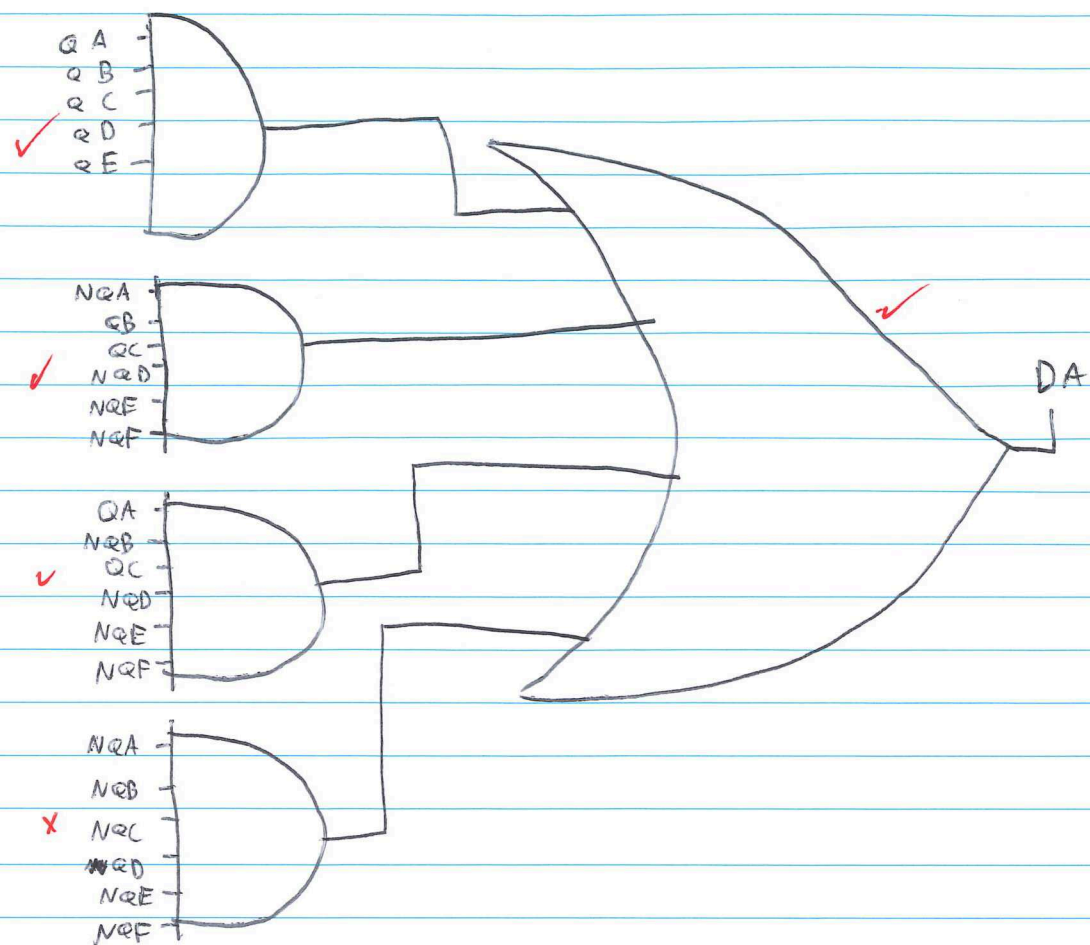
$$E+ = DE = NA \cdot NB \cdot NC \cdot D \cdot NE \cdot NF + A \cdot B \cdot C \cdot D \cdot E \cdot NF$$

error in E+ due to missing line in initial table!

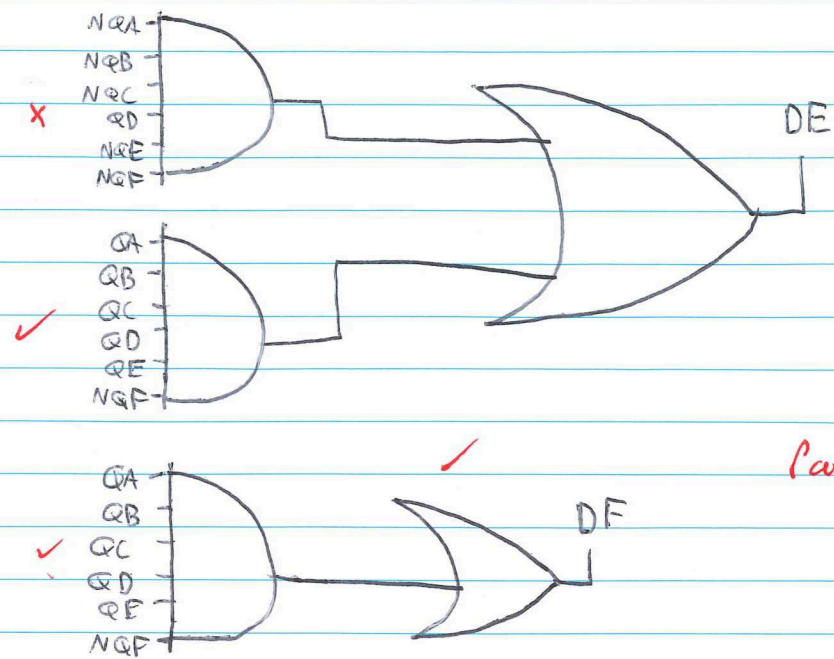
F+

	ABC							
DEF	000	001	011	010	100	101	111	110
000	0	0	0	0	0	0	0	0
001	0	0	0	0	0	0	0	0
011	0	0	0	0	0	0	0	0
010	0	0	0	0	0	0	0	0
100	0	0	0	0	0	0	0	0
101	0	0	0	0	0	0	0	0
111	0	0	0	0	0	0	0	0
110	0	0	0	0	0	0	1 ✓	0

$$F+ = FD = A \cdot B \cdot C \cdot D \cdot E \cdot NF$$



Partial correct



1/2

Part correct.

- ii) The CUT will run a reduced amount of test vectors. If there was a fault in the circuit ~~with~~ it is sent into an ex-or gate which acts as a comparator and will compare the output of the CUT with a ~~good~~ known good output source. If the circuit is under fault the ex-or will give a logic 1 output. ✓

3

3/3