



Prifysgol Cymru
Y Drindod Dewi Sant
University of Wales
Trinity Saint David

Examination Answer Books

12 Pages

Instructions to Candidates

1. Please give the information requested in the boxes below.
2. Enter your name in the space provided to the right, fold over and seal down (using the label provided) to hide your name.
3. The answers must be legibly written. The Examiners can either ignore illegible script or have it typed and the expense of typing charged to the candidate.
4. Write your answers in ink.
5. Begin each answer on a fresh page. Do all rough work in the answer book and cross it through.
6. No part of this book is to be torn out; it must be handed in complete.
7. If more books than one are used, fasten them together using the tags available from the invigilator(s).
8. **Every book must be handed in. In no circumstances may answer books, used or unused, be taken out of the examination venue.**

Complete, fold and seal
(see note 2 below)

SURNAME: Sayadi Choo bari

FORENAME(S): Iman

1	Student Number	P148275
2	Title of Examination Paper	
3	Module Code	
4	Date and Time of Examination	18.5.18
5	Examination Venue	
6	Seat Number	1
7	Number of Answer Books handed in	

List the numbers of the questions you have attempted	Office Use
Q1 a	44
s b	515
s c	—
Q2 a	66
s b	—
s c	66
Q3	1313
Total	34

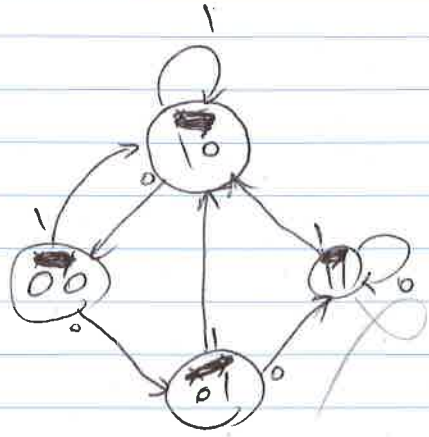
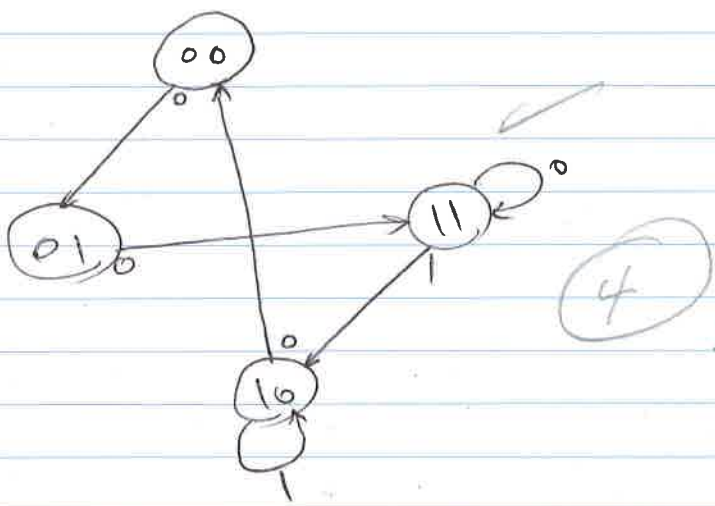
(Gweler yr ochr arall am y fersiwn Cymraeg)

Handwritten signature

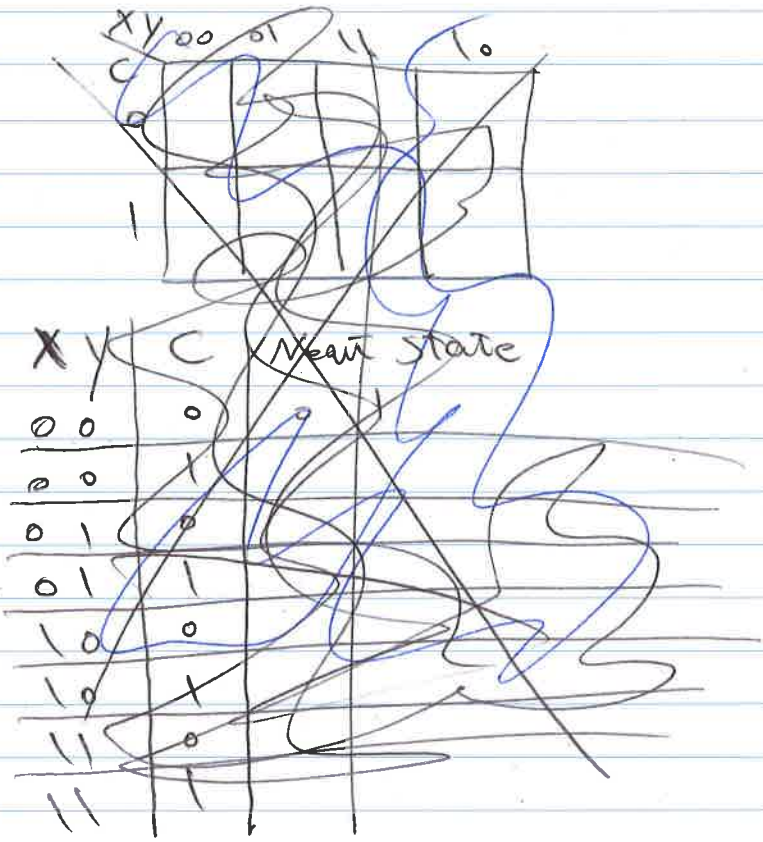
~~SUB~~

Q4

a) $csup = xy$
 $1 = 10$



b)



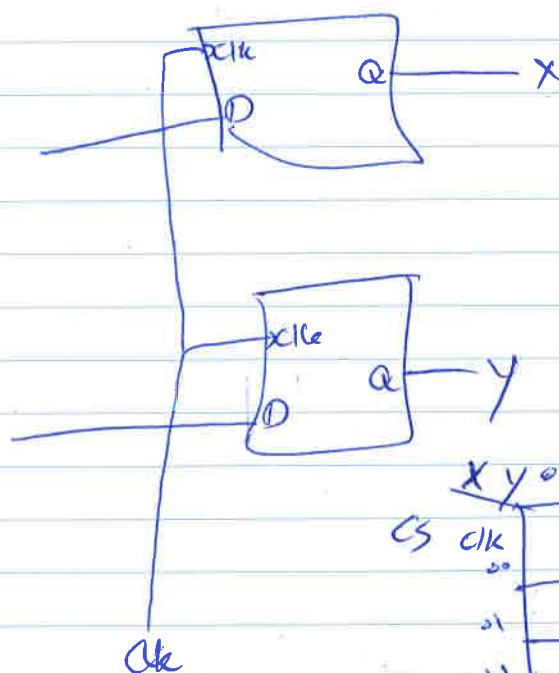
Question No.

Q1
b)

Present state Next state

A	B	C	X	Y
0	0	0	0	1
0	0	1	1	0
0	1	0	1	1
0	1	1	1	0
1	0	0	0	0
1	0	1	1	0
1	1	0	1	1
1	1	1	1	0

	CSup	CLK	X	Y
0	0	0	0	1
1	0	1	1	1
2	1	0	0	0
3	1	1	1	0



	X	Y	00	01	11	10
CS						
00						
01						
11						
10						

Q2
a)

	AB				
	00	01	11	10	
C					
0	0	1	1	1	
1	0	0	1	1	

$$B\bar{C}\bar{D} +$$

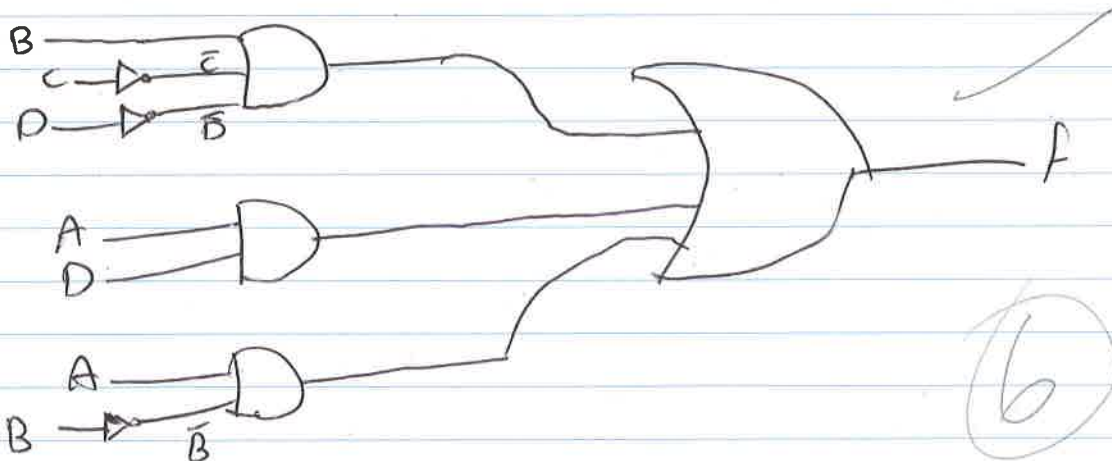
$$AD$$

b)

	AB				
	00	01	11	10	
C					
0	0	0	X	1	
1	0	0	0	1	

$$A\bar{B}$$

c) $F = B\bar{C}\bar{D} + AD + A\bar{B}$



```
1  -----
2  -- Company:
3  -- Engineer:
4  --
5  -- Create Date:    12:11:01 05/18/2018
6  -- Design Name:
7  -- Module Name:    Q3_Iman - Behavioral
8  -- Project Name:
9  -- Target Devices:
10 -- Tool versions:
11 -- Description:
12 --
13 -- Dependencies:
14 --
15 -- Revision:
16 -- Revision 0.01 - File Created
17 -- Additional Comments:
18 --
19  -----
20 library IEEE;
21 use IEEE.STD_LOGIC_1164.ALL;
22
23 -- Uncomment the following library declaration if using
24 -- arithmetic functions with Signed or Unsigned values
25 --use IEEE.NUMERIC_STD.ALL;
26
27 -- Uncomment the following library declaration if instantiating
28 -- any Xilinx primitives in this code.
29 --library UNISIM;
30 --use UNISIM.VComponents.all;
31
32 entity Q3_Iman is
33     Port ( x : in  STD_LOGIC;
34           CLK : in  STD_LOGIC;
35           y : out STD_LOGIC); x should be vector
36 end Q3_Iman;
37
38 architecture Behavioral of Q3_Iman is
39
40     type state_type is (state1, state2, state3, state4, state5, state6, state7,
41 state8);
42     signal present_state : state_type;
43     signal next_state : state_type;
44
45     begin
46         counter : process (x, present_state)
47         begin
48             if (x = '0') then
49                 case present_state is
50                     when state1 => next_state <= state1;
51                     when state2 => next_state <= state5;
52                     when state3 => next_state <= state4;
53                     when state4 => next_state <= state6;
54                     when state5 => next_state <= state6;
55                     when state6 => next_state <= state8;
```

```
56         when state7 => next_state <= state8;
57         when state8 => next_state <= state2;
58         when others => NULL;
59     end case;
60
61     else if (x = '1') then
62         case present_state is
63             when state1 => next_state <= state2;
64             when state2 => next_state <= state3;
65             when state3 => next_state <= state6;
66             when state4 => next_state <= state5;
67             when state5 => next_state <= state3;
68             when state6 => next_state <= state7;
69             when state7 => next_state <= state3;
70             when state8 => next_state <= state1;
71             when others => NULL;
72         end case;
73     end if;
74 end if;
75 end process counter;
76
77     clocked : process (CLK)
78
79     begin
80         if ((CLK = '1') and (CLK'last_value = '0')) then
81             present_state <= next_state;
82         end if;
83     end process clocked;
84
85
86 end Behavioral;
87
88
```

(13)