

Assignment 1

by Brian Jones

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Assignment 1

Electronic Production & Test

PSDE 6018
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With Rob Jenkins

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1 Introduction

1.1 Aims & objectives

Knowledge and skills will be tested through the undertaking of tasks designed to evaluate one's ability. The learning outcomes tested include for the evaluation & analysis to a range of manufacturing techniques. Printed circuit boards (PCB) and integrated circuits (IC) undergo stringent testing process which, because of the fast pace nature of the industry, are required to be automated, therefore, it is necessary to demonstrate an understanding of automatic test equipment (ATE).

As well as, and in connection with, ATE in testing PCB's & IC's, these manufacturing process, that are designed and prototyped to meet customer requirements, investigations into soldering techniques will be included. These investigations and research into simple 2-layer PCB design and soldering techniques will include SMT (surface mount technology) & PTH (Plated through hole) soldering processes.

Other investigations to assess learning outcomes will include research into AOI & AXI in the production process for automatic testing equipment. To show competency, it will be a requirement to investigate, design & test a set of pattern generators that will be used to test a prototype design. The use of CAD/CAM systems will be utilised to produce a PCB that will be used for the pattern generators.

2. Research

2.1 SMT & PTH, PCB technologies

Surface mount technology (SMT) is an efficient method used to mount surface-mount devices (SMD) onto printed circuit boards (PCB). SMT is a widely used method of producing electronic circuits in large commercial amounts and although plated through hole (PTH) methods are still used, especially where budgets are tight, SMT presently has replaced through hole technology in most cases, although a combination of the methods is also used as SMT is not very effective at mounting larger components such as bulky transformers and/or heatsinks. Wakerly states that *"Most of the components in modern PCBs use surface mount technology (SMT)"* (2013, p. 16).

The benefits of such technologies allow for the mass production of electronic circuits, but this ultimately leads to a greater number of defective PCBs as the miniature and more densely packed boards are at a greater risk of imperfections. The faster method of producing electronic circuits, SMT uses smaller components than through hole methods, components with small to no leads at all.

According to Williams (2005), there are two main ways of mounting components onto electronic circuit boards and they are, as previously mentioned, surface mount and through hole. The difference being, SMD's using the surface mount technology have termination areas rather than leads and are held in place only by solder between pads on the board and their terminations. Lead wires are used for through hole, taken through holes in the board.

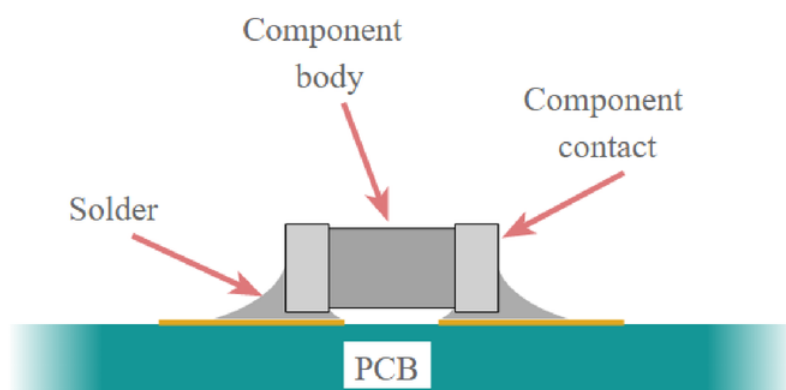


Figure 1: This shows the method of mounting SMD's onto PCB's using SMT. (Electronic Notes, 2013)

According to Wakerly (2013), multi-layered PCB's have their copper wire etching on thin fibreglass laminates layered into a single board of around 1/16 of an inch thick. The individual copper traces that makeup the wiring layout for connections are very narrow, typically 10 to 25 mils (a mil is 1/1000 of an inch) in most PCB's. More layers are required when PCBs are more tightly pack. The average fine-line board has copper traces of as little as 3-mil spacings and hence up to 166 connections can be made between adjacent traces.

SMT combined with fine-line PCBs and smaller and compact components, surface mount allows for the use of an automated processes for placement and soldering bringing significant improvements in reliability. This process also limits certain adverse analogue phenomena, such as speed of light limitations and transmission line effects. Unlike through hole methods, components of SMT, such as ICs and DIP packages are designed specifically to be placed onto the PCB. Before the placement of the components, a solder paste, which is a sticky mixture of powdered solder and flux, known as

reflow soldering, is applied to the location of the component on the board using a stencil whose hole pattern matches the contact pads. Either by hand or machine placed, the components are then fixed into position, held in place by the solder paste, the PCB is passed through an oven where the paste is melted fixing the components into permanent position (Wakerly, 2013).

The history of SMT was first developed in the 1960's with more progress made in the mid 80's and much more use in the 90's with IBM leading the way. This evolution allowed for the mass commercial use of automation to develop PCB's that meant that leads didn't have to pass through the boards but could be soldered straight onto the PCB.s. As a result, space could be saved by the development of purposely designed components and moreover both sides of the circuit board could be used more efficiently, hence cutting costs and reducing the size of the devices.

According to Landers (1994), technical challenges with the placement of active and passive electronic components differ between both SMT & PTH methods, a major difference is the way the components are attached to the board. PTH allows for a secure mechanical attachment prior to soldering while SMT does not. Challenges are also faced with the densely packed boards of surface mount and the constant necessity to reduce costs while increasing production and keeping high quality within the automated process of SMT.

Landers states that *"Relatively high costs, concerns about reliability, rework and field repair problems, and a lack of industry standardisation in component and process equipment have somewhat hindered adoption of SMT. However, the following advantages ensure that SMT will be a major component of the electronics packaging field for the foreseeable future"*. (1994, p. 265)

Components	Printed Circuit Boards	Assembly Process
Miniaturisation	Substantial size reduction	Replaces multiple machines (e.g. Axial, radial & DIP insertion)
Light weight	Hole drilling eliminated	Assembly speed & accuracy
Lead forming elimination	Lower power requirements	Mixed technology (SMD & PTH)
Packaging permits greater lead density		
Closer tolerances on electrical parameters		

Table 1: Advantages of SMT over PTH, PCB development.

For PTH, PCBs consist of one or more layer. Layers are created one at a time and then bonded together to create the final PCB stack with the most common stack being the 2-layer. This consists of

2 conductive sheets sandwiched either side of an insulated sheet. When more layers are required, manufacturers produce large 2-layer stock sheets and separate specific orders by cutting the orders, then, using the cuts, make up greater layer requirements as shown in the following Figure.

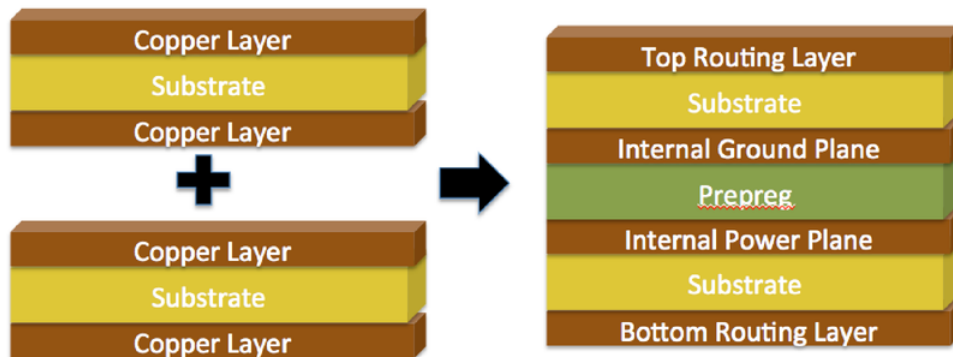


Figure 2: Example of PCB creation from stock materials. <http://www.bitweenie.com/listings/pcb-construction/>

It can be seen in the previous Figure, that the 2-layers are etched and cut-out then bonded together to make up a 4-layer structure. The middle layer is a non-conductive layer called the prepreg, this is a base laminate made up of materials such as woven glass cloth, paper, epoxy resin and fiberglass and is used to separate the layers. The laminations are then bonded under high pressure and heat after the interconnected circuitry is defined. Holes are then drilled before the board goes through a plating process to give a protective layer to the exposed copper surfaces and fill the holes that were previously drilled, finally a solder mask is added.

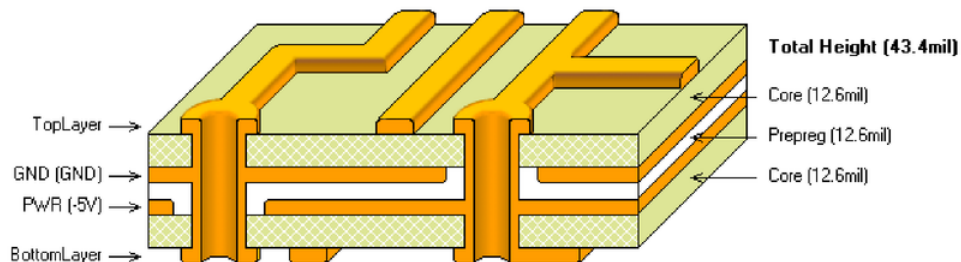


Figure 3: The basic structure of a PCB including the order of layers. <http://www.bitweenie.com/listings/pcb-stackup/>

Landers states that "Sizing of the boards is accomplished by shearing, sawing, routing, or using blanking dies. Process used to transfer images to the board are screen printing and photo-printing. Photo-printing can be further divided into wet-film and dry-film processes. Two other heavily used chemical processes are plating and etching. Prior to insertion of components, electrical testing of the board is performed". (1994, p. 168)

Research in this area is detailed.

So, to summarise, PCB design and construction techniques are set out in the following Table;

Construction, design and soldering techniques during printed circuit board process
o Layers created one at a time
o Individual pieces bonded together to form final stack
o 2 copper sheets laminated either side of substrate
o Larger stacks made up from 2-layer stacks
o Larger stacks made up by bonding either side of prepreg, with pressure and heat applied
o Holes are drilled including mounting holes
o Following holes being drilled, circuit board goes through plating process
o Solder mask is applied & any silk screening with client references applied
o Each PCB is unique and therefore the previous information is for standard methods
o Common 4 – layer stacks include two route layers & two internal planes, one for ground and one for power
o Three major types of PCB – single sided – double sided and multi-layer
o When single sided are overcrowded, double sided are used
o Double sided – electrical connections between circuits on each side are obtained by drilling holes through substrate and plating the inside of the holes with conducting material
o Multi-layered, substrate made up of layers, printed circuits separated by insulation. Components connected through holes drilled to appropriate circuit layer, thus simplifying circuit pattern
o Components, older through hole, thin wires or leads pushed through small holes in substrate and soldered to connection pads. Components held in place by gravity and friction between leads and sides of holes
o Components, newer surface mount, stubby J-shaped or L-shaped legs contact PCB directly. Held in place by solder paste (glue/flux) and solder applied at point of contact to hold components in place until solder or “reflow” in oven is melted
o Greater care required with surface mount, but, eliminates drilling process and consumes less space on PCB
o Computer aided design (CAD) used to design PCBs layout circuit patterns
o Hole locations or contact points for components laid-out by CAD software
o Information created by CAD is translated into instructions for a computer numerical controlled drilling machine or for automatic solder pasting machine used in manufacturing process
o Following circuit pattern layout, a negative image or mask is printed out onto plastic sheet. Negative images, areas in black not part of circuit pattern
o Most common substrate materials include glass fibre reinforced, epoxy resin with a copper foil bonded onto both sides, reinforced paper phenolic resin with a bonded copper foil

Table 2: Listed process of printed circuit board creation.

The reliability of a solder joint is assessed by both how well it bonds a component to the PCB conductive tracks and its ability to conduct electricity i.e. its electrical continuity between substrate and component. The contributing factors effecting qualities in the soldering techniques are the process and connection materials. Base metals i.e. the component leads and PCB conductive traces

along with solder fluxes and alloys that makeup the connection materials and how these materials are affected during the bonding process when thermal energy is being applied.

When using SMT, the most common method of bonding components to the PCB is “reflow soldering”. This method involves applying the solder paste, correctly positioning the devices and reflowing the solder in an oven, the oven is part of a conveyor system. Jointing is achieved as the reflow process melts the powder particles in the solder paste. During the cooling process, the solder solidifies, thus creating a potential strong bond. The principle process is split into four different processes and these include preheat, thermal sock, reflow and then finally cooling. The characteristics are identified in the following graph.

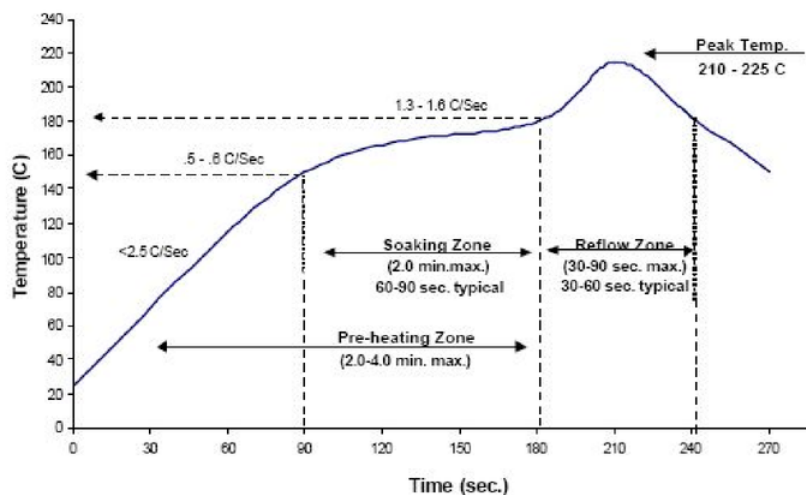


Figure 4: Reflow thermal characteristics. <http://www.instructables.com/id/Hack-a-Toaster-Oven-for-Reflow-Soldering/>

A method of soldering components to PCBs that is used for both SMT and PTH is “wave soldering”. This method is suitable for large scale processes that has in most cases been replaced by reflow soldering techniques except where larger components require attaching to the board. The wave soldering method utilises a tank that retains molten solder. The relevant method of attaching the components to the board for either SMT or PTH are undertaken, then, the loaded PCB is passed across a pumped wave of solder. The exposed parts of the PCB, not protected by a solder mask, receive wet solder to metallic areas of the PCB, thus creating a high-quality product that is superior to manual soldering.

Wave soldering is undertaken by various types of wave soldering machines, but, the principles are mostly the same. The process basically consists of three zones, fluxing zone, preheating and soldering zones. Dependant on the type of flux applied, a fourth zone where cleaning is undertaken can be added. The temperature/time characteristics can be seen in the following graph.

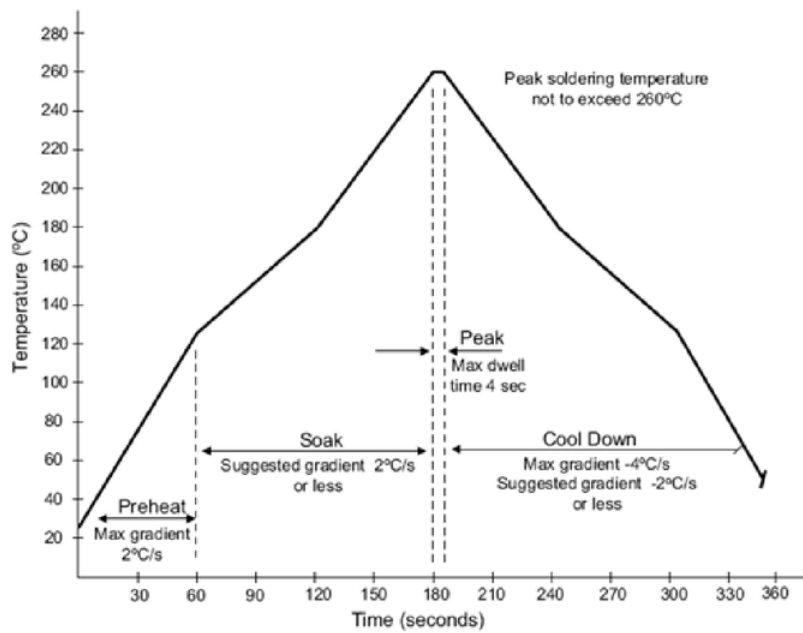


Figure 5: Thermal characteristics for wave soldering techniques. http://www.industrial-electronics.com/et-4e_15b.html

Good explanation of heat profiles for solder process.

2.2 AOI & AXI in the PCB production process for ATE

To prove the correct function of a PCB and its related components, testing is required. The method of testing should be known prior to completion of the finished PCB and test access points provided. Departments responsible for undertaking testing should already know if the testing will include manual function testing, in circuit testing boundary scan, functional testing on ATE (automatic test equipment) or a combination of these methods. (Williams, 2005).

ATE

The cost of producing a PCB design is increased by the time taken to test & verify the board and its components. This status is amplified as the production levels increase and therefore time saved by reducing test technician involvement to a minimum increases the profitability of the PCB. ATE allows the testing of PCB & related components to be undertaken very quickly thus increasing profits.

The initial cost of the automatic test equipment can be expensive and therefore a balance must be struck on whether it is a cost effective to have ATE or whether the testing of the PCB and equipment testing is more feasible using an experienced technician to perform testing. Experienced technicians will have a vast knowledge of the testing process and hence will understand common issues during

testing, but, as PCBs have become more complicated, manual inspection and testing has become complicated, inconsistent and unreliable, thus ATE has become the standard for pick and place PCB manufacturing.

There are many types of ATE approaches, all with their own advantages and disadvantages.

Understanding the type of systems is important when specifying the ATE to be adopted for an application, the type of testing required and what method is suited to a particular stage in production test cycles.

During the assembly of a PCB, a common first test is confirmation that a component has been properly inserted into the board and that the correct component values have been chosen. The quality of the solder joints, polarity, open & short circuits etc... must be confirmed during production as well as conformation the components haven't been missed out altogether during the automation process.

William states, "Automatic assembly is supposed to avoid such errors, but it is still possible to load the wrong component into the machine, or for components to be marked incorrectly. Automatic soldering has a higher success rate than hand soldering but bad joints due to lead or pad contamination can still occur." (2005, p. 300)

Types of automatic inspection & testing of PCB and equipment tests.
• AOI – Automatic Optical Inspection
• AXI – Automatic X-ray Inspection
• ICT – In-circuit Testing
• JTAG – Boundary Scan Testing
• Functional Automatic Test
• Combination Testing

Table 3: Types of automatic testing.

AOI: As PCBs become much more complicated and surface mount technology leads the way with automatic manufacturing processes of PCBs, automatic inspection has become more vital. During inspections, defects in the board such as surface defects, board dimensional defects, open & short circuits, missing components, thinning solder and misplaced components etc...are automatically identified during the automated inspection process. This inspection prior to it being automated was undertaken visually by trained technicians, but as would be expected, mistakes were made and much time was consumed.

According to Poole (2016), speed and accuracy as well as a much greater degree of repeatability is dramatically improved by AOI. Optical inspection techniques can be inserted into production lines, typically just after the soldering process. The PCB is automatically scanned visually by illuminating

the board with several light sources (either fluorescent, LED, infra-red or ultra violet) and a minimum of one HD camera (streaming video or still). An image of the board is built-up and then the picture is compared against information held on the board under inspection within the testing machine. Comparisons are made to indicate any defects or suspect areas within or on the PCB. Different techniques are used to identify defects including, template matching, pattern matching and statistical pattern matching.

Template matching uses a “golden board” to compare against the captured image. Pattern matching uses a known defective PCBs information and a known perfect PCBs information and compares the image against them to prove quality and statistical pattern matching is a statistical method of comparing against stored results of many failures and is thus able to accommodate minor acceptable deviations without flagging errors.

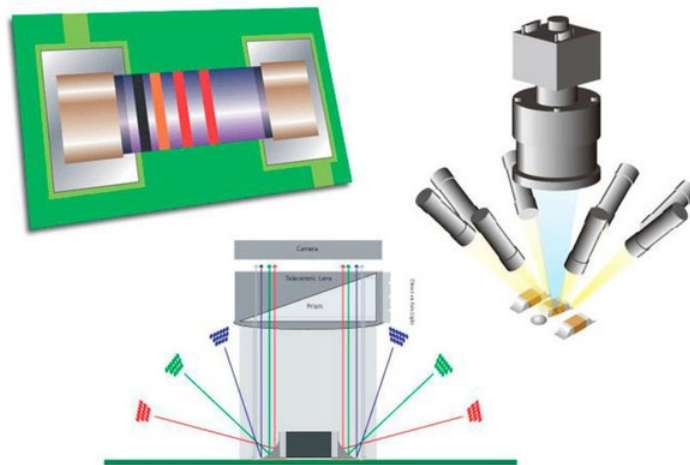


Figure 6: Automatic optical inspections using lighting and a HD camera, <http://interelectronic.com/products/automated-optical-inspection>

AXI: AS AOI is used to verify the visible joints of a PCB, a method is required to confirm the quality of non-visible joints. Some technologies have non-visible solder joints, such as “ball grid arrays”, “CSPs” and ICs and chip scale packages. The complexity of modern PCBs requires a greater method of confirming IC interconnections and solder joints. This is achieved by automated X-ray inspections which as well as checking the quality of solder joints and under solder joints, also checks for defects in the joints that may not be visible with standard optical inspection equipment.

According to Landers (1994), X-ray inspections are performed using an X-ray source and an image recording device. The PCB under inspection is placed between the X-ray source and recording device, the recording medium can be halide film. Digital X-ray images are displayed on a HD monitor

as data is directly fed into a computer. Scatter radiation produced when X-ray impinge upon an object is reduced by a technique known as reverse geometry X-ray.

A great benefit of AXI is that they not only perform two-dimensional (2D) inspections but also provide three-dimensional (3D) information that is available in machines that have, over the past few years, improved significantly in performance.

As with AOI, AXI would normally be placed after the soldering process during assembly production to monitor PCB defects. As well as having the ability of providing an internal view of a joint, hence spotting any voids under the solder joints, AXI can “see” through chips. Adjustments can be made in the assembly production as X-ray inspection detect any defects during assembly thus improving quality and keeping high standards of the automated production of PCBs.

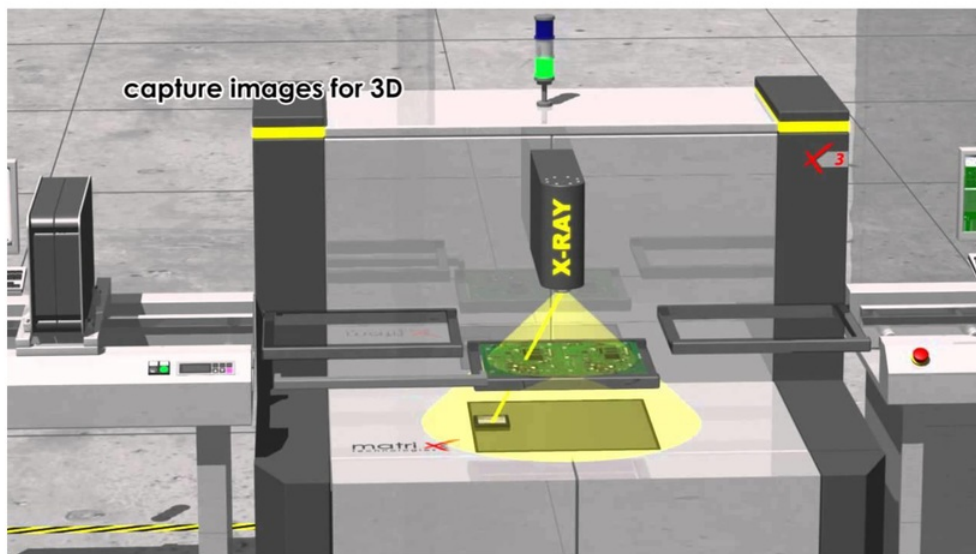


Figure 7: Automatic X-ray inspections using X-ray machines during production, <https://www.electronics-notes.com/articles/test-methods>

3. Multisim – Design, test & analysis

A variety of ATE for production industry is included and explained. Good effort.

This task involved, through using linear feedback shift register (LFSR) principles, creating a pseudo random pattern generator using computer aided design (CAD) techniques and by combining CAR (cellular automata register) rule 90 and rule 150 CAR. It was necessary to combine both CAR 90 & CAR 150, thereby creating a hybrid CAR 90/150, so that a maximum length binary output from the pseudo random pattern generator could be produced. The CAD software program National Instruments, Multisim.

A CAR system is implemented using flip-flops (FFs) whose present state determines the next state and as well as the previous state values of neighbouring FFs. The output of a particular FFs next value is the result of its present state and a result of its neighbouring left and right FF inputs. The FFs provide tap-offs that determine the number sequences generated and are connected through an XOR logic gate. The seed value is the initial value loaded into the LFSR and provides a maximum length value if $2^n - 1$ numbers are generated before the sequence is then again repeated.

Consequently, the LFSR is fixed at zero if the initial loaded seed value is also zero.

The way the connections are made can have the effect of reducing the output length of the pattern generator, this has been made apparent by Wolfram and is identified by considering XOR combinations of all 3-bit sequences. Wolframs rule 90 CAR, shown in the next figure, identifies the next state of a FF o/p, Q_t^+ , is gained by XORing the FF o/p's either side i.e. Q_{t-1} and Q_{t+1} .

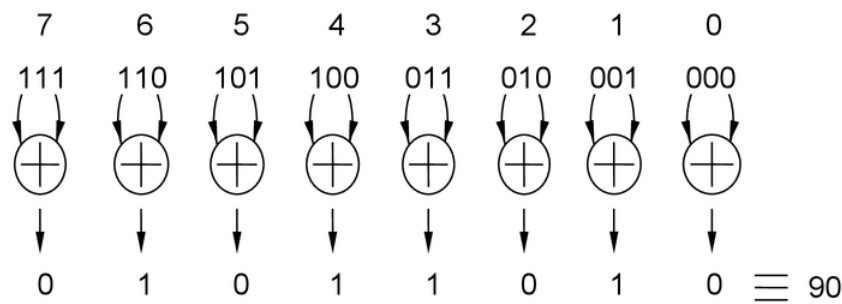


Figure 8: Wolfram rule for CAR 90

Therefore, Wolfram identifies and develops the expressions for rule 90 CAR: $Q_t^+ = Q_{t-1} \oplus Q_{t+1}$ and as show in the following figure, rule 150 CAR: $Q_t^+ = Q_{t-1} \oplus Q_t \oplus Q_{t+1}$.

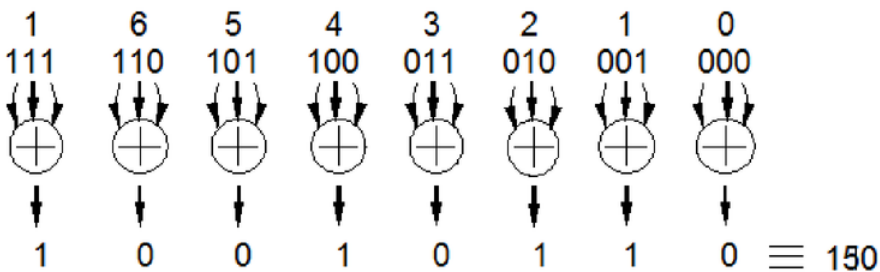


Figure 9: Wolframs rule for CAR 150

It is necessary to combine both CAR 90 and CAR 150 pseudo-random number generators that can then alternate as a hybrid circuit and output a maximum length binary count. The following table

identifies how the hybrid circuit alternates the sequences of both rules according to Wolframs equations to create the maximum length cycle.

Register 1	Register 2	Register 3	Register 4	Register 5	Register 6
90	150	90	150	-	-
90	150	90	150	90	150

Table 4 Shows the alternating sequences for rule 90/150 hybrid cycle.

The following table shows the maximum length output of a 4-bit hybrid CAR 90/150 pseudo-random number generator with a maximum cycle of 1 to 15 repeating back to 1 followed by the hybrid CAR circuit containing 4 - FF and 4 - XOR logic gates.

Decimal Value	Q1 - LSB	Q2	Q3	Q4 - MSB
1	1	0	0	0
3	1	1	0	0
6	0	1	1	0
11	1	1	0	1
13	1	0	1	1
8	0	0	0	1
7	1	1	1	0
10	0	1	0	1
4	0	0	1	0
9	1	0	0	1
14	0	1	1	1
12	0	0	1	1
15	1	1	1	1
2	0	1	0	0
5	1	0	1	0
1	1	0	0	0

Table 5: 4-bit hybrid CAR maximum cycle sequence.

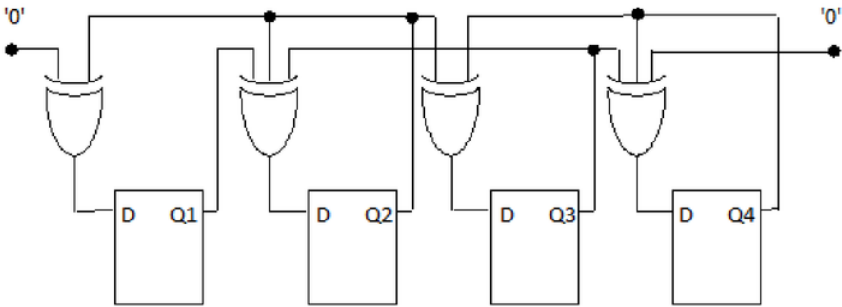


Figure 10: Maximum length 15 hybrid CAR circuit.

Reasonable explanation of the theory behind the

The unpredictability of the CAR is more apparent than with standard LFSR. This is because LFSR purely shift previous input values, but, CAR bit positions are functions of other bit positions therefore making the sequences more random. These CARs are only limited in their output by the gate count and thus are virtually available up to any length maximum cycle.

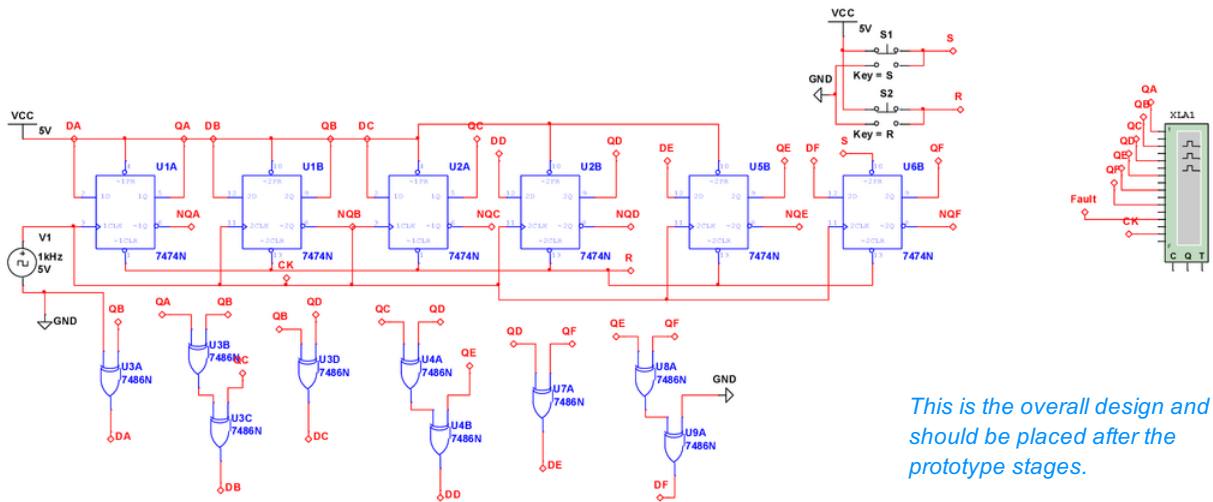


Figure 11: Hybrid 90/150 CAR circuit.

The previous circuit shows a full circuit CAR 90/150 hybrid constructed within Multisim CAD software. The maximum length output table can be seen in the next table. The outputs QA to QF are seen as the outputs of the D-type FFs and these outputs are fed into the XOR logic gates. The XOR logic is then fed back into the FFs as inputs thus creating the CAR 90/150 hybrid circuit.

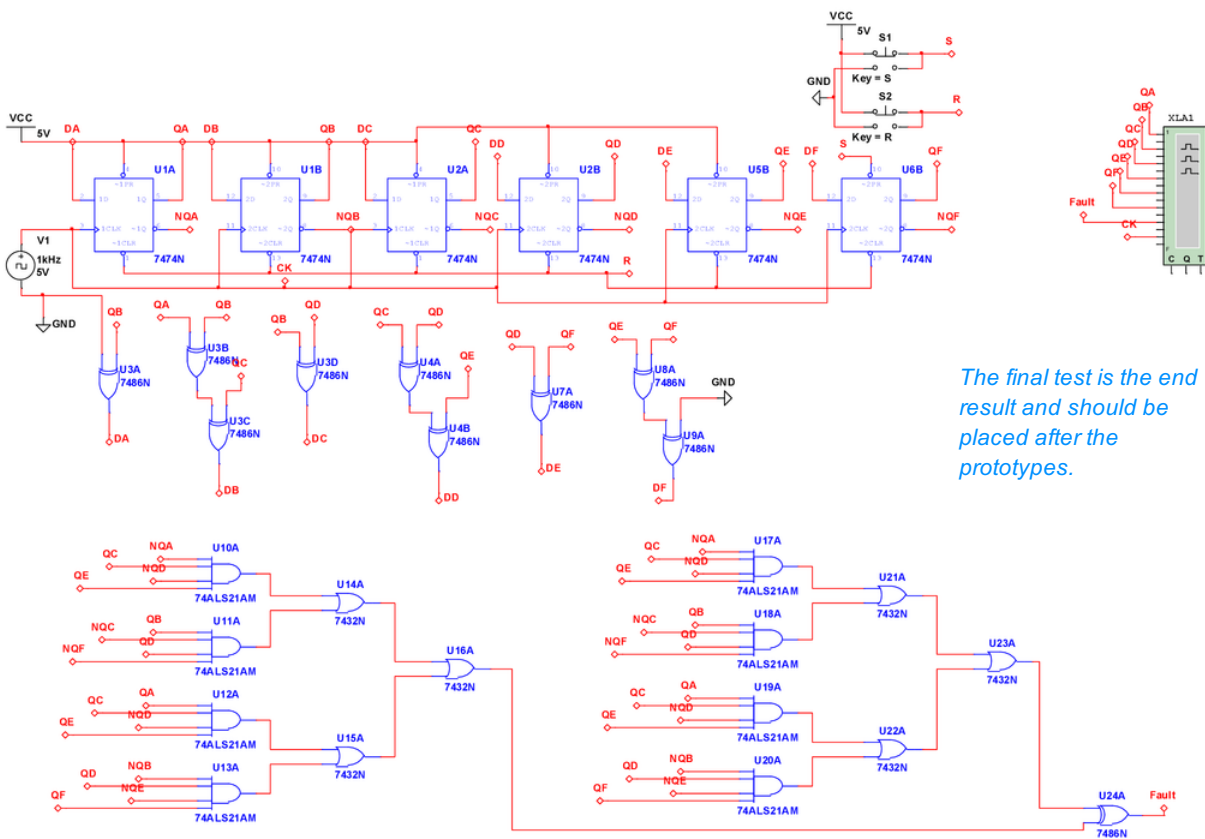
Car 90	Car 150	Car 90	Car 150	Car 90	Car 150	Decimal count	Repeats y/n
0	0	0	0	0	1	1	Y
0	0	0	0	1	1	3	N
0	0	0	1	1	0	6	N
0	0	1	0	1	1	11	N
0	1	0	0	1	0	18	N
1	1	1	1	0	1	61	N
1	1	0	0	0	1	49	N
1	0	1	0	1	1	43	N
0	0	0	0	1	0	2	N
0	0	0	1	0	1	5	N
0	0	1	1	0	1	13	N
0	1	1	0	0	1	25	N
1	0	1	1	1	1	47	N
0	0	1	1	0	0	12	N
0	1	1	0	1	0	26	N
1	0	1	0	0	1	41	N
0	0	0	1	1	1	7	N
0	0	1	0	0	0	8	N
0	1	0	1	0	0	20	N
1	1	1	0	0	0	54	N
1	0	0	0	1	1	35	N
0	1	0	1	1	0	22	N
1	1	0	0	1	1	51	N
1	0	1	1	1	1	45	N
0	0	1	1	1	1	15	N
0	1	1	0	0	0	28	N
1	0	0	0	1	0	34	N
0	1	0	1	0	1	21	N
1	1	0	1	0	1	53	N
1	0	0	1	0	1	37	N
0	1	1	1	0	1	29	N
1	0	0	0	0	1	33	N
0	1	0	0	1	1	19	N
1	1	1	1	1	0	62	N
1	1	0	1	1	1	55	N

1	0	0	0	0	0	32	N
0	1	0	0	0	0	16	N
1	1	1	0	0	0	56	N
1	1	1	1	0	0	60	N
1	1	0	0	1	0	50	N
1	0	1	1	0	1	45	N
0	0	1	0	0	1	9	N
0	1	0	1	1	1	23	N
1	1	0	0	0	0	48	N
1	0	1	0	0	0	40	N
0	0	0	1	0	0	4	N
0	0	1	1	1	0	14	N
0	1	1	1	1	1	31	N
1	0	0	1	0	0	36	N
0	1	1	1	1	0	30	N
1	0	0	1	1	1	39	N
0	1	1	0	0	0	24	N
1	0	1	1	0	0	44	N
0	0	1	0	1	0	10	N
0	1	0	0	0	1	17	N
1	1	1	0	1	1	59	N
1	1	1	0	1	0	58	N
1	1	1	0	0	1	57	N
1	1	1	1	1	1	63	N
1	1	0	1	0	0	52	N
1	0	0	1	1	0	38	N
0	1	1	0	1	1	27	N
1	0	1	0	1	0	42	N
0	0	0	0	0	1	1	Y

Table 6: Shows the maximum length CAR 90/150 hybrid sequence.

The table above shows the maximum length hybrid sequence. This is a 6-bit sequence, 1 to 64 with only the one repeat i.e. starting over. The previous figure, Figure 11, as previously stated is a maximum count CAR 90/150 hybrid. This circuit was then connected to two identical healthy circuits within Multisim CAD environment as shown in the next figure.

Good
Maximum
count
analysis.



The final test is the end result and should be placed after the prototypes.

Table 7:Hybrid 90/150 CAR circuit schematic with two identical circuits connected to it.

The two identical circuits were connected in parallel to an XOR logic gate, thus any one change in a circuit will create a high output from the XOR gate thus denoting a fault in the changed circuit, as;

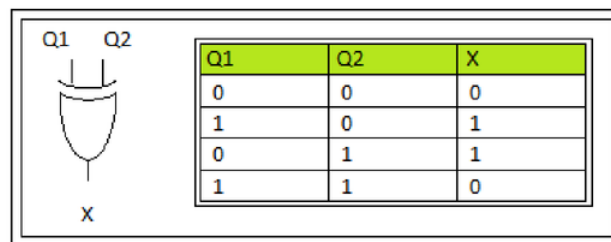


Figure 12: Exclusive OR logic gate and associate truth table.

This method can be used as a testing circuit by providing a healthy circuit with a known output and comparing it to identical circuits. If there are no repeats during a maximum cycle, then the circuit is healthy, if there are repeats within a cycle, then there is a fault in the circuit under test.

The Boolean expression for a health circuits is $NQA \cdot QC \cdot NQD \cdot QE + QB \cdot NQC \cdot QD \cdot NQF + QA \cdot QC \cdot NQC \cdot QE + NQB \cdot QD \cdot NQE \cdot QF$, the health circuit was connected to the logic analyzer and the full 6-bit output, 1 to 63 decimal, can be seen in the following figure.

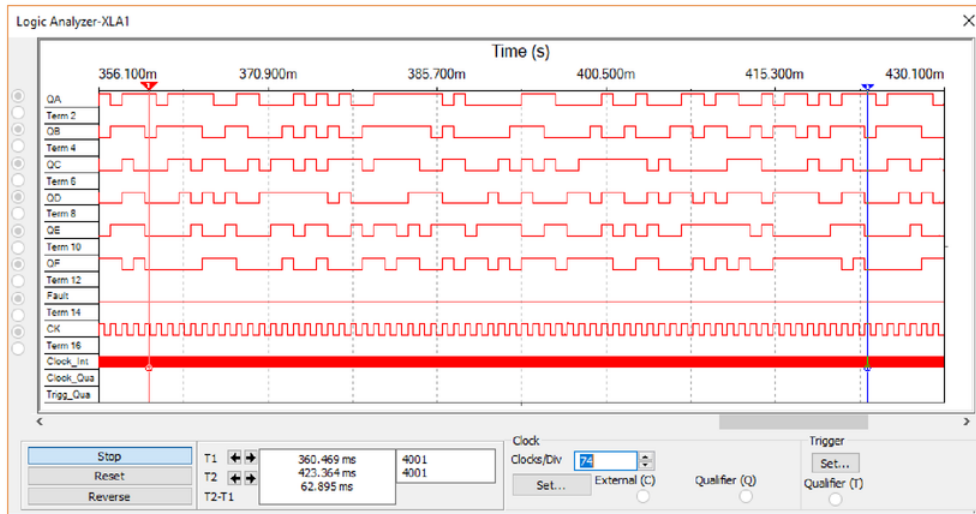


Figure 13: 6-Bit CAR 90/150 hybrid logic analyzer results, no repeats and hence no faults detected.

The following circuit is a CAR 90, 4-bit circuit. This random pattern generator should show a 4-bit count, 1 to 16, but it is limited to a sequence of only 7 random digits as can be seen.

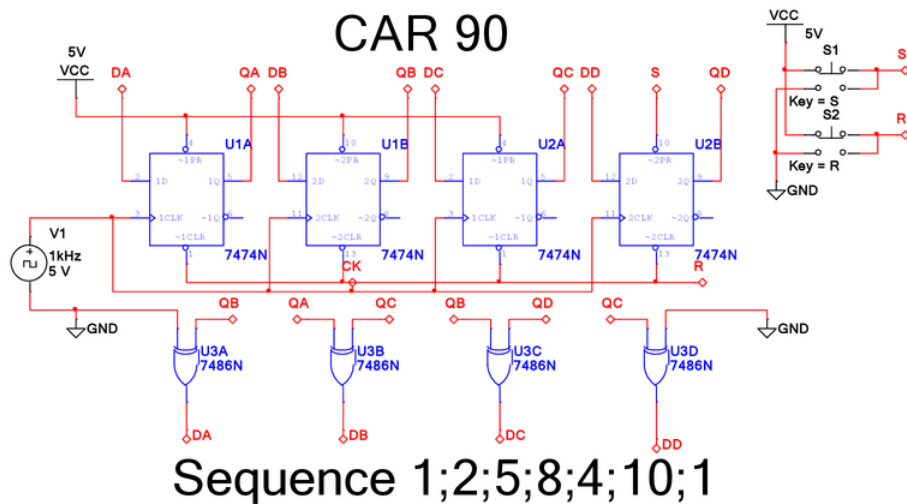


Figure 14: CAR 90 4-bit pseudo random pattern generator schematic.

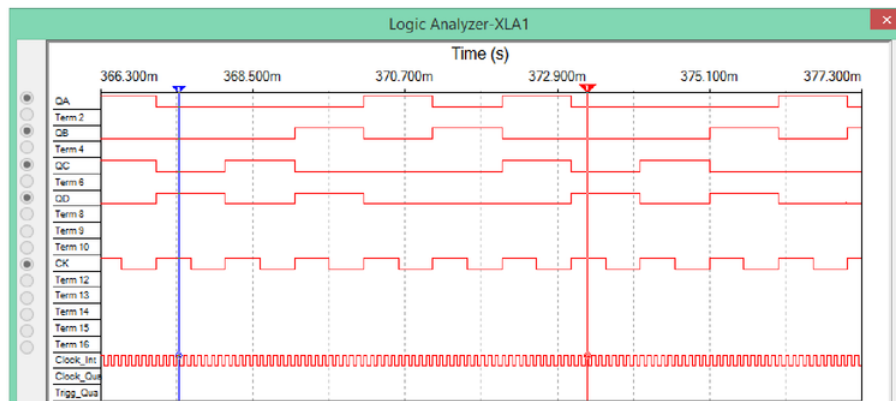
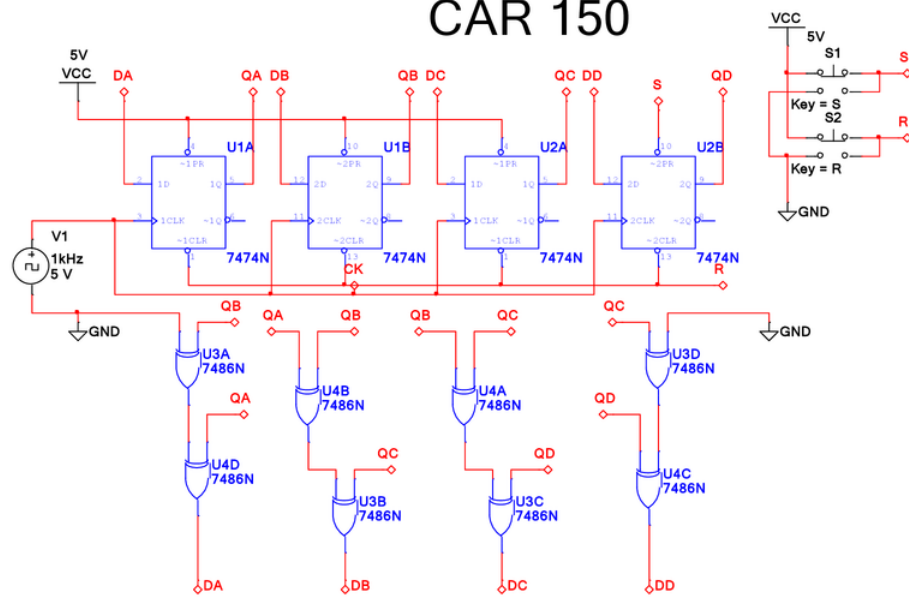


Figure 15: 4 Bit CAR 90 logic analyser results.

The circuit of the 4-bit CAR 90 comprises four flip flops whose next state is determined by the previous values and the values of the next f/f. The outputs, QA, QB, QC & QD, of the f/f are fed through a logic analyzer and the results shown following the circuit. The logic analyzer demonstrates the failure of the CAR 90 as the ideal output would show the complete 4-bit range, 0001 to 1111, i.e. 1 to 15. One complete cycle can be seen as the output of the logic analyzer and the sequence is marked by the blue and red markers giving the output 0001 (1), 0010 (2), 0101 (5), 1000 (8), 0100 (4) & 1010 (10) before starting back at 0001 (1).

As with the 4- bit CAR 90, the following 4-bit CAR 150 will show the output values, 0001 to 1111, i.e. 1 to 15, that are not a maximum length cycle since this is dependent upon the way adjacent cells are connected as suggested in previous sections and continue to be demonstrated in the following information.

CAR 150



Sequence 1;3;4;14;5;13;1

Figure 16: CAR 150 4-bit pseudo random pattern generator schematic.

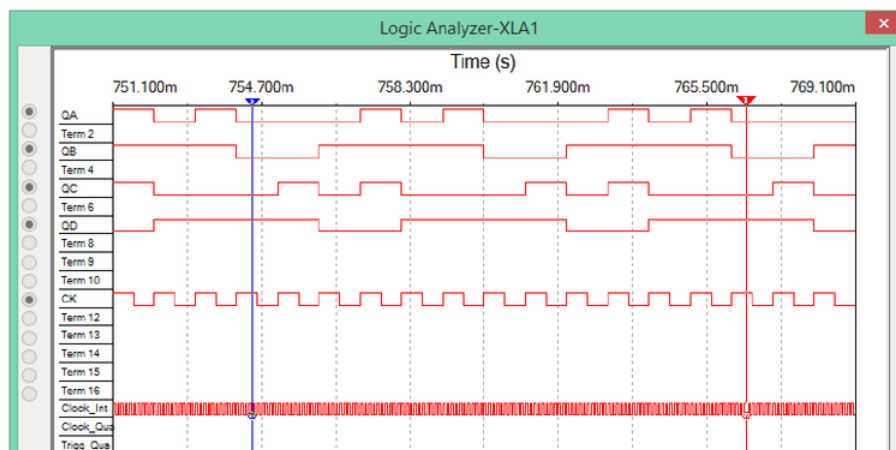
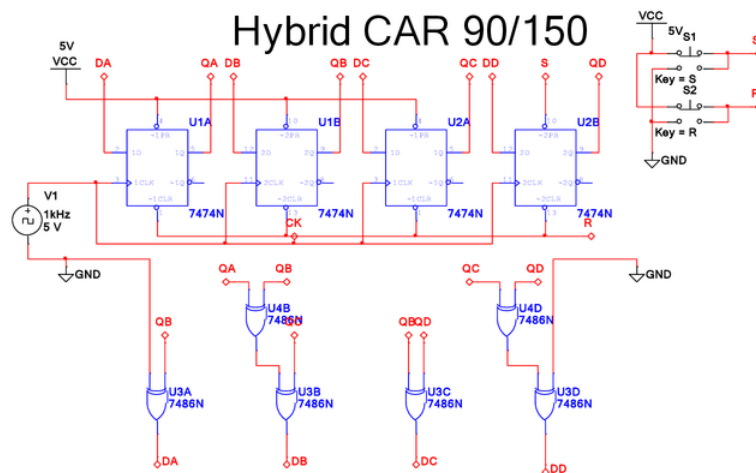


Figure 17: 4 Bit CAR 150 logic analyser results.



Sequence 1;3;6;11;2;5;13;9;7;8;4;14;15;12;10;1

Figure 18: 4 -bit hybrid 90/150 CAR circuit schematic.

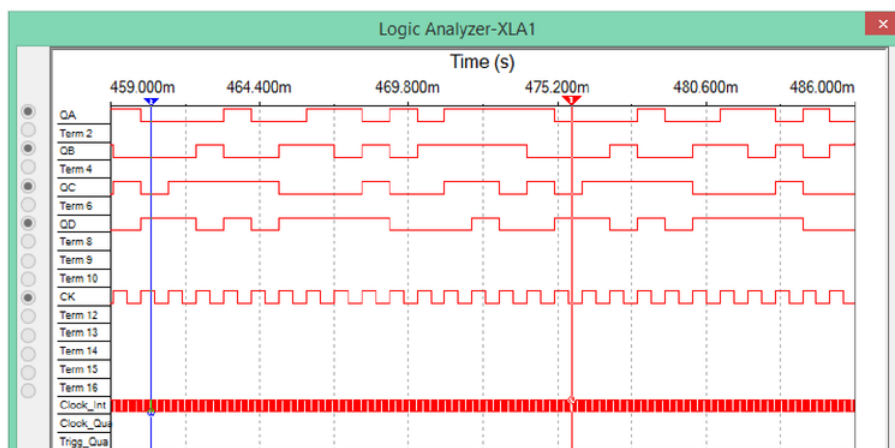


Figure 19: 4-Bit CAR 90/150 hybrid logic analyser results

Now the theory of the healthy circuits has been shown and discussed, the following tests were undertaken to obtain results when deliberate faults were added to one of the circuits. This was undertaken using the full 90/150 CAR circuit and a table of results gathered.

*Proof of
system
performanc
e using
prototypes
should be
before the
final
design.*

Test 1.

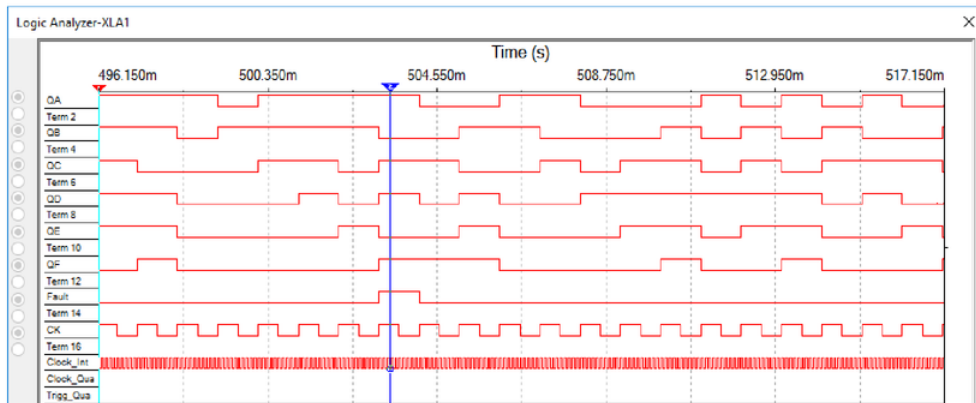


Figure 20: Logic analyser results with fault 1 added to CAR 90/150 hybrid circuit.

Test results taken at fault QF grounded: QA, NQB, QC, QD, NQE, QF = 101101

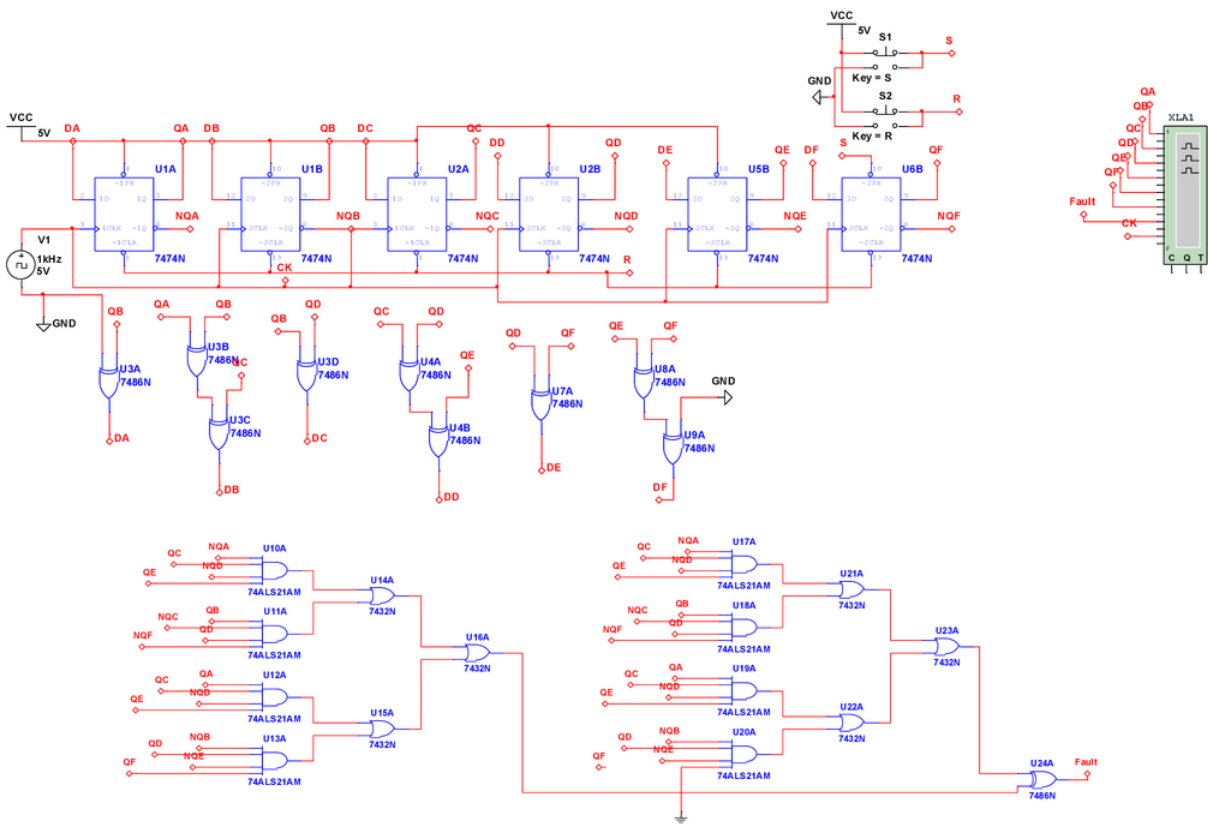


Figure 21: CAR 90/150 hybrid schematic with one circuit logic input grounded, QF.

Test 2.

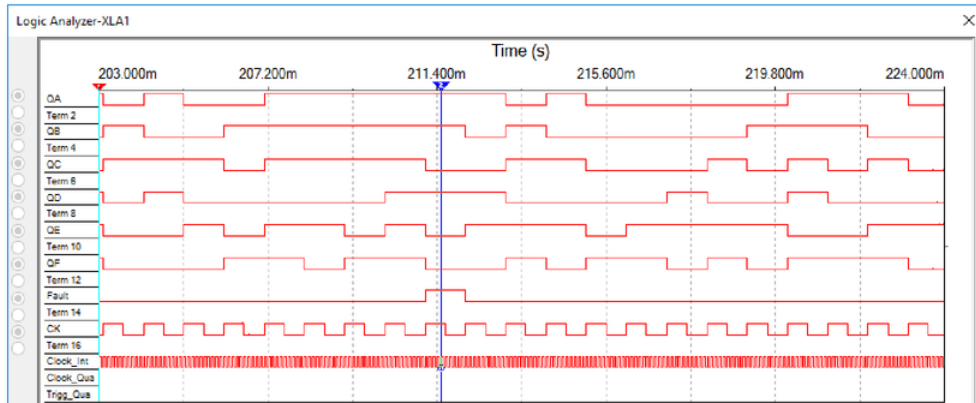


Figure 22: Logic analyser results with fault 2 added to CAR 90/150 hybrid circuit.

Test results taken at fault NQF grounded: QA, QB, NQC, QD, NQE, NQF = 110100

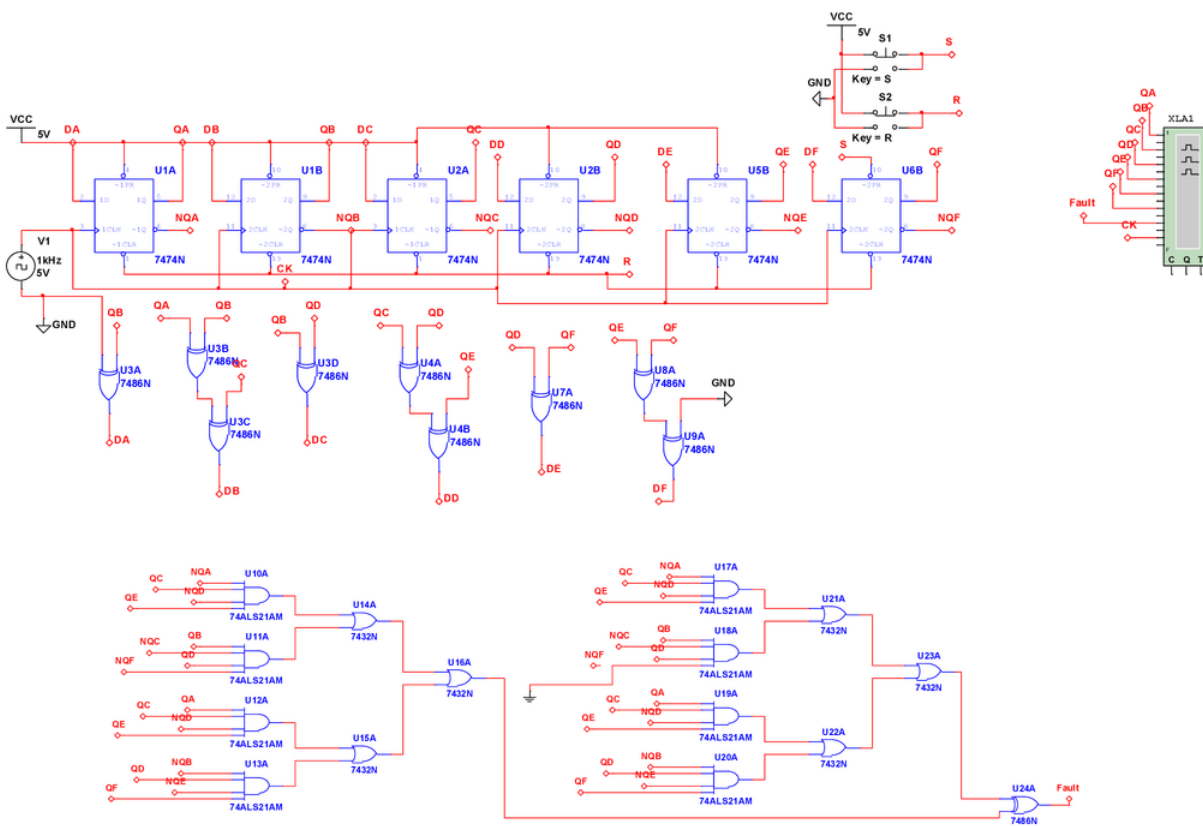


Figure 23: CAR 90/150 hybrid schematic with one circuit logic input grounded, NQF.

Test 3 with fault, fault E tied to ground.

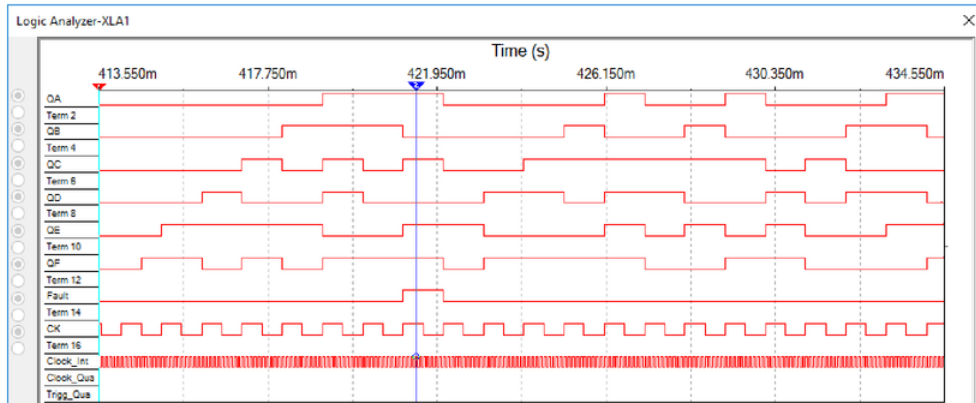


Figure 24: Logic analyser results with fault 3 added to CAR 90/150 hybrid circuit.

Test results taken at fault QE grounded: QA, NQB, QC, NQD, QE, QF = 101011

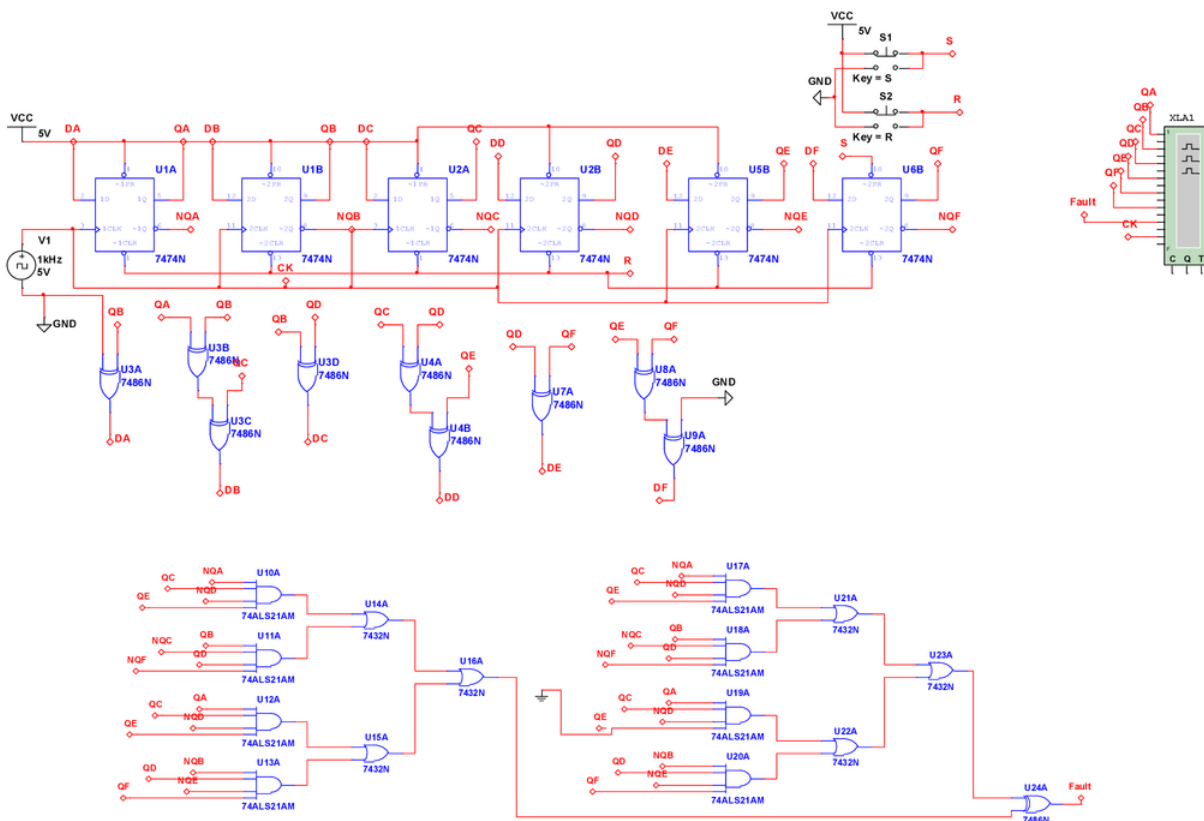


Figure 25: CAR 90/150 hybrid schematic with one circuit logic input grounded, QE.

Final CAD
design and
test looks
correct.

Boolean o/p from 6 bit CAR	Boolean required from good cct	Sim fault result from test cct	Fault detected y/n
A NB C D NE F	$NQA.QC.NQD.QE + QB.NQC.QD.NQF + QA.QC.NQD.QE + NQB.QD.NQE.QF$	$NQA.QC.NQD.QE + QB.NQC.QD.NQF + QA.QC.NQD.QE + NQB.QD.NQE.'0'$	Y
A B NC D NE NF	$NQA.QC.NQD.QE + QB.NQC.QD.NQF + QA.QC.NQD.QE + NQB.QD.NQE.QF$	$NQA.QC.NQD.QE + QB.NQC.QD.'0' + QA.QC.NQD.QE + NQB.QD.NQE.QF$	Y
A NB C ND E F	$NQA.QC.NQD.QE + QB.NQC.QD.NQF + QA.QC.NQD.QE + NQB.QD.NQE.QF$	$NQA.QC.NQD.QE + QB.NQC.QD.NQF + QA.QC.NQD.'0' + NQB.QD.NQE.QF$	Y

Table 8: Results when various faults were added to one of the healthy circuits.

4. Vivado – FPGA, HDL design, test & analysis

Following the design, test and analysis of the cellular automata register using CAD software Multisim, the procedures were repeated using another CAD software, Xilinx Vivado. Design with Multisim included selecting FFs and logic gates to build the various CAR circuits. Vivado is different in that the register and logic gates are created using hardware descriptive language within function block known as IPs which are loaded into an FPGA. The following results were obtained using the hardware language, creating a test bench and running to provide the timing diagrams relate to the 4-bit CAR 90 and 150 rules.



Figure 26: 4-Bit CAR 90 rule timing diagram.

It can be seen in Figure 26 that, as with the Multisim examples 4-bit CAR 90 rule, a maximum sequence has not been achieved. The blue marker shows the start of the cycle with the yellow marker ending it. The Boolean output at the blue marker is Q0, NQ1, NQ2, NQ3 = 1000 binary = 8 decimals. The uncompleted full 4-bit sequence is shown in the following table.

Boolean expression	Binary sequence	Decimal value
Q0, NQ1, NQ2, NQ3	1000	8
NQ0, Q1, NQ2, NQ3	0100	4
Q0, NQ1, Q2, NQ3	1010	10
NQ0, NQ1, NQ2, Q3	0001	1
NQ0, NQ1, Q2, NQ3	0010	2
NQ0, Q1, NQ2, Q3	0101	5
Q0, NQ1, NQ2, NQ3	1000	8

Table 9: Uncomplete 4-bit CAR 90 cycle.

This table clearly shows that the CAR 90 cycle has not been completed. The following figure and table will go on to show, as expected, that the 4-bit individual CAR 90 and CAR 150 rules will not generate a maximum sequence cycle. Not shown, but already proven, the same is true with the individual 6-bit CAR 90 and CAR 150 circuits.

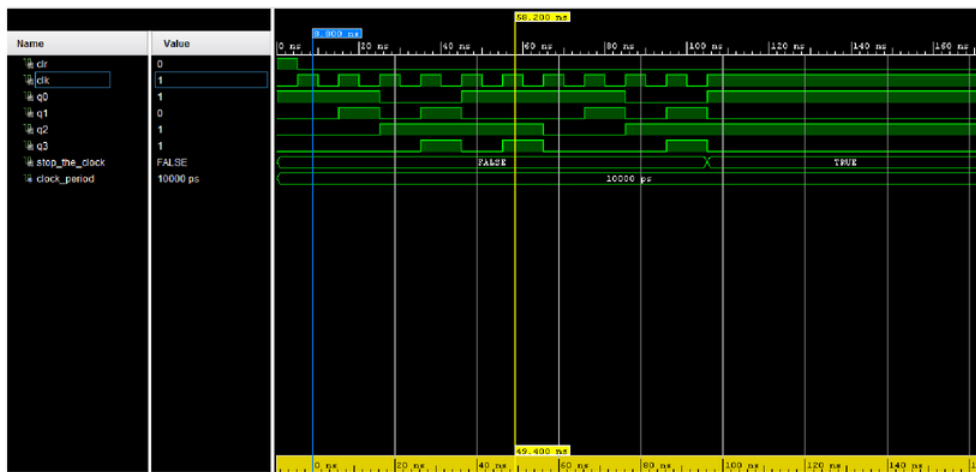


Figure 27: 4-Bit CAR 150 rule timing diagram.

Boolean expression	Binary sequence	Decimal value
Q0, NQ1, NQ2, NQ3	1000	8
Q0, Q1, NQ2, NQ3	1100	12
NQ0, NQ1, Q2, NQ3	0010	2
NQ0, Q1, Q2, Q3	0111	7
Q0, NQ1, Q2, NQ3	1010	10
Q0, NQ1, Q2, Q3	1011	11
Q0, NQ1, NQ2, NQ3	1000	8

Table 10: Uncomplete 4-bit CAR 150 cycle.

*Good proof
testing of the
individual
CAR svstems.*

A 4 – bit 90/150 hybrid register IP was created as can be seen in the following figure. As with the previous examples a CAR 90/150 hybrid and timing diagrams obtained. A table was completed with the obtained results.

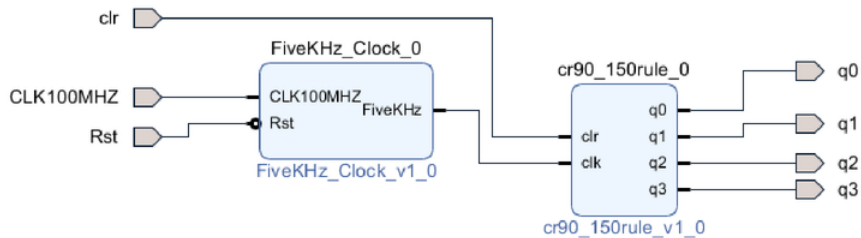


Figure 28: 4 - Bit CAR 90/150 hybrid IP created in Vivado.



Figure 29: 4-Bit CAR 90/150 hybrid timing diagram.

Boolean expression	Binary sequence	Decimal value
Q0, NQ1, NQ2, NQ3	1000	8
Q0, Q1, NQ2, NQ3	1100	12
NQ0, Q1, Q2, NQ3	0110	6
Q0, Q1, NQ2, Q3	1101	13
NQ0, Q1, NQ2, NQ3	0100	4
Q0, NQ1, Q2, NQ3	1010	10
Q0, NQ1, Q2, Q3	1011	11
Q0, NQ1, NQ2, Q3	1001	9
Q0, Q1, Q2, NQ3	1110	14
NQ0, NQ1, NQ2, Q3	0001	1
NQ0, NQ1, Q2, NQ3	0010	2

Tests show clearly that the hybrid does work and has maximum count capability before repeat. This shows the prototyped 4 bit version.

NQ0, Q1, Q2, Q3	0111	7
Q0, Q1, Q2, Q3	1111	15
NQ0, NQ1, Q2, Q3	0011	3
NQ0, Q1, NQ2, Q3	0101	5
Q0, NQ1, NQ2, NQ3	1000	8

Table 11: 4 – Bit maximum sequence CAR 90/150 hybrid count.

It can be seen from the timing diagram and table above that the CAR 90/150 hybrid circuit has achieved a maximum 4 – bit sequence, 1 to 15 with the only repeat being the start again in the random sequence. This shows a healthy output from the register. The following test was undertaken on the 6 – bit version of the hybrid circuit and a timing diagram obtained. The results show a maximum cycle 1 to 63, zero is not loaded as at zero the initial loaded seed value is also zero.

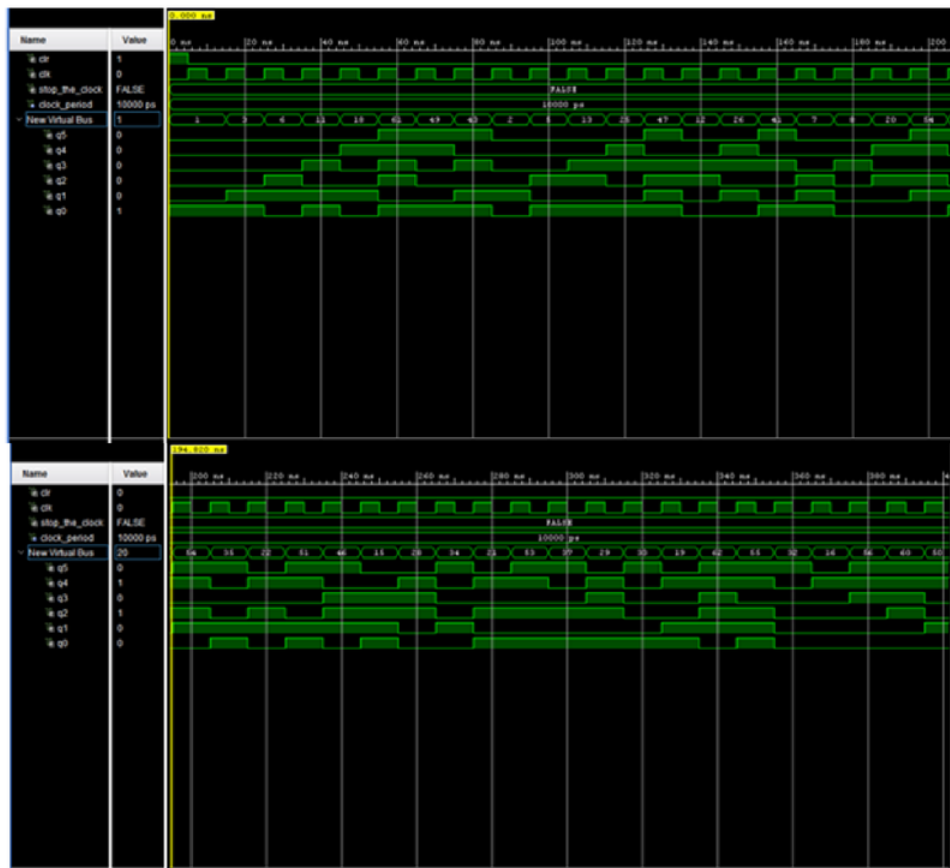


Figure 30: Maximum sequence 6 - bit CAR 90/150 hybrid part 1.

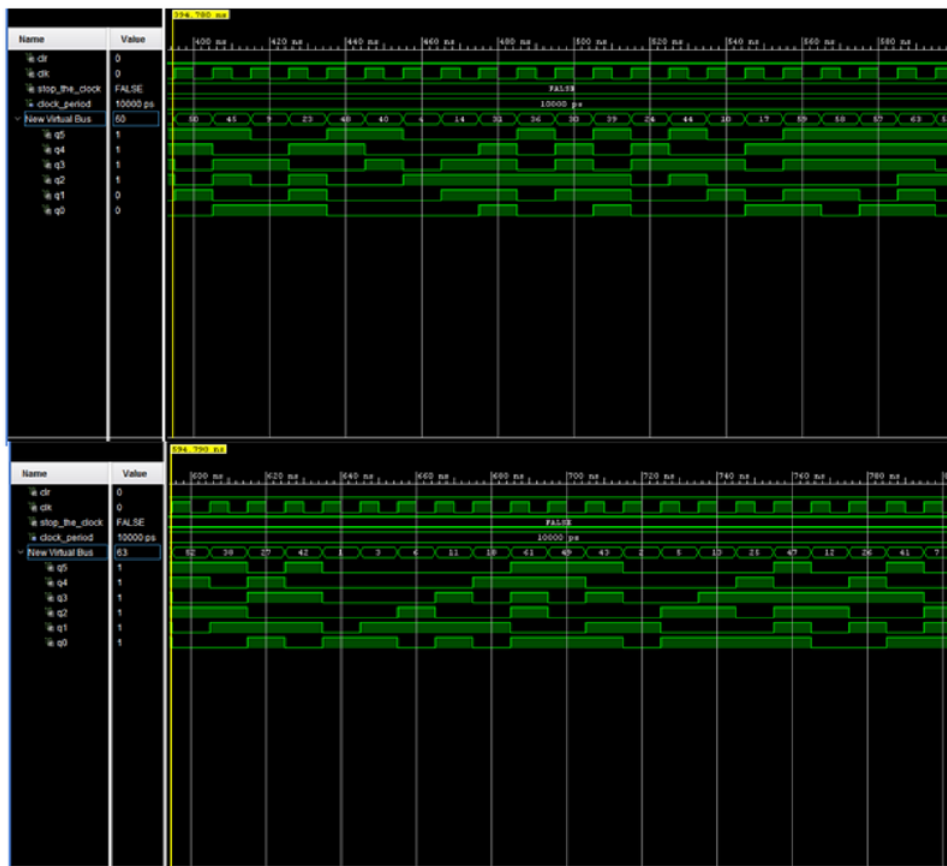


Figure 31: Maximum sequence 6 - bit CAR 90/150 hybrid part 2.

6 bit hybrid CAR max count analysis shows correct results.

With the created VHDL programs and simulation files, a Vivado project was created and source files added to obtain the complete 6 – bit register 90/150 hybrid and clock IPs as shown in the following figure. Each component, the register and clock, act as function blocks that when create, are exported through the software and used at leisure by the creator when required. All the various components and logic are created in the same way and then the complete circuit was built for downloading to the FPGA located on the Nexus 4DDR development board.

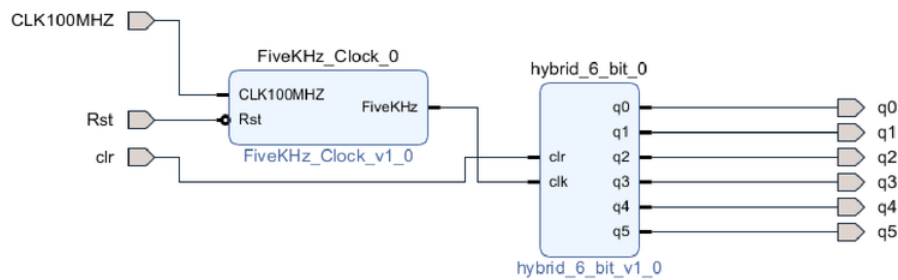


Figure 32: The clock and CAR 90/150, 6 - bit register created in Vivado as IPs.

Now that a register has been completed that replaces the FFs in the Multisim simulations, the logic IPs can be created in the same way and added to the register circuit.

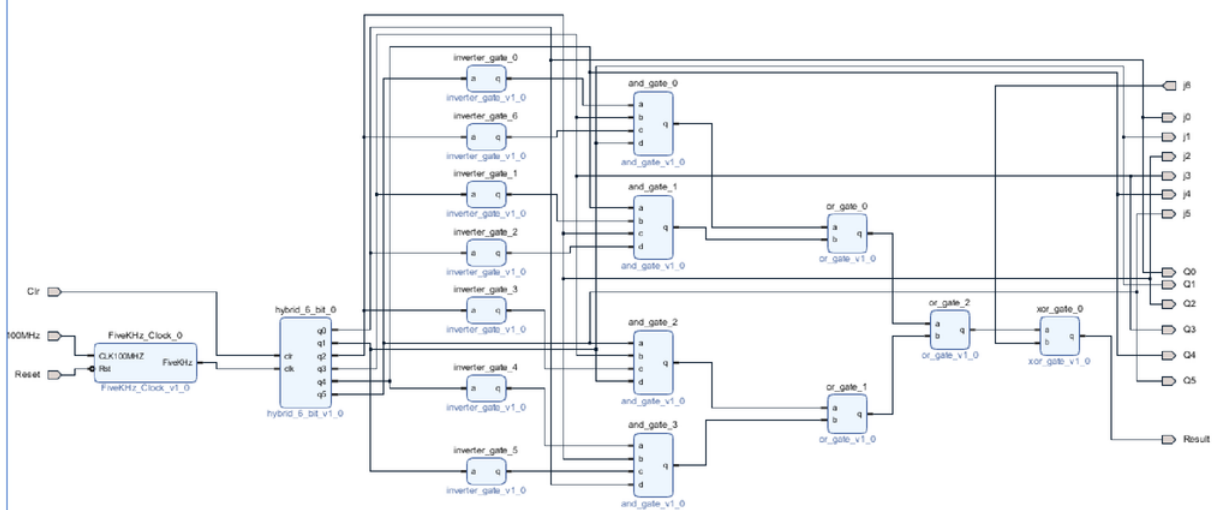


Figure 33: The complete healthy 6-bit CAR 90/150 circuit.

Design looks good and includes the output from x-or gate.

The completed circuit is connected as one of the inputs into an IP XOR logic gate. The other input of the XOR gate is available for the connection of a test circuit and will be utilised in the practical task. All code for the various IPs, including the registers and all associated logic is available to view in the appendix section of this report.

The completed IP circuit, following running through the synthesis tool and proving okay, can now be downloaded to the FPGA on the Nexus development board. This can then be compared with an exact physical circuit created on breadboard. The breadboard circuit can then be adjusted to create faults thereby using the FPGA as a test circuit. The following images show the Nexus 4DDR development board and the breadboard circuit.

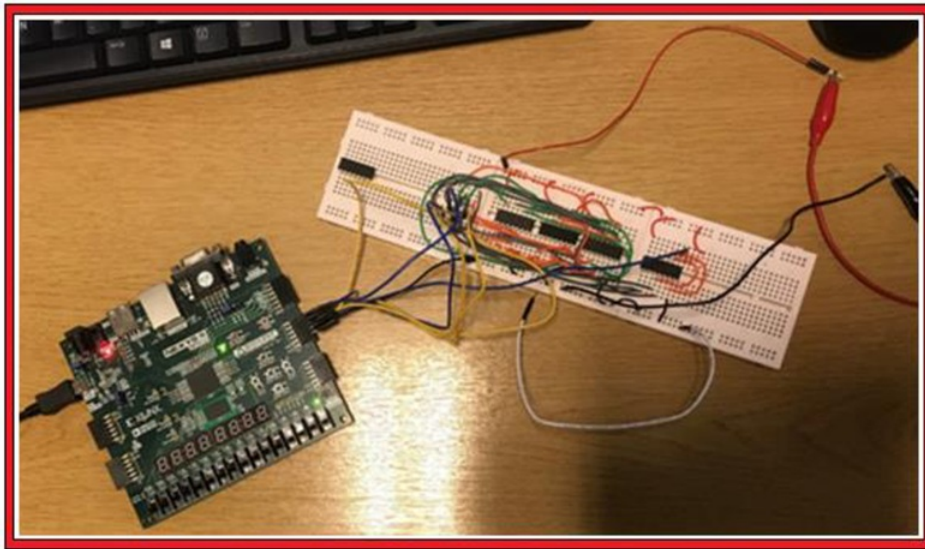


Figure 34: The development board connected to the PC and the breadboard circuit.

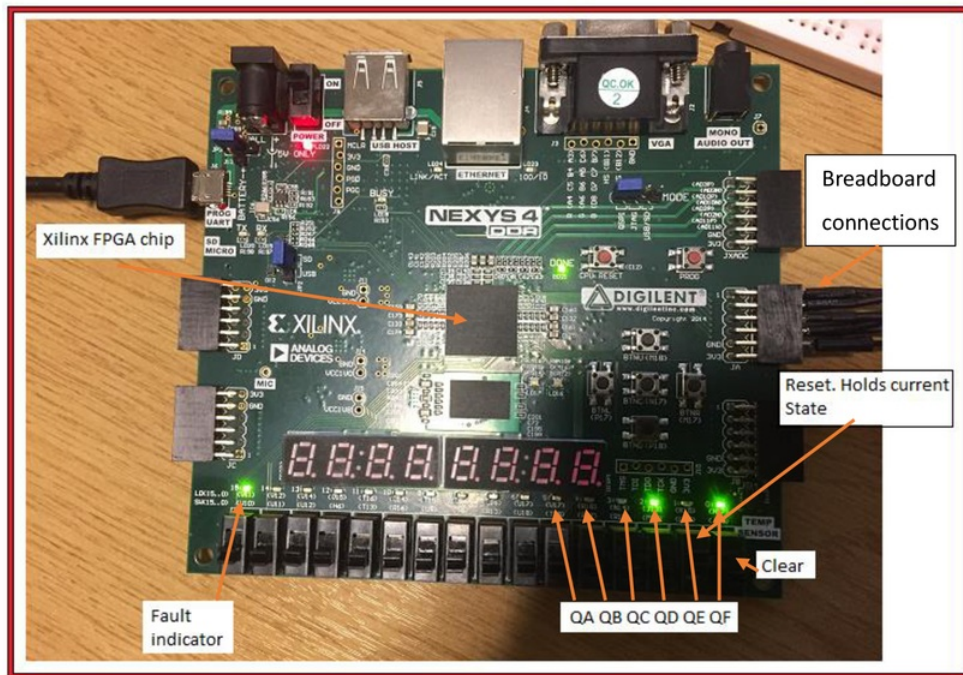


Figure 35: Nexys 4DDR development board with Xilinx FPGA.

The above figure shows the development board that houses the FPGA which now has the Vivado program contained within it. The 6 – bit LEDs are labelled with QA the least significant bit going through to QF the most significant bit, but, as the LEDs are inverted, a lit LED indicates a low (0), therefore the binary o/p shown in the figure is 111010 LSB. The fault indicator is labelled as well as

the actual FPGA, reset switch, clear switch and the connections to the breadboard. The next figure shows the physical circuit built on the breadboard. Various faults were created on the breadboard circuit and results obtained.

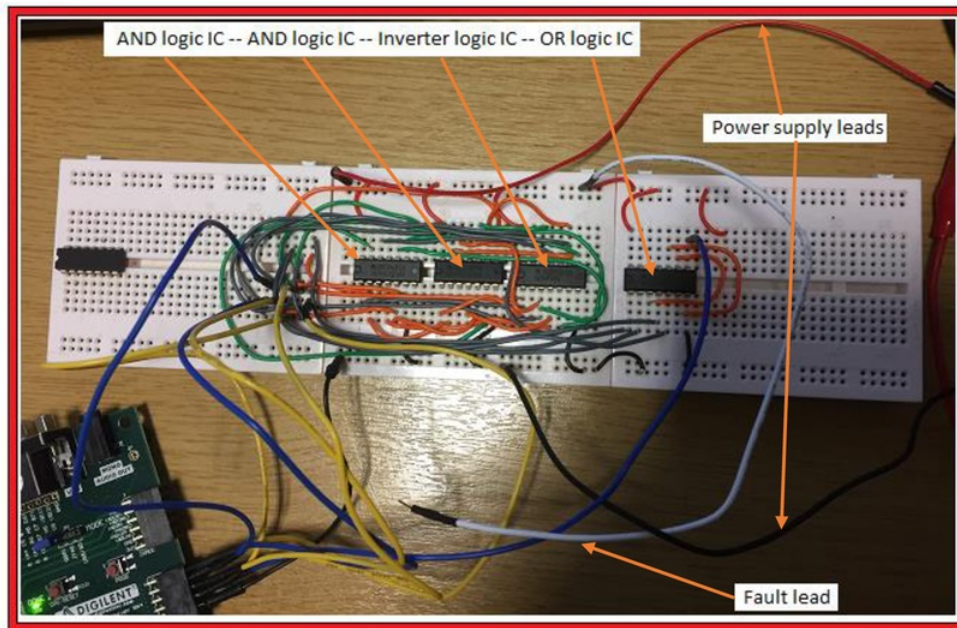


Figure 36: The breadboard physical circuit 6 - bit CAR 90/150 hybrid designed using logic ICs.

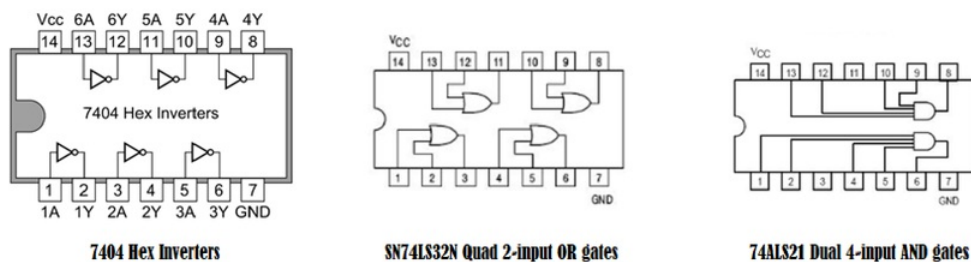


Figure 37: Integrated Circuits used to provide the logic for the breadboard circuit.

The following images were the results of the practical testing of the pattern generator used to test the prototype design. The faults produced on the breadboard are a repeat of the Multisim test and therefore a table for comparison will be produce following the images of the practical test results. A direct comparison will not be possible as the sequences will identify the fault in different locations as these are random.

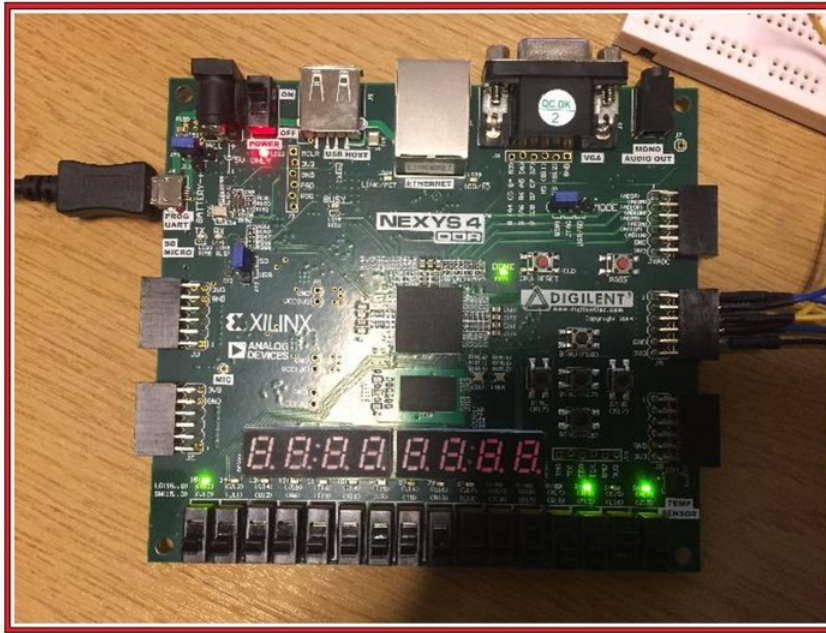


Figure 38: Image of the first practical test using the Nexys 4DDR development board.

Test results taken at fault QF grounded: QA, QB, QC, NQD, QE, NQF = $111010_B = 106_D$

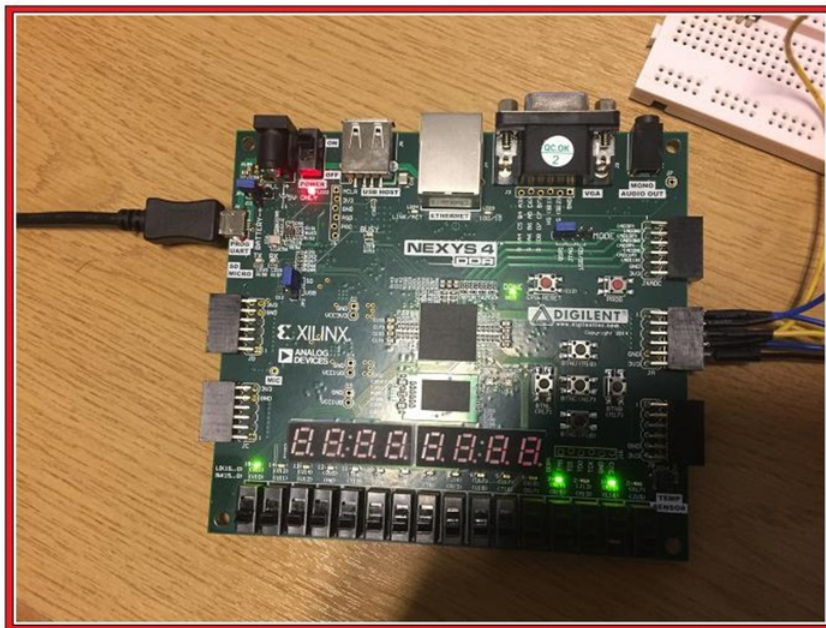


Figure 39: Image of the second practical test using the Nexys 4DDR development board.

Test results taken at fault NQF grounded: QA, QB, NQC, QD, NQE, QF = $110101_B = 101_D$

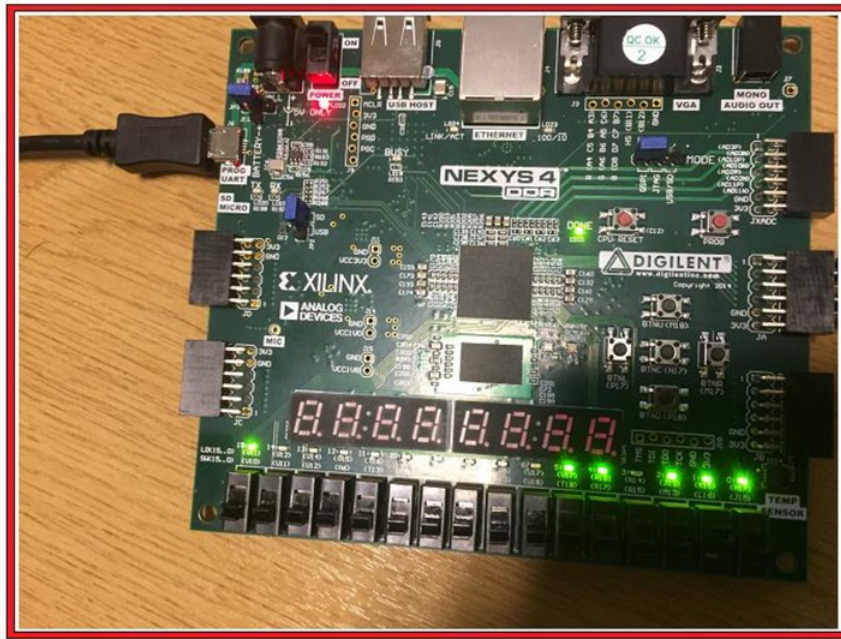


Figure 40: Image of the second practical test using the Nexus 4DDR development board.

Test results taken at fault QE grounded: NQA, NQB, QC, NQD, NQE, NQF = 001000_B = 12_D

Boolean expression	Binary sequence	Decimal value	Fault detected Y/N	Test number
QA, QB, QC, NQD, QE, NQF	111010	106	Y	1
QA, QB, NQC, QD, NQE, QF	110101	101	Y	2
NQA, NQB, QC, NQD, NQE, NQF	001000	12	Y	3

Table 12: Showing the results of the practical testing of the breadboard circuit.

The practical breadboard circuit, connected in parallel with the FPGA healthy circuit through the XOR IP within the program of the FPGA, has been tested and has shown the correct operation of the generator prototype. It was then necessary to design and build the physical circuit using design and build PCB methods. The results will follow in the next section.

5. Practical PCB build & testing of prototype on prototyping board

This task involved designing the physical test prototype circuit onto a printed circuit board (PCB). The design suite software, Eagle, was used to undertake this task and the results follow. The first step is to create the circuit schematic containing the design components, the following figure shows the results.

Practical testing with CUT is illustrated and explained well. Good table of results.

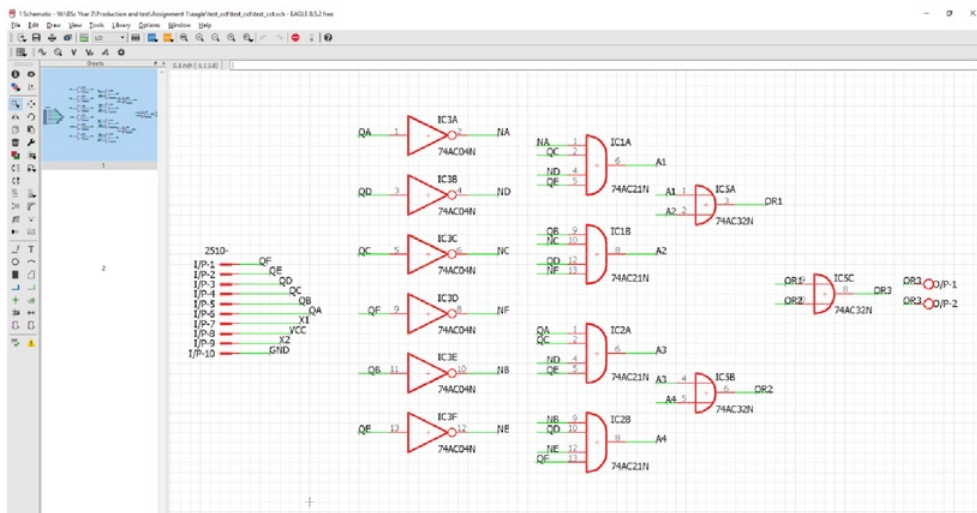


Figure 41: The schematic design showing the chosen components relative information.

The PCB schematic design identifies the inputs along with the chosen components and their relative identifications which will ultimately identify the trace circuit positions. The schematic shows the 6 inverter, 4 AND gate, 3 OR gate and the output positions. The PCB schematic design is not sent to manufacturer, the following built up layered designs, developed with software provided by Gerber – Viewer is sent to manufacturer.

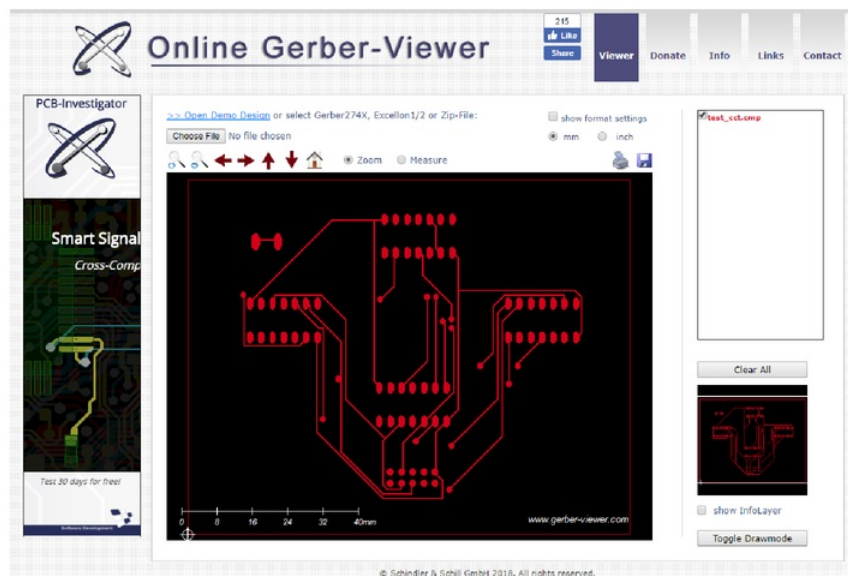


Figure 42: First layer of PCB being the copper, component side, CMP file.

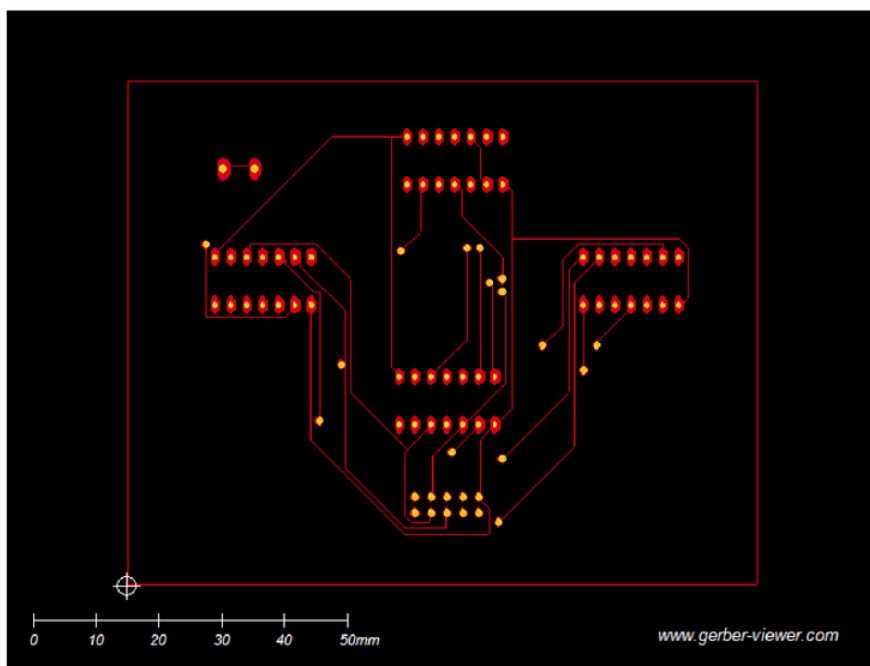


Figure 43: PCB second layer being the drill file, DRD.

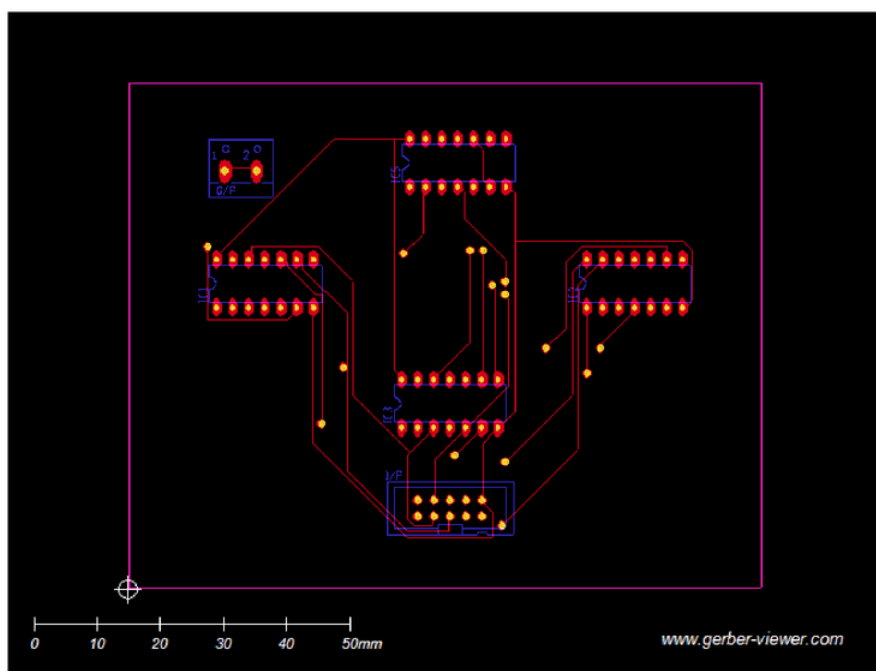


Figure 44: PCB third layer being the silk screen, component side, PLC file.

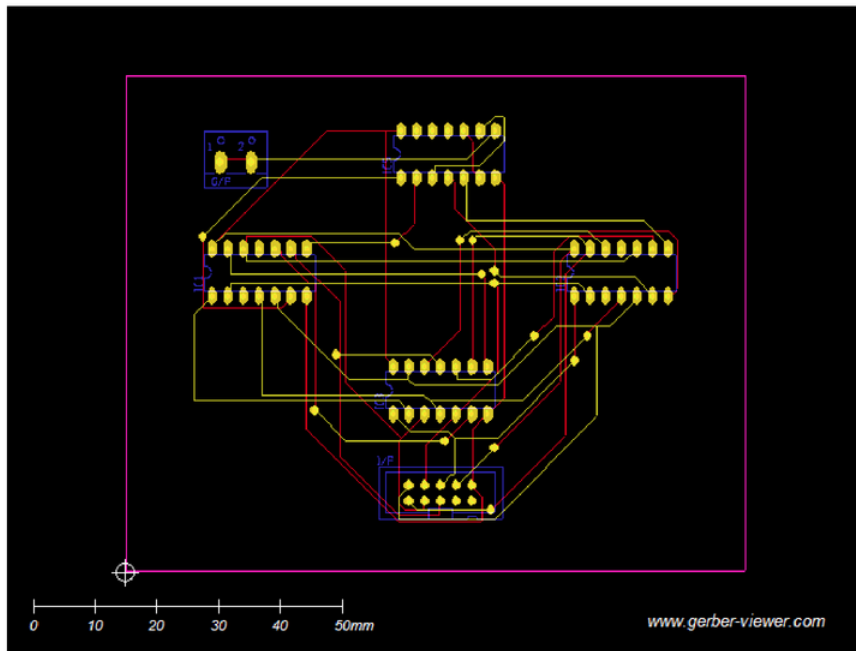


Figure 45: PCB fourth layer being the copper, solder side, SOL file.

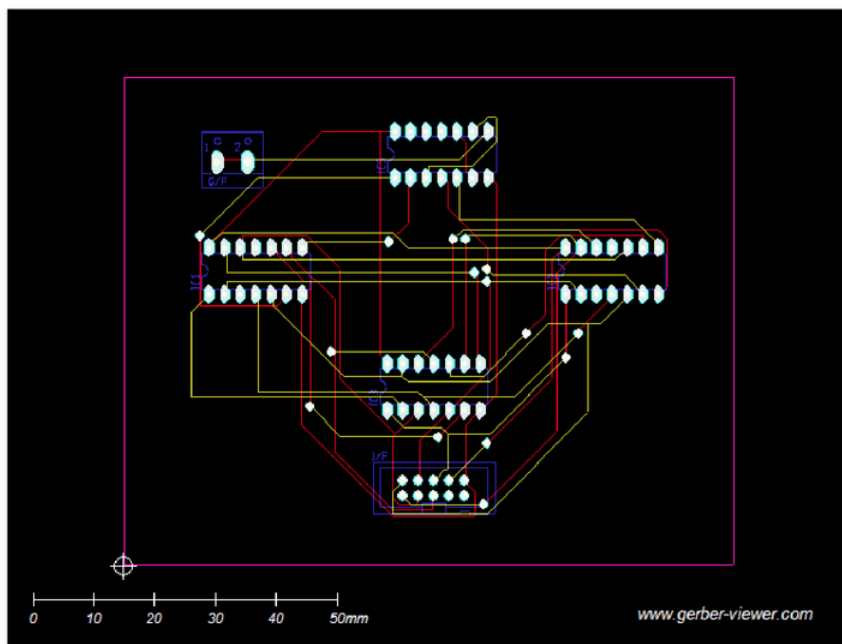


Figure 46: PCB fifth layer being the solder stop mask, component side, STC file.

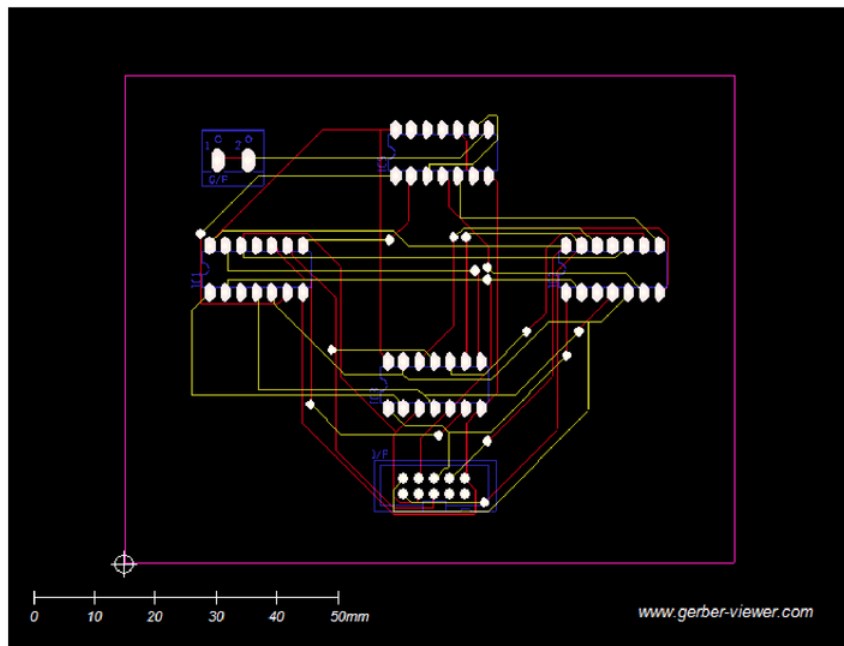


Figure 47: PCB sixth layer being the solder stop mask, solder side, STS file.

This design is sent to manufacturer to develop and produce the PCB. This is PTH, with holes drilled and all layers made up to produce conductors. The components are soldered to this design. The on board chips are solder and include all logic, but, the XOR gate is not on this board as it is on the Nexus 4DDR circuit board and therefore this PCB is connected to the Nexus XOR gate.

The different layers are all generated independently within the Eagle software and are identified with the following description.

- .CMP File (Copper, component side)
- .DRD File (Drill)
- .DRI File (Drill station info file) not usually required
- .GPI file (Photoplotter info file) not usually required
- .PLC File (Silk screen, component side)
- .PLS File (Silk screen, solder side)
- .SOL File (Copper, solder side)
- .STC File (Solder stop mask, component side)
- .STS File (Solder stop mask, solder side)

The completed layers files are sent off to a manufacturer for the PCB to be fabricated. The following images show the PCB before and after the component ICs are solder using the holes provided during the manufacturing process.

Explanation of process is clear and includes the file types needed for production.

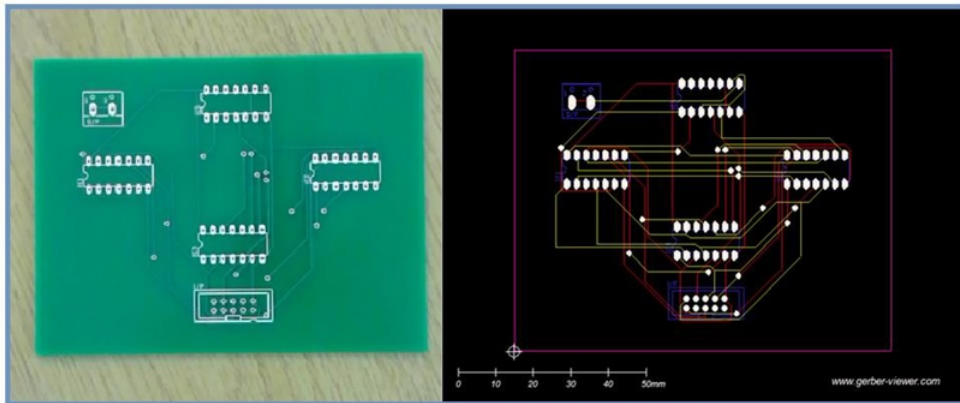


Figure 48: Showing the manufactured PCB from the Eagle design files.

Following the development of the PCB circuit layout, the selected IC components were soldered to the PCB and then the PCB was connected to the Nexus 4DDR development board and a healthy test was completed as well as a circuit with a fault added. The following images show the obtained results.

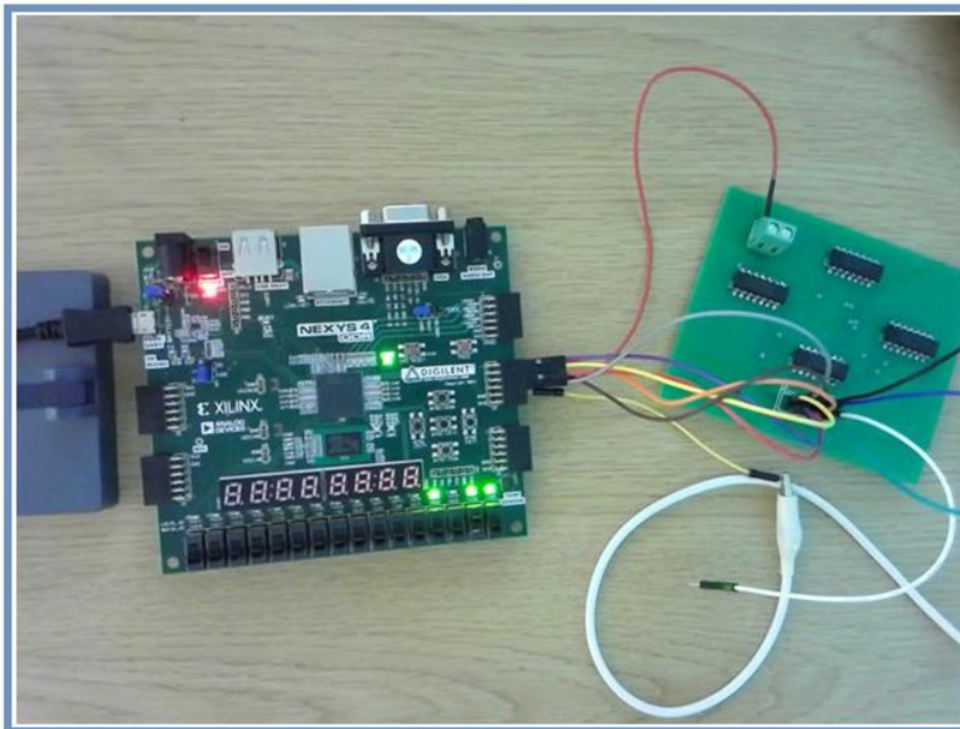


Figure 49: The completed PCB was connected in parallel, as a healthy circuit, with the FPGA HDL circuit.

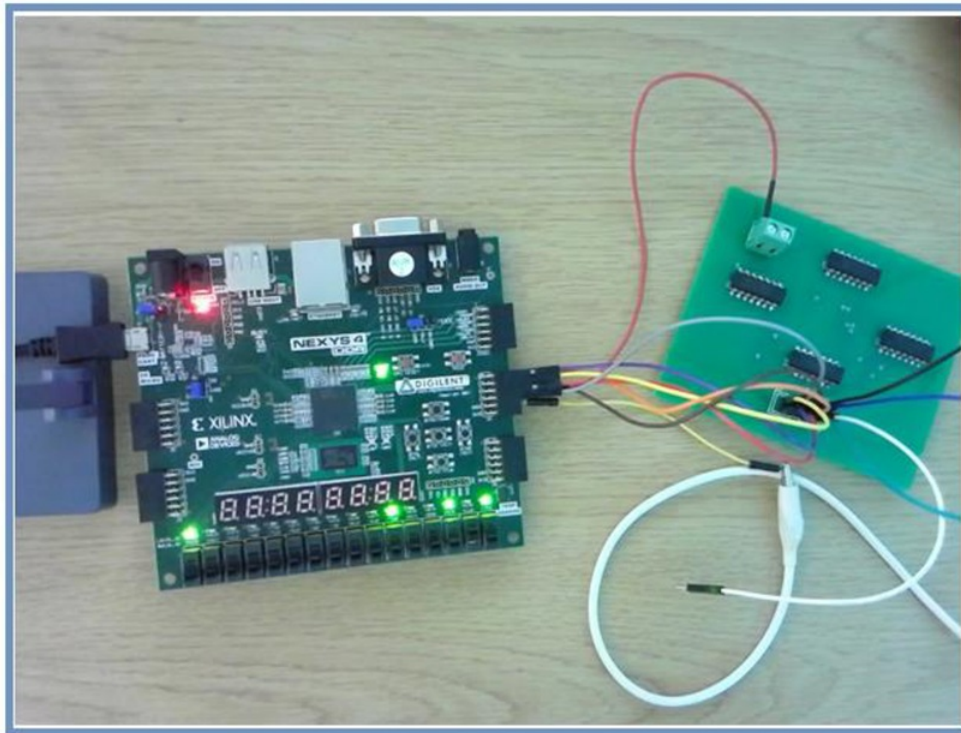


Figure 50: The completed PCB was connected in parallel, as an unhealthy circuit, with the FPGA HDL circuit.

6. Conclusions

The aims and objectives were to research the soldering techniques and design methods of a basic 2-layer printed circuit board. This was achieved by referencing several reputable sources. The different methods of attaching components to the PCB by either plated through hole or surface mount techniques and combinations of both were discussed in great depth. The difference in the types of components when adopting either PTH or SMT was researched and discussed. The history and economics of PCB manufacturing was deliberated over and the trends toward mass production through the automatic assembly of SMT including the benefits and quality assessments. Investigations through research was undertaken into the use of automatic testing of PCBs and the quality of soldering, conductive traces and component selection and placement qualities by both optical inspections and X-ray inspections.

A systematic approach was adopted during the design and testing of a prototype product. The investigations into pattern generators was undertaken and an effort to obtain best practices when meeting customer requirements. Through a combination of computer aided design software

National Instruments, Multisim and hardware development tools using HDL on a FPGA, computer aided manufacturing design and testing techniques were used to create a hybrid pattern generator. The techniques were used to produce material for analysis of a maximum cycle pattern generator, running and alternating two pseudo-random shift registers according to rules identified by Wolfram, CAR rule 90 and CAR rule 150 as a hybrid, produced the desired results of a 6-bit maximum count output. The results of these tasks are clearly shown within this report and the progression to a physical prototype identified.

The developed 6-bit pseudo-random pattern shift register success was measured by performing analysis and testing the design to perform several maximum sequence outputs. This has been identified and shown to be successful by the results produced within this report. The successfulness was then amplified by downloading the HDL program to the Nexus 4DDR development board to compare the hardware with an identical circuit built on a breadboard. The circuits were connected in parallel and faults created within the breadboard circuit. A successful result would be measured by whether the faults, identified by repeats during a 6-bit sequence, were indicated on the Nexus 4DDR board. This was the case and the results obtained were used to produce a table of results.

Using CAD software, Eagle, the random 6-bit pattern generator was, after first testing the circuit on breadboard, designed to be developed as a PCB. IC logic components were chosen to perform the logic tasks. The circuit layers were identified and built up using CAM processes and sent off to be produced. The completion of the PCBs was undertaken back in the lab, by mounting the components onto the board and soldering in place. Tests and inspections were performed to confirm traces and the quality of the solder joints and then the PCB was connected in parallel with the FPGA circuit and tested in the same way the breadboard was tested. The results and images are contained within this report.

*Good points made
here.*

7. References

- Abadir, M., 1994. *Economics of Electronic Design, Manufacture and Test*. Second ed. Dordrecht: Kluwer Academic.
- Electronic Notes, 2013. *Surface Mount Technology & SMT Devices*. [Online]
Available at: www.electronics-notes.com
[Accessed Wednesday January 2018].
- Landers, T. L., 1994. *Electronics Manufacturing Processes*. Second ed. New Jersey: Prentice - Hall.
- Poole, I., 2016. *Electronics notes*. [Online]
Available at: <https://www.electronics-notes.com>
[Accessed Monday Feb 2018].
- Wakerly, J. F., 2013. *Digital Design Principles & Practices*. fourth ed. Bangladesh: Pearson.
- Williams, T., 2005. *The Circuit Designers Companion*. Second ed. Oxford: Elvsevier.

8. Bibliography

- Abadir, M., 1994. *Economics of Electronic Design, Manufacture and Test*. Second ed. Dordrecht: Kluwer Academic.
- Electronic Notes, 2013. *Surface Mount Technology & SMT Devices*. [Online]
Available at: www.electronics-notes.com
[Accessed Wednesday January 2018].
- Landers, T. L., 1994. *Electronics Manufacturing Processes*. Second ed. New Jersey: Prentice - Hall.
- Poole, I., 2016. *Electronics notes*. [Online]
Available at: <https://www.electronics-notes.com>
[Accessed Monday Feb 2018].
- Wakerly, J. F., 2013. *Digital Design Principles & Practices*. fourth ed. Bangladesh: Pearson.
- Williams, T., 2005. *The Circuit Designers Companion*. Second ed. Oxford: Elvsevier.

*Good number of
sources used.*

9. Appendix

9.1 Vivado program codes and IP circuits

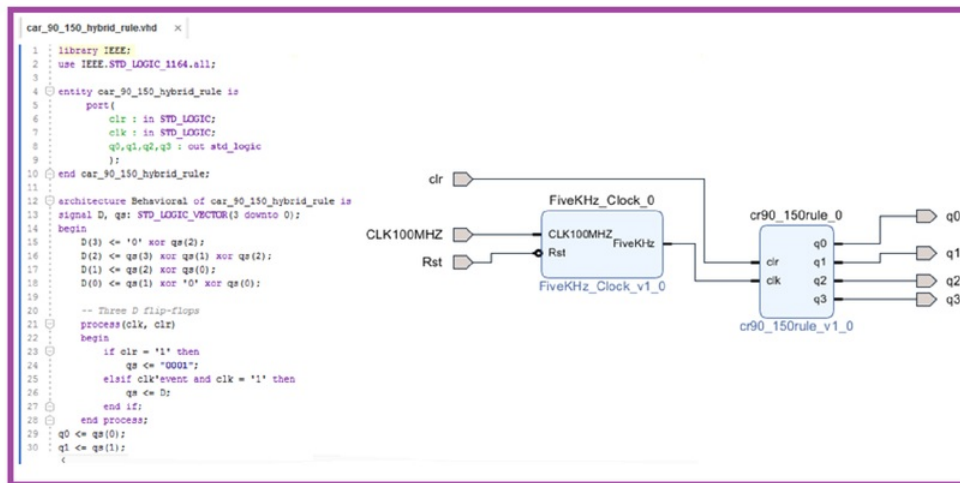


Figure 51: 4-Bit CAR 90/150 hybrid program and IP circuit.

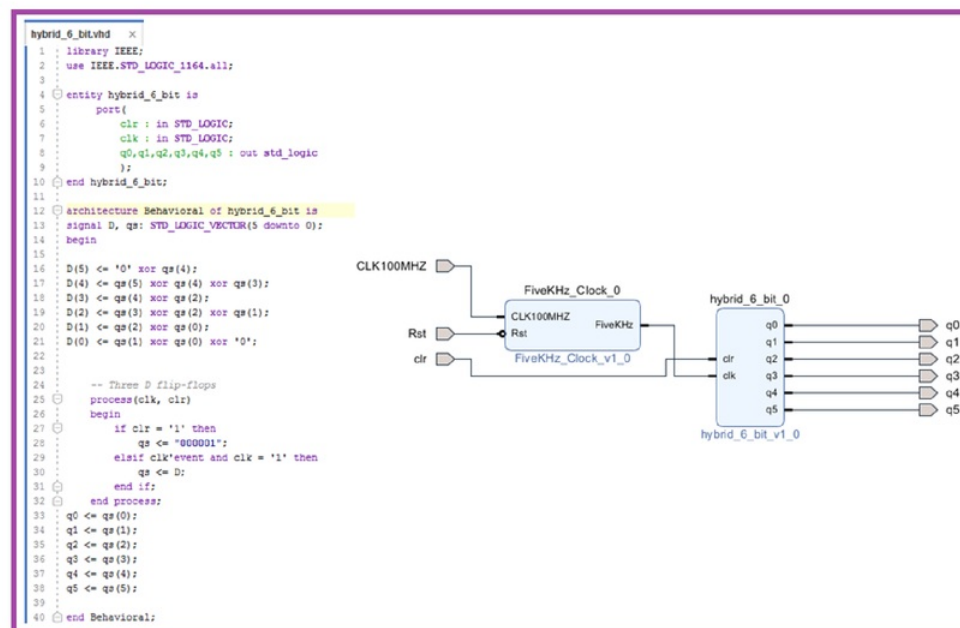


Figure 52: 6-Bit CAR 90/150 hybrid program and IP circuit.

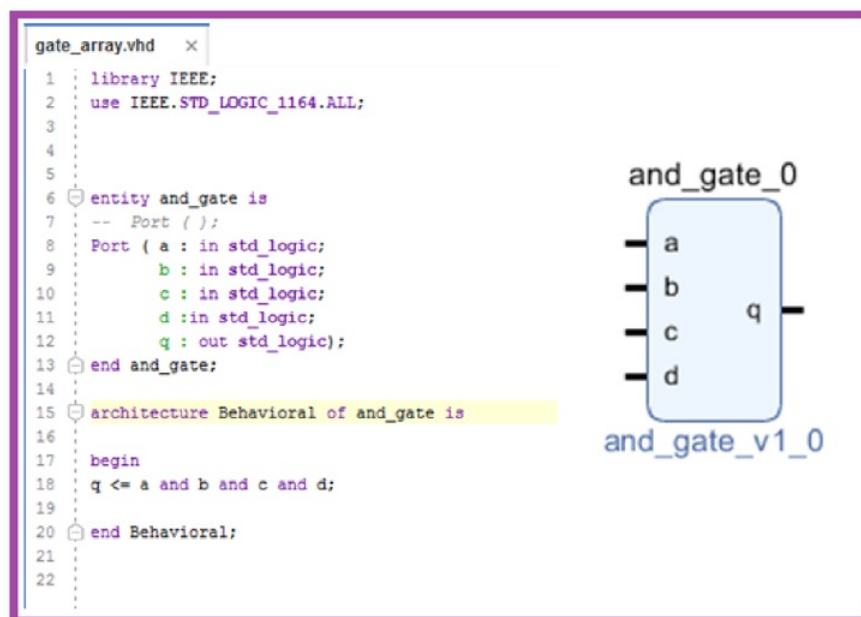


Figure 53: AND logic gate program and IP circuit.

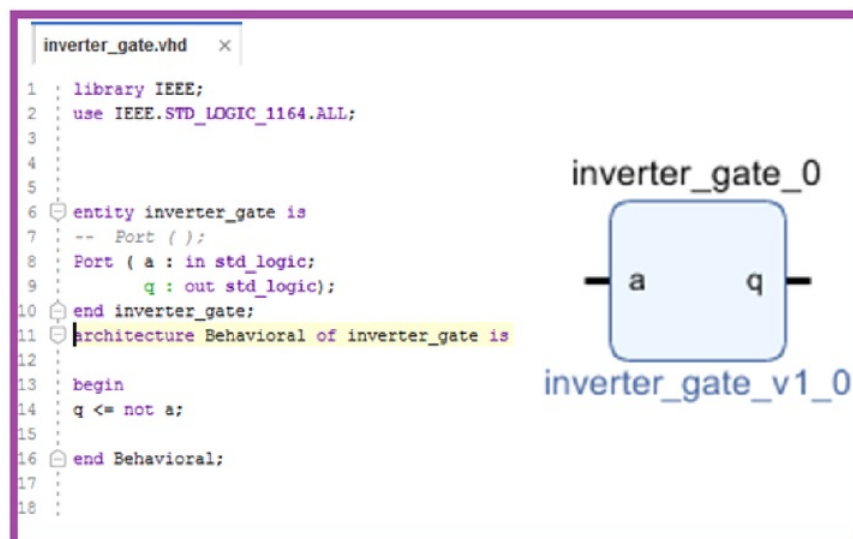


Figure 54: Inverter logic gate program and IP circuit.

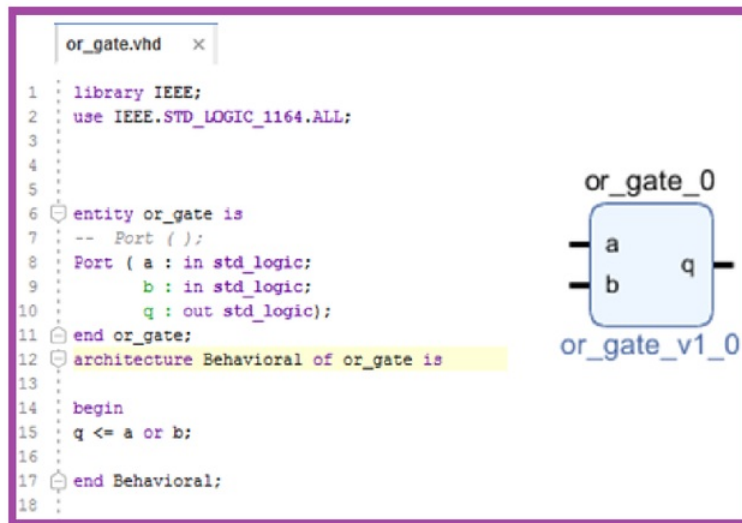


Figure 55: OR logic gate program and IP circuit.

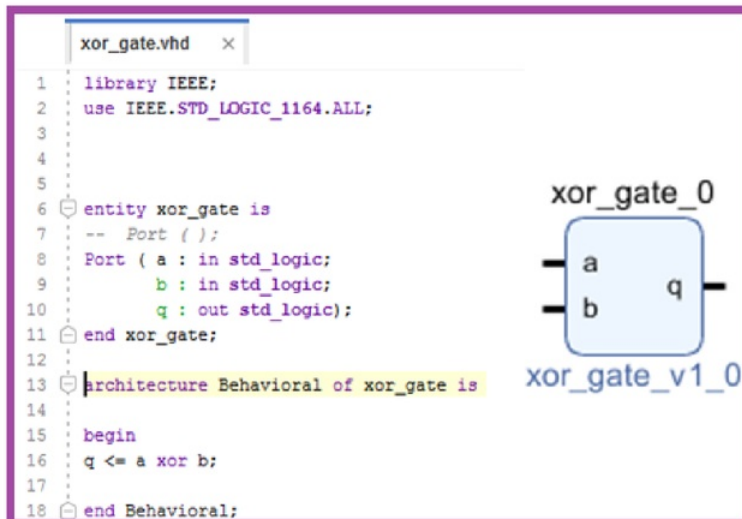


Figure 56: XOR logic gate program and IP circuit.

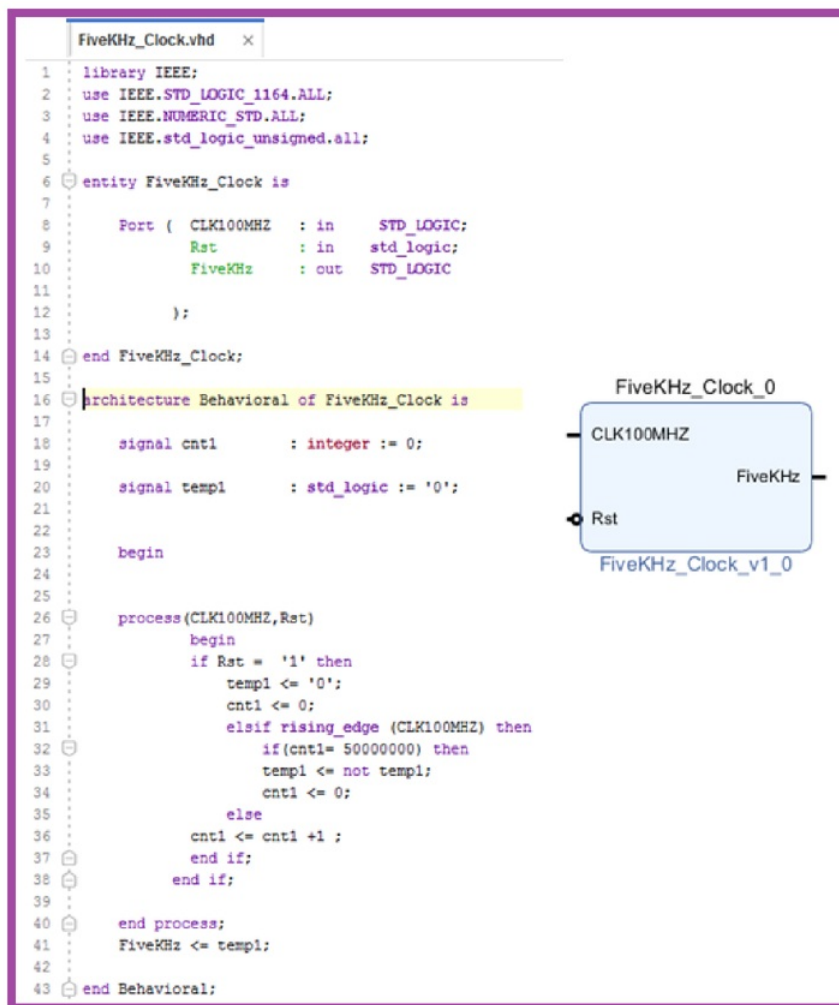


Figure 57: The clock program and IP circuit.

Appendix of the prototypes is good. Would have been good to make references to this appendix from the main report.

Assignment 1

GRADEMARK REPORT

FINAL GRADE

GENERAL COMMENTS

Instructor

68/100

PAGE 1

PAGE 2

PAGE 3

PAGE 4

PAGE 5

PAGE 6

PAGE 7

PAGE 8

Text Comment. Research in this area is detailed.

PAGE 9

PAGE 10

PAGE 11

Text Comment. Good explanation of heat profiles for solder process.

PAGE 12

PAGE 13

PAGE 14

Text Comment. A variety of ATE for production industry is included and explained. Good effort.

PAGE 15

PAGE 16

Text Comment. Reasonable explanation of the theory behind the CAR rules. There many rules which could have been mentioned.

PAGE 17

Text Comment. This is the overall design and should be placed after the prototype stages.

PAGE 18

PAGE 19

Text Comment. Good Maximum count analysis.

PAGE 20

Text Comment. The final test is the end result and should be placed after the prototypes.

PAGE 21

PAGE 22

PAGE 23

PAGE 24

Text Comment. Proof of system performance using prototypes should be before the final design. This part proves the hybrid and disproves the individual rule applications.

PAGE 25

PAGE 26

PAGE 27

Text Comment. Final CAD design and test looks correct.

PAGE 28

PAGE 29

Text Comment. Good proof testing of the individual CAR systems.

PAGE 30

PAGE 31

Text Comment. Tests show clearly that the hybrid does work and has maximum count capability before repeat. This shows the prototyped 4 bit version.

Text Comment. 6 bit hybrid CAR max count analysis shows correct results.

Text Comment. Design looks good and includes the output from x-or gate.

Text Comment. Practical testing with CUT is illustrated and explained well. Good table of results.

Text Comment. Explanation of process is clear and includes the file types needed for production.

Text Comment. Good points made here.

Text Comment. Good number of sources used.

Text Comment. Appendix of the prototypes is good. Would have ben good to make

GRADING FORM: CSG-RUBIC

BRIAN JONES

0

RESEARCH-INFORMED LITERATURE



SMT research into the technology is good and has relevant diagrams for support. Solder process for this is included with heat profiles explanations. 3.5/5 SMT and PTH technology is discussed with an evaluation. 3/5 ATE for modern production industry includes a good variety and are explained clearly. 7.5/10 Good intro. Could have pointed out the virtual ATE theme with this assignment.

14/20

KNOWLEDGE AND UNDERSTANDING



Design of 6 bit CAR is good and all the prototypes are there and have been explained. They are however in the wrong order. 4.5/7 PCB design process is logical and several design scenarios were created and tested for the best selected design. 5.5/7 Design of FPGA 6 bit CAR is good with all stages included. the appendix does include all the VHDL prototype components necessary for the final system. 4/6

14/20

ANALYSIS

Test results for the hybrid CAR with comparison to



theory is achieved but the order of the content makes this difficult to piece together. 6/10 FPGA and PCB analysis is good. All the prototypes are included in the appendix. It would be beneficial to reference the appendix from within the main report. 7/10 A little disorganised in parts

13/20

PRACTICAL APPLICATION AND DEP.



PCB manufacture procedure is clearly explained. All the files needed for manufacture process are explained for each layer. 11/15 FPGA testing proved the prototype stages were not capable of maximum count and further design stages proved the hybrid. This is explained well but the sequence in the report could be better. 6/10 Good despite being a little disorganised.

17/25

SKILLS FOR PROFESSIONAL PRAC.



Use of appropriate software was professional and some good research is shown with external software. 3.5/5 Report is good but layout / order could be better. Some parts in wrong order. 3/5 Conclusion includes some good points. 3.5/5 Good. Could have pointed out Virtual ATE theme.

10/15