1809810

by David Thomas

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Table of Contents

1. Element 1 10
1.1. Executive Summary 10

1.2. Research 11
1.2.1 NI DAQmx data acquisition used in LabVIEW 11
1.2.2 Digital Magnitude Comparators 14
1.2.3 Digital Design Methods using VHDL and IP Integration 16
1.2.4 Analogue to Digital Convertors 17
1.2.5 Instrumentation and Signal Conditioning 19
1.2.6 Load Cells – (LCKD-1Kg) 20

1.3. Design Requirements 21
1.3.1. Half Adder 21
1.3.2 Full Adder 22

1.4. Implementation 23
1.4.1 4-Bit Adder & Comparator 23
1.4.2. 8-Bit Adder & Comparator 26

1.5. Testing & Analysis 27
1.5.1. 4-Bit Testing & Analysis 27
1.5.2. 8-Bit Testing & Analysis 33

1.6. Evaluation 37

2. Element 2 38
2.1. Introduction 38

2.2. Design requirements 39
2.2.1. Load Cells & Signal Conditioning 39
2.2.2. 10 & 12 Bit Analogue to Digital Convertors 43

2.3. Implementation 46
2.3.1. 8-Bit Analogue to Digital Convertor 46
2.3.2. Magnitude Comparator 48

2.4. Testing and Analysis 51
2.4.1. Load Cells and Signal Conditioning 51
2.4.2. 10 & 12 Analogue to Digital Convertors 54
2.4.3. 8-Bit Analogue to Digital Convertor 56
2.4.4. Magnitude Comparator 58

2.5. Evaluation 62

3. Element 3 63
3.1. Introduction 63
3.2. Design requirements 64
3.3. Implementation 66
3.4. Testing and Analysis 67
3.5. Conclusions and Recommendations 73
4. Reference List 74
5. Appendix 77
5.1. Element 1 77
5.2. Element 2 78
5.2.1. Load Cell Testing 78
5.3. Element 3 82
5.3.1. Data Logging 82
5.3.2. 200 Gram Test Images 85
5.3.3. 500 Gram Test images 86
5.3.4. 700 Gram Test Images 87
5.3.5. 200 Gram Data 88
5.3.6. 500 Gram Data 95
5.3.7. 700 Gram Data 101

Good table of contents with good level of detail

Table of Figures

Figure 1 - Element 1 - NI DAQmx Block Diagram 11
Figure 2 - Element 1 - NI DAQmx Add Icon 11
Figure 3 - Element 1 - NI DAQmx Create Icon 12
Figure 4 - Element 1 - NI DAQmx Read Icon 12
Figure 5 - Element 1 - NI DAQmx Clear Icon 13
Figure 6 - Element 1 - NI DAQmx Digital Input 13
Figure 7 - Element 1 - NI DAQmx Digital Output 13
Figure 8 - Element 1 - 4-Bit Magnitude Comparator Logic 14
Figure 9 - Element 1 - 8-Bit Digital Magnitude Comparator 15
Figure 10 - Element 1 - VHDL Code, FPGA based algorithm 16
Figure 11 - Element 1 - Quantization Illustration 17
Figure 12 - Element 1 - Basic SAR ADC architecture 18
Figure 13 - Element 1 - ADC Comparison Chart 18
Figure 14 - Element 1 - Signal Conditioning System 19
Figure 15 - Element 1 - Dual micropower instrumentation amplifier 19
Figure 16 - Element 1 - Load cell 20
Figure 17 - Element 1 - Wheatstone Bridge 20
Figure 18 - Element 1 - 4 Bit Adder Logic 21
Figure 19 - Element 1 - Full Adder Logic 22
Figure 20 - Element 1 - 4-Bit Adder Block Diagram 23
Figure 21 - Element 1 - 4-Bit Adder Hierarchy 23
Figure 22 - Element 1 - VHDL Code 24
Figure 23 - Element 1 - 4-Bit Mag Comparator Block Diagram 25
Figure 24 - Element 1 - 4-Bit Mag Comparator PLD 25
Figure 25 - Element 1 - 8-Bit Adder Hierarchy 26
Figure 26 - Element 1 - 8-Bit Mag Comparator PLD 26
Figure 27 - Element 1 - 4-Bit Adder Simulation Testing 27
Figure 28 - Element 1 - 4-Bit Adder Programming for Simulation 28
Figure 29 - Element 1 - Magnitude Comparator Simulation Testing 28
Figure 30 - Element 1 - 4-Bit Magnitude Comparator Programming for Simulation 29
Figure 31 - Element 1 - 4-Bit Functional Testing AEQB 30
Figure 32 - Element 1 - 4-Bit Functional Testing AGTB 31
Figure 33 - Element 1 - 4-Bit Functional Testing ALTB 32
Figure 34 - Element 1 - 8-bit PLD Configuration 33
Figure 35 - Element 1 - 8-Bit Functional Testing AEQB 34
Figure 36 - Element 1 - 8-Bit Functional Testing ALTB 35
Figure 37 - Element 1 - 8-Bit Functional Testing AGTB 36
Figure 38 - Element 2 - Unity Gain Amplifier 39
Figure 39 - Element 2 - Unity Gain Amplifier Output 40
Figure 40 - Element 2 - Instrument Amplifier 41
Figure 41 - Element 2 - Load Cell 42
Figure 42 - Element 2 - LabView 10-bit ADC Design 43

Figure 43 - Element 2 - 10-Bit ADC 44
Figure 44 - Element 2 - LabView 12-bit ADC Design 44
Figure 45 - Element 2 - 12-Bit ADC 45
Figure 46 - Element 2 - 8-Bit ADC Design 46
Figure 47 - Element 2 - LabView Dual Variable Power Supply 47
Figure 48 - Element 2 - 8-Bit ADC Front Page 47
Figure 49 - Element 2 - FPGA Magnitude Comparator 48
Figure 50 - Element 2 - Magnitude Comparator LabView Front Page 49
Figure 51 - Element 2 - Multisim PLD 49
Figure 52 - Element 2 - PMOD Ports 50
Figure 53 - Element 2 - Load Cell 50% Load Test 51
Figure 54 - Element 2 - Load Cell 75% Load Test 51
Figure 55 - Element 2 - Load Cell 100% Load Test 52
Figure 56 - Element 2 - Load Cell Output 53
Figure 57 - Element 2 - 10-Bit ADC Test 54
Figure 58 - Element 2 - Element 2 -10-Bit ADC Test 54
Figure 59 - Element 2 - 12-Bit ADC Test 55
Figure 60 - Element 2 - 12-Bit ADC Test 55
Figure 61 - Element 2 - National Instruments Elvis II Board - Test 56
Figure 62 - Element 2 - 8-Bit ADC Test 56
Figure 63 - Element 2 - National Instruments Elvis II Board - Test 57
Figure 64 - Element 2 - 8-Bit ADC Test 57
Figure 65 - Element 2 - FPGA & Nexys Boards 58
Figure 66 - Element 2 - LabView - Less Than 59
Figure 67 - Element 2 - FPGA - Less Than 59
Figure 68 - Element 2 - LabView - Equal to 60
Figure 69 - Element 2 - FPGA - Equal to 60
Figure 70 - Element 2 - LabView - Greater Than 61
Figure 71 - Element 2 - FPGA - Greater Than 61
Figure 72 - Element 3 - FPGA Magnitude Comparator with Data Logging 64
Figure 73 - Element 3 - FPGA Magnitude Comparator Front Page 65
Figure 74 - Element 3 - File & File 2 Connections 66
Figure 75 - Element 3 - File 3, File 4 & File 5 Connections 66
Figure 76 - Element 3 - 200g Equal to Test 67
Figure 77 - Element 3 - 200g Test Result 68
Figure 78 - Element 3 - 500g Less Than Test 69
Figure 79 - Element 3 - 500g Test Result 70
Figure 80 - Element 3 - 700g Greater Than Test 71
Figure 81 - Element 3 - 700g Test Result 72
Figure 82 - Element 2 - Load Cell 55% Load Test 78
Figure 83 - Element 2 - Load Cell 60% Load Test 78
Figure 84 - Element 2 - Load Cell 65% Load Test 79
Figure 85 - Element 2 - Load Cell 70% Load Test 79
Figure 86 - Element 2 - Load Cell 80% Load Test 80

Figure 87 - Element 2 - Load Cell 85% Load Test 80
Figure 88 - Element 2 - Load Cell 90% Load Test 81
Figure 89 - Element 2 - Load Cell 95% Load Test 81
Figure 90 - Element 3 - Data Logging File 1 82
Figure 91 - Element 3 - Data Logging File 2 82
Figure 92 - Element 3 - Data Logging File 3 83
Figure 93 - Element 3 - Data Logging File 4 83
Figure 94 - Element 3 - Data Logging File 5 84
Figure 95 - Element 3 - 200g Less Than Test 85
Figure 96 - Element 3 - 200g Greater Than Test 85
Figure 97 - Element 3 - 500g Equal to Test 86
Figure 98 - Element 3 - 500g Greater Than Test 86
Figure 99 - Element 3 - 700g Equal to Test 87
Figure 100 - Element 3 - 700g Less Than Test 87

Table of figures is extensive and in good order

Table of Tables

Table 1 - Element 1 - 4 Bit Adder Truth Table 21
Table 2 - Element 1 - Full Adder Truth Table 22
Table 3 - Element 2 - Load Cell Testing 52
Table 4 - Element 3 - 200 Gram Data 94
Table 5 - Element 3 - 500 Gram Data 100
Table 6 - Element 3 - 700 Gram Data 107

Good use of tables

Table of Equations

Equation 1 - Element 2 - Unity Gain....39
Equation 2 - Element 2 - Buffer Gain....41
Equation 3 - Element 2 - Differential Amplifier Gain....41
Equation 4 - Element 2 - Amplifier Gain....41
Equation 5 - Element 2 - Load Cell Gain....42
Equation 6 - Element 2 - 10-Bit Formula Block....43
Equation 7 - Element 2 - 12-Bit Formula Block....44

Good use of tables

1. Element 1

1.1. Executive Summary

Good summary

The basis of Element 1 was the design, testing and implementation of a combinational program using Vivado design and Multisim software packages along with a Nexys DDR FPGA development board. Successful final design required each elemental part to be designed, built and tested individually.

Using VHDL, a 4-bit adder and magnitude comparator combinational logic system was designed, built and tested. Following this, the final 8- bit magnitude comparator was tested and implemented, allowing the results to be analysed once the software operation was proven to be successful.

1.2. Research

1.2.1 NI DAQmx data acquisition used in LabVIEW

NI DAQmx is the latest generation driver used for data acquisition in NI LabVIEW. It differs from its predecessor, the traditional NI DAQ in that a large number of architectural changes have been made to significantly advance its performance. (National.Instruments, 2020)

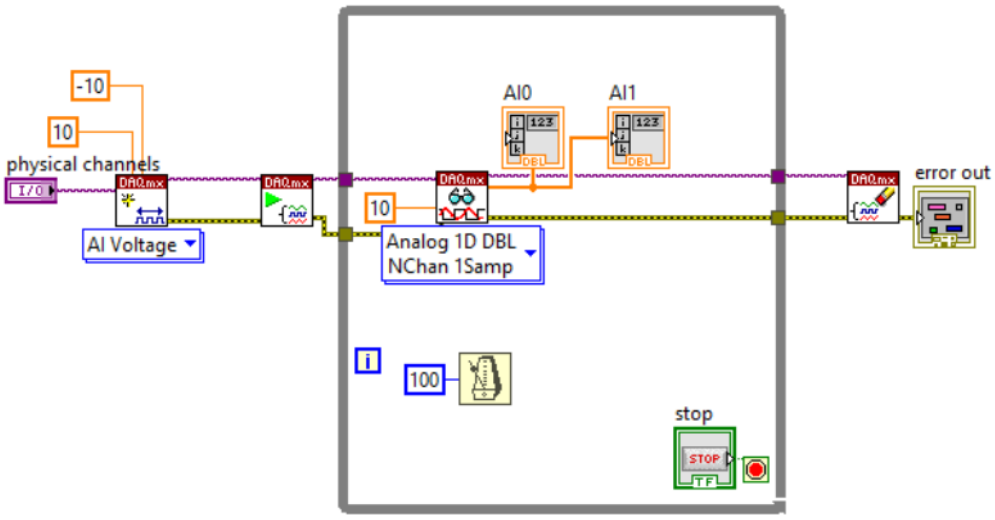


Figure 1 - Element 1 - NI DAQmx Block Diagram

(National.Instruments, 2020)

Illustrated above is the block diagram created in NI DAQmx, within which are several icons with differing uses and operations.



Figure 2 - Element 1 - NI DAQmx Add Icon

(National.Instruments, 2020)

The 'Add' icon sums the values of inputs x and y.

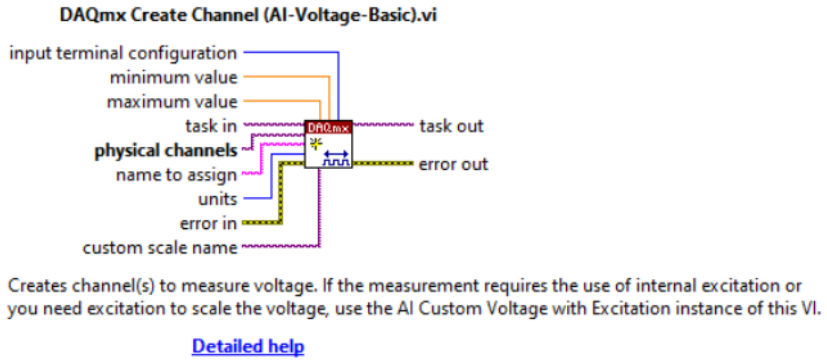


Figure 3 - Element 1 - NI DAQmx Create Icon

(National.Instruments, 2020)

The 'Create' icon shown above acts as a virtual channel. Variables, such as voltage, can be created and measured, and are also able to be scaled for input and output. 'Task In' acts as the virtual channel input, while 'Physical Channels' takes the output from the connected devices.

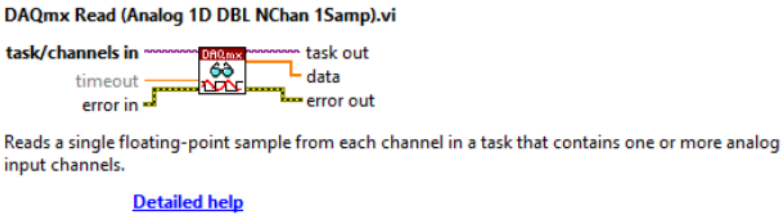


Figure 4 - Element 1 - NI DAQmx Read Icon

(National.Instruments, 2020)

A specified input will be read by the 'Task' icon, as shown above. Both analogue and digital signals can be generated as a result of the number and variety of options available, allowing the acquisition of specific data from selected channels or samples.

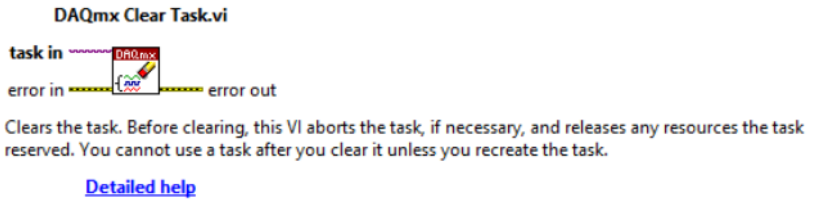


Figure 5 - Element 1 - NI DAQmx Clear Icon

(National.Instruments, 2020)

Deletion of tasks is achieved using the "Clear' icon. However, prior to performing this, useful resources are released that were reserved within the task.

Digital Input

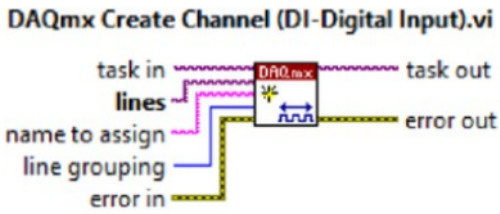


Figure 6 - Element 1 - NI DAQmx Digital Input

(National.Instruments, 2020)

Illustrated above is the digital input icon which incorporates several parameters to allow for either the generation of a single channel, or multiple channels, by combining or separating digital lines respectively. As with the function of the analogue input, only digital signals can be measured by the digital input.

Digital Output

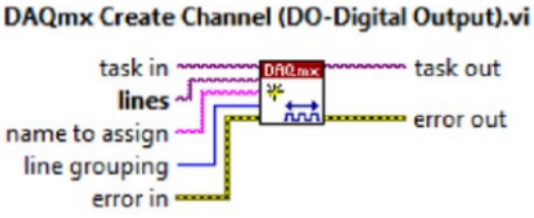


Figure 7 - Element 1 - NI DAQmx Digital Output

(National.Instruments, 2020)

A good explanation of the LabVIEW design with the DAQ interface blocks identified

As with the digital input described above, multiple or single channels can be generated by the digital output.

1.2.2 Digital Magnitude Comparators

Digital magnitude comparators allow for a comparison of two inputs using a range of logic gates, most commonly in the form of AND, NOT and XNOR. The magnitude comparator shown below contains three output terminals (for defined conditions), which generates the compared or output value by assessing given or provided / inputted values. (Electrical4U, 2020)

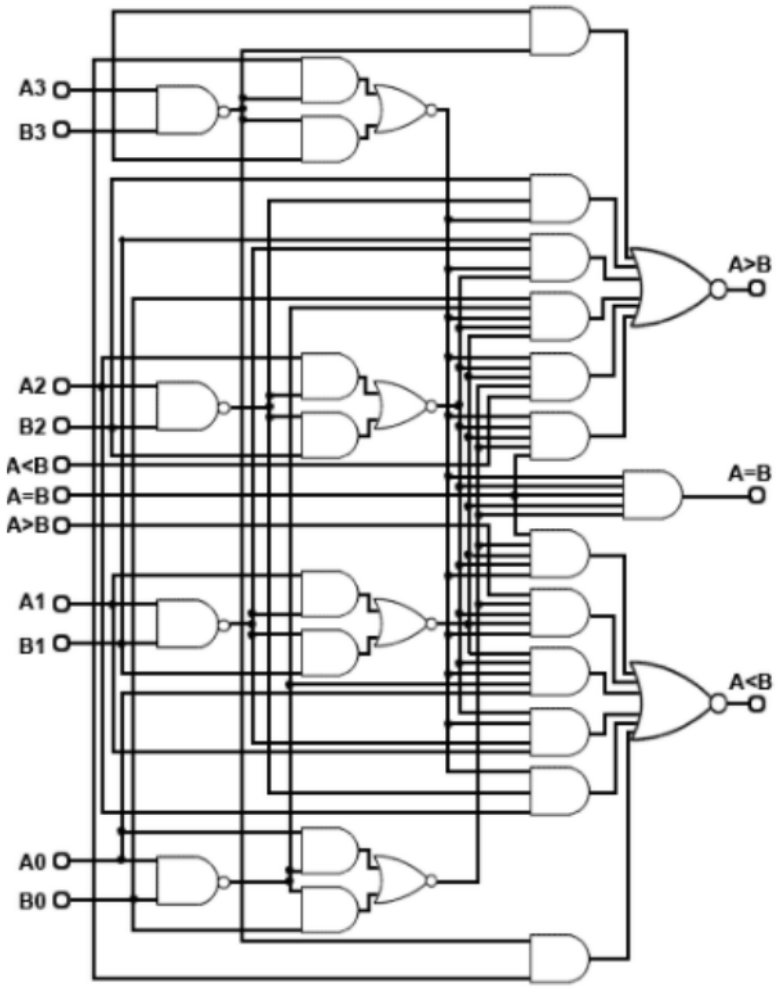


Figure 8 - Element 1 - 4-Bit Magnitude Comparator Logic

(Coates, 2020)

Illustrated above is an example of logic for a 4-bit magnitude comparator. Instead of extending the block logic, it is cascaded with a second 4-bit magnitude comparator which, in turn, creates an 8-bit magnitude comparator (as shown below).

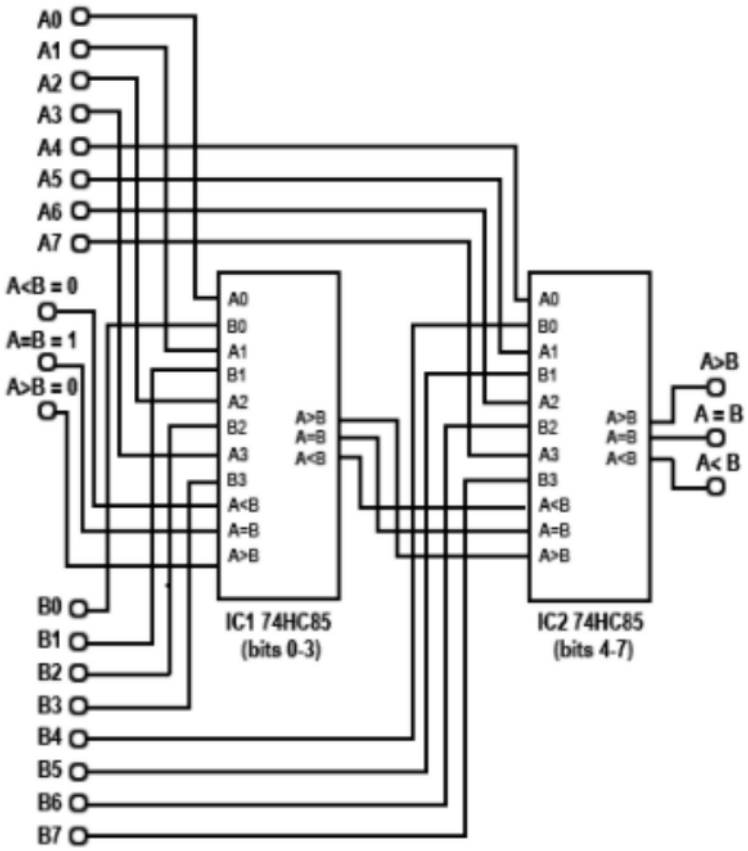


Figure 9 - Element 1 - 8-Bit Digital Magnitude Comparator

(Coates, 2020)

Further cascading allows for the creation of additional capacity. A typical system will operate by initially comparing the most significant parts/bits to ensure inputs are equivalent, progressing in sequence to compare every part of the system. As part of this process, by comparing large binary numbers, the magnitude comparators aim to associate one of three relationships of A to B:

A>B: (A greater than B)

A=B: (A equal to B)

A<B: (A less that B)

As such digital magnitude comparators are found widely in communication and technology industries. (Electronics-Tutorial, 2020)

Explained very well and shows a good understanding which is crucial to this element

1.2.3 Digital Design Methods using VHDL and IP Integration

VHDL, (VHSIC-HDL), Very High-Speed Integrated Circuit Hardware Description Language, is an adaptable hardware description programming language used in both mixed-signal and digital systems, commonly field-programmable gate arrays (FPGA) or integrated circuits (ASIC). Its adaptability and use as a programming language in these circuits allows for a result to be obtained through a variety of methods and tools. The use of VDHL in electronic design automation is under the regulation of the IEEE. (Spiegel, 2001)

```
entity PID_Controler is
      Generic(Kp : std_logic_vector(7 downto 0) := B"11111010";
               Kv : std_logic_vector(7 downto 0) := B"00111100";
               Ki : std_logic_vector(7 downto 0) := B"00111100");
      Port(Actual_input : in  STD_LOGIC_VECTOR (29 downto 0);
        Dsired_input : in  STD_LOGIC_VECTOR (29 downto 0);
        PID_control : out  STD_LOGIC_VECTOR (34 downto 0);
        Reset : in  STD_LOGIC;
        CLK : in  STD_LOGIC;
        Sample_clk : in  STD_LOGIC);
end PID_Controler;
----------------------------------------------------------------------
architecture Behavioral of PID_Controler is
----------------------------------------------------------------------
------Signals definitions
----------------------------------------------------------------------
signal Actual_input_buf : std_logic_vector(39 downto 0);
signal Desired_input_buf : std_logic_vector(39 downto 0);
signal Error_gain : std_logic_vector(47 downto 0);
signal Error_diff : std_logic_vector(39 downto 0);
signal Error_integral : std_logic_vector(39 downto 0);
signal Error : std_logic_vector(39 downto 0);
signal Error_diff_gain : std_logic_vector(47 downto 0);
signal Error_integral_gain : std_logic_vector(47 downto 0);
signal PID_control_buf : std_logic_vector(39 downto 0);
```

Figure 10 - Element 1 - VHDL Code, FPGA based algorithm

(Taghizadegan, 2016)

IP (Intellectual Property) integration is a reusable component used in electronic chips, that remains the intellectual property of the party. It is most commonly a unit of logic, cell or integrated circuit.

Incorporation of IP provides the chip with a degree of adaptability. Use of a diverse layout allows the chip to perform a number of high-speed complex functions, whilst retaining the ability to be reconfigured for additional use if needed. (IEEE, 2004)

Coverage is good on this and the IP design method has been identified

1.2.4 Analogue to Digital Convertors

In order to generate a digital signal output that is illustrative of the signal of the analogue input, an analogue to digital convertor (ADC) is necessary. However, the quality of the digital signal generated is variable, and is related to the sampling frequency, or resolution (samples per second) of the analogue input signal.

In order to generate an accurate depiction of the analogue input signal, the quantization error; variation between the analogue input signal and closest representative digital output signal, should be minimized. As such, an ADC with a higher number of bits per analogue has a smaller quantization error, and therefore a higher resolution. Any quantization error also results in the introduction of noise, referred to as quantization noise. (Arar, 2019)

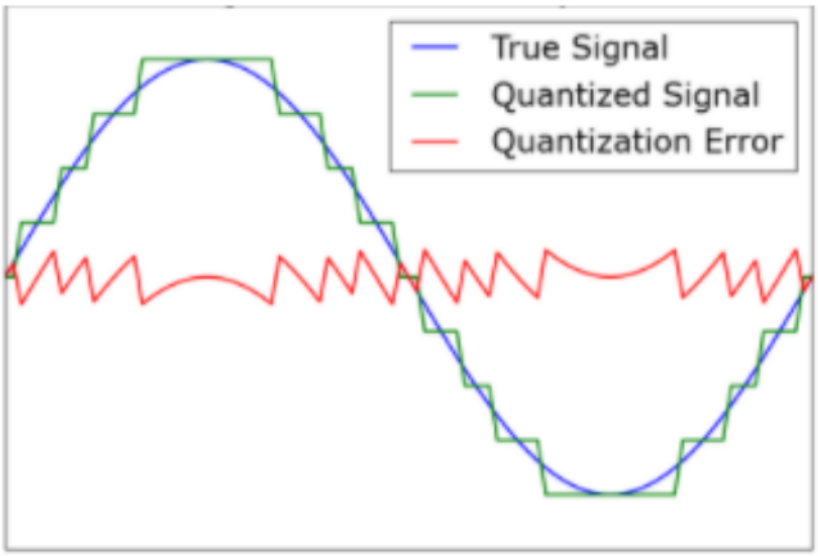


Figure 11 - Element 1 - Quantisation Illustration

(Swiston, 2014)

A commonly used ADC is the Successive approximation register (SAR), which can be used for a large variety of applications. It has the ability to sustain a high sample frequency with very little latency and can be obtained in a series of resolutions up to 18bits. (Arar, 2019)

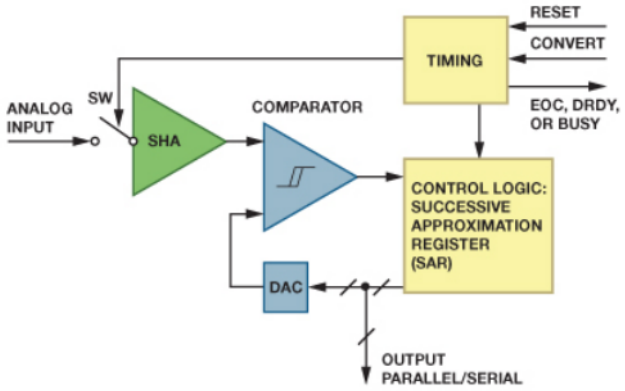


Figure 12 - Element 1 - Basic SAR ADC architecture

(Xie, 2013)

Illustrated above are the four main sub-circuits constructed for SAR ADC's. The sub circuits compromise of: SHA - sample and hold comparator, DAC, and SAR.

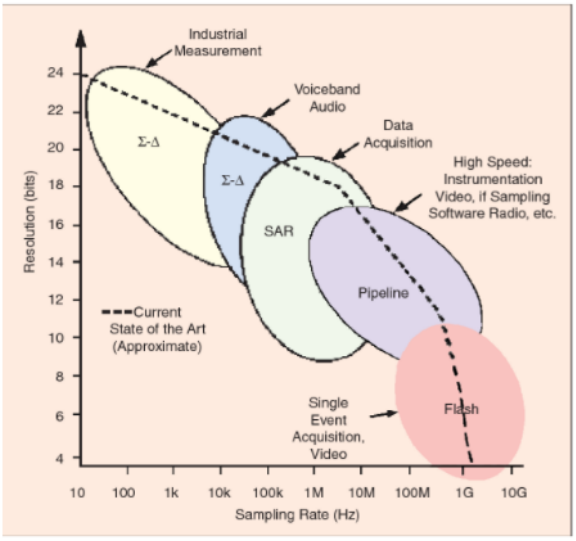


Figure 13 - Element 1 - ADC Comparison Chart

(Blair, 2005)

Explanation is very good supported with good images

The above chart illustrates the relationship between resolution and sampling rate for different ADC types. The resolution is represented by the vertical axis, while the horizontal axis represents the sampling rate. It can be seen from the chart that there is overlap between the ADC architecture, illustrating their appropriateness for multiple applications. However, consideration of key factors such as required resolution and sampling frequency are essential to selection of most appropriate ADC. (Kester, 2005)

1.2.5 Instrumentation and Signal Conditioning

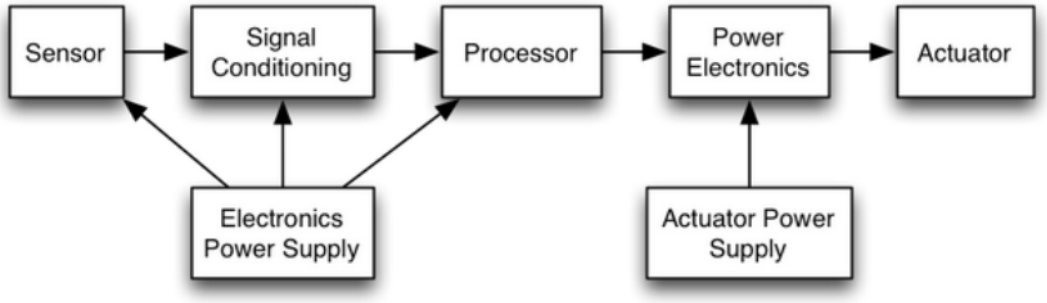


Figure 14 - Element 1 - Signal Conditioning System

(Chegg, 2020)

Signal conditioning ensures that analogue signals are manipulated in order to meet the next stage's processing requirements. In the case of electronics this may be the limiting of voltage or current in ADCs. The block diagram above illustrates the process of signal conditioning between a sensor, processor, and output of an actuator.

At the first stage, the transducer stage, following detection, the input is transduced electrically, before processing the output to a signal suitable to operate as an output. (EEE_Guide, 2020)

Good work here which demonstrates your knowledge of the methods

Illustrated below is an ECG circuit, a current example of high precision low power signal conditioning. The ECG circuit operates by measuring a voltage generated by a heartbeat, however the small signal, in the range of 0.2mv to 2.0mv peak to peak and a 0.5Hz to 150Hz bandwidth, presents a number of obstacles to conditioning . (Analogue_Devices, 2020)

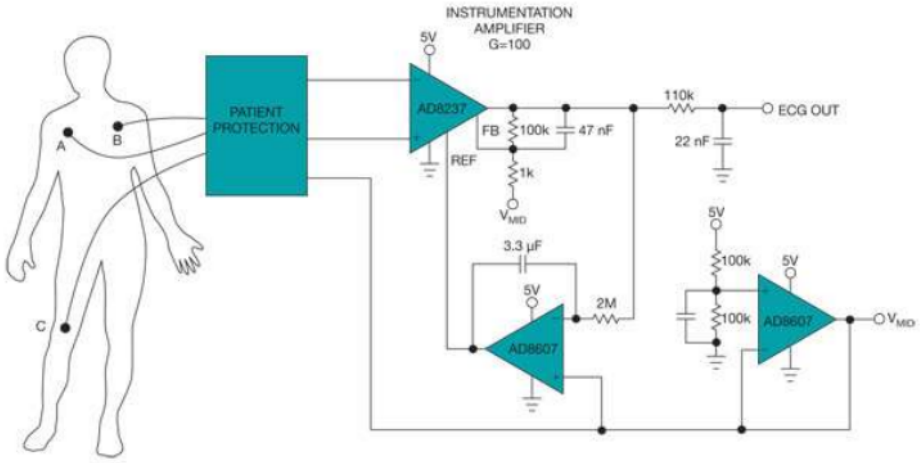


Figure 15 - Element 1 - Dual micropower instrumentation amplifier

(Aspencore, 2020)

1.2.6 Load Cells – (LCKD-1Kg)

Load cells are a class of sensor that are used to convert mass, most commonly the weight of an object, into a resultant electrical signal. They often incorporate an instrument such as a strain gauge, which contains an in-built miniature circuit board, to compensate for temperature.

LCKD, manufactured with a robust alloy stainless steel housing by a number of companies including Omega, are the load cells most commonly seen. With the ability to operate over a wide range of weights, from 1kg to 1000lbs, a large number of different load cells are available dependent of the mass of the object(s) to be weighed and the units (imperial or metric) desired. (Omega-Engineering, 2019)



Figure 16 - Element 1 - Load cell

(Farnell, 2020)

Being accurate and versatile, strain gauge load cells are most often seen in the industrial setting. They operate by measuring the change (reduction) in resistance as the mass of the object causes compression in the strain gauge. Use of a single gauge makes the accuracy of any one measurement limited as the change in resistance is very small, however by connecting and grouping a number of gauges together, a more quantifiable value is obtained, significantly improving the accuracy. An example of this is a Wheatstone bridge, in which four strain gauges are connected. (Aspencore, 2020)

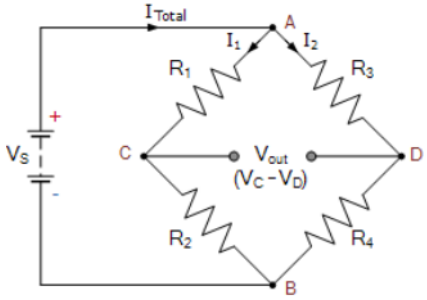


Figure 17 - Element 1 - Wheatstone Bridge

(Aspencore, 2020)

Explanation is good and all the research in this section is supported significantly with relevant sources

1.3. Design Requirements

1.3.1. *Half Adder*

The first stage used Vivado software to design a combinational logic system using VHDL and IP integration. Initial design of a half adder is required as it forms one of the blocks that will be used to construct a 4-bit adder. In order to design the system, a half ladder logic diagram/schematic and truth table are created to enable determination of the logic (see below).

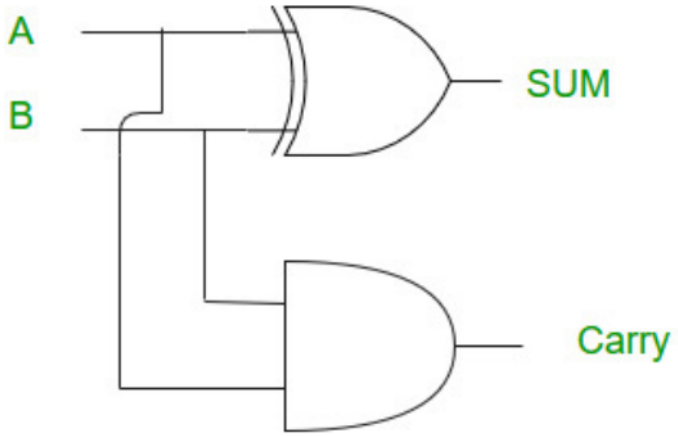


Figure 18 - Element 1 - 4 Bit Adder Logic

(Geeksforgeeks, 2020)

Half Adder Truth Table			
A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Table 1 - Element 1 - 4 Bit Adder Truth Table

1.3.2 *Full Adder*

Once built, the half adder is then duplicated to create a full adder. Due to the hierarchy system built into the Vivado software, each individual system will be placed to construct the required design of a 4-bit adder.

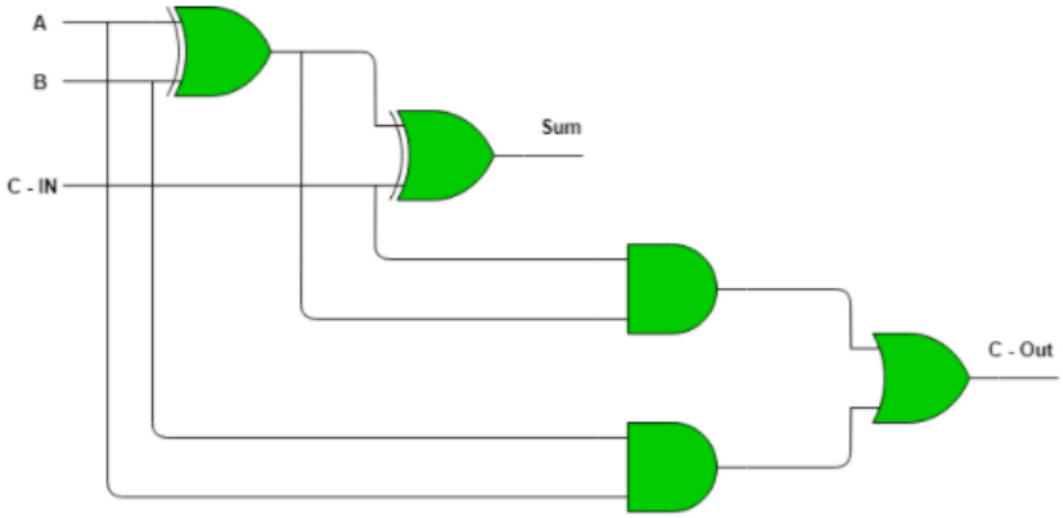


Figure 19 - Element 1 - Full Adder Logic

(Geeksforgeeks, 2020)

Full Adder Truth Table				
Cin	B	A	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Table 2 - Element 1 - Full Adder Truth Table

1.4 Implementation

1.4.1 *4-Bit Adder & Comparator*

With the full adder built and proven, the 4-bit adder can then be built by combining duplicating 4 full adders, the hierarchy system in the Vivado software then arranging the full adders and half adders to provide the required outputs of a 4-bit adder.

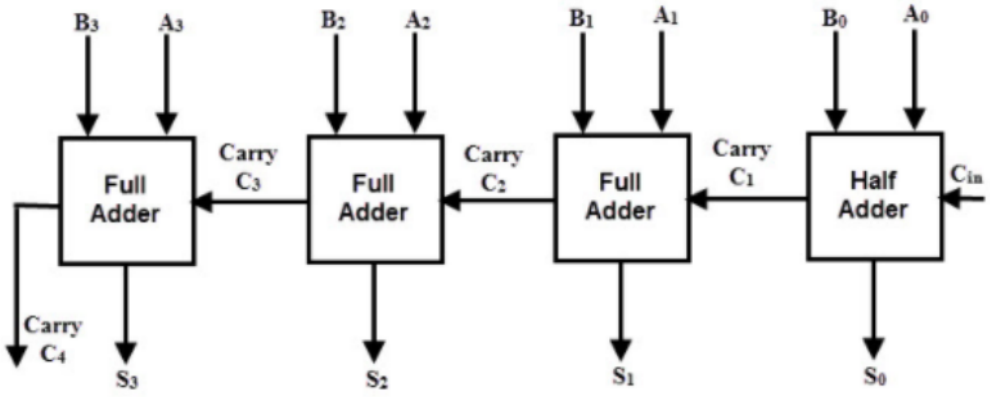


Figure 20 - Element 1 - 4-Bit Adder Block Diagram

(X.Ellis, Unknown)

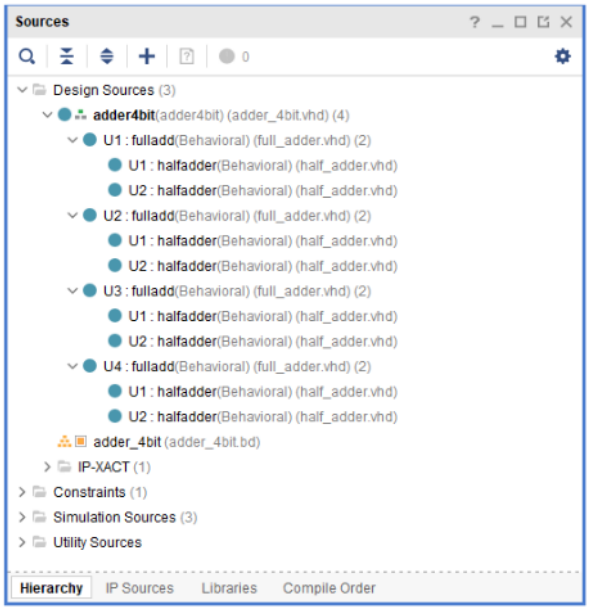


Figure 21 - Element 1 - 4-Bit Adder Hierarchy

Excellent work. The 4 bit adder hierarchy and inheritance has been identified and explained very well. All the components are explained.

The image above displays the hierarchy system of a 4-bit adder. Within each separate bit is a full adder that consists of two half adders. Once the system had been tried and tested, it was then designed using VHDL.

Illustrated below is the VHDL code that was used for the 4-bit adder.

```
1  library IEEE;
2  use IEEE.std_logic_1164.all;
3  entity adder4bit is
4  port(
5  cin : in STD_LOGIC;
6  a0 : in STD_LOGIC;
7  a1 : in STD_LOGIC;
8  a2 : in STD_LOGIC;
9  a3 : in STD_LOGIC;
10
11 b0 : in STD_LOGIC;
12 b1 : in STD_LOGIC;
13 b2 : in STD_LOGIC;
14 b3 : in STD_LOGIC;
15
16 cout : out STD_LOGIC;
17 s0 : out STD_LOGIC;
18 s1 : out STD_LOGIC;
19 s2 : out STD_LOGIC;
20 s3 : out STD_LOGIC
21 );
22 end adder4bit;
```

```
24 architecture adder4bit of adder4bit is
25 component fulladd
26 port (
27 a : in STD_LOGIC;
28 b : in STD_LOGIC;
29 cin : in STD_LOGIC;
30 cout : out STD_LOGIC;
31 s : out STD_LOGIC
32 );
33 end component;
34 signal c1 : STD_LOGIC;
35 signal c2 : STD_LOGIC;
36 signal c3 : STD_LOGIC;
37 begin
38 U1 : fulladd
39 port map(
40 a => a0, b => b0, cin => cin, cout => c1,
41 s => s0);
42 U2 : fulladd
43 port map(
44 a => a1, b => b1, cin => c1, cout => c2,
45 s => s1);
46 U3 : fulladd
47 port map(
48 a => a2, b => b2, cin => c2, cout => c3,
49 s => s2);
50 U4 : fulladd
51 port map(
52 a => a3, b => b3, cin => c3, cout => cout,
53 s => s3);
54 end adder4bit;
55
```

Figure 22 - Element 1 - VHDL Code

The code lines 1 to 22 display the entity, detailing the designated ports for the blocks. The architecture i.e. function(s) of each specific entity and their associated links to the logics, are shown in code lines 24 to 36. Finally, code lines 37 to 54 map the correct port for each entity. Within the Vivado software, the hardware description of the component, including logic, entity, and input/output operations, is contained within source files, whereas the mapping of process variables to physical inputs/outputs is held in constraint files

Good work and the code looks very neat and tidy

Illustrated below, an input/output of the comparator is created by combining the 4-bit adder, with outputs 'AGTB', 'AEQB' and 'ALTB' corresponding to LED displays that will illuminate on the Nexys DDR board. The output from the adder also acts as the input for the comparator, the comparator then evaluating the input value against the set point value, determined by the combined values of inputs 'A'.

Demonstrated in the block diagram is intellectual property, IP.

IP integration is demonstrated and backed up with a good explanation.

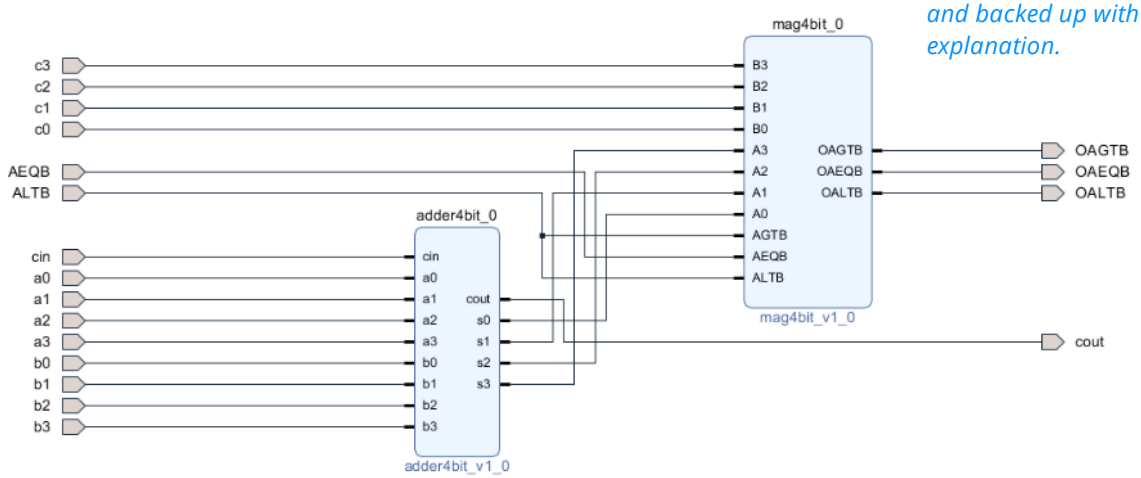


Figure 23 - Element 1 - 4-Bit Mag Comparator Block Diagram

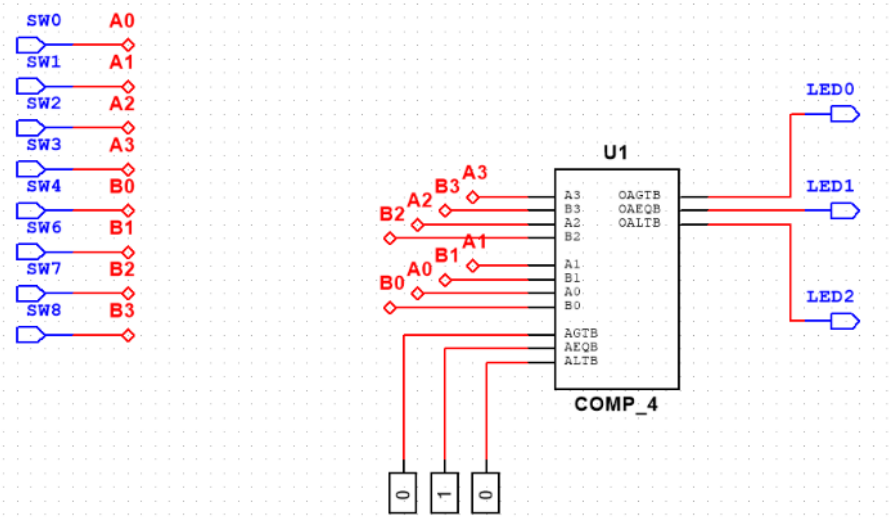


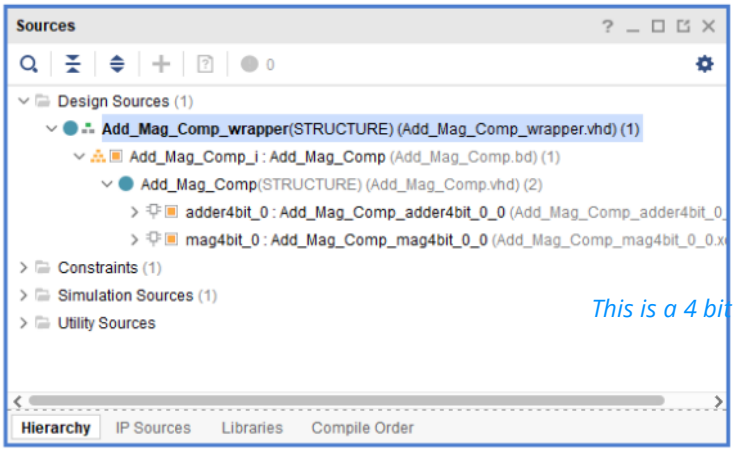
Figure 24 - Element 1 - 4-Bit Mag Comparator PLD

In order to perform the functional testing process of the comparator, a 4-bit mag comparator was built using Multisim's PLD software, enabling download to Nexys DDR board. Expander inputs are set with a constant digital high or low to allow for the 'compare' function of the design to work.

1.4.2. *8-Bit Adder & Comparator*

This is a 4 bit adder and 4 bit comparator

Once the 4-bit adder and comparator had been tested and its function proven, the 8-bit adder is created by combining two 4-bit adders and comparators. The hierarchy of the Vivado software then packages the program.



Good source design image showing no errors and IP design created

This is a 4 bit adder and 4 bit comp

Figure 25 - Element 1 - 8-Bit Adder Hierarchy

Error here: should be 4 bit hierarchy

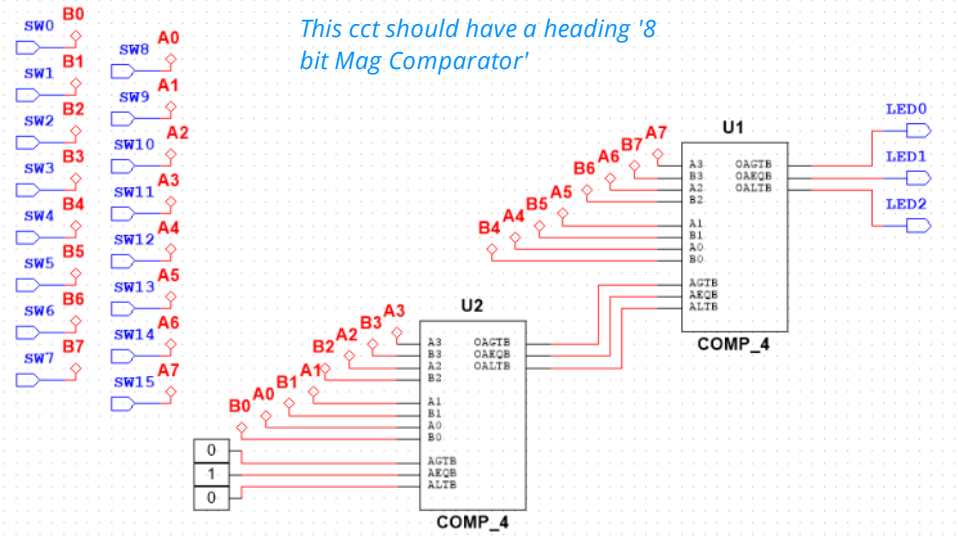


Figure 26 - Element 1 - 8-Bit Mag Comparator PLD

In order to perform the functional testing process of the comparator, an 8-bit mag comparator was built using Multisim's PLD software, enabling download to Nexys DDR board. Expander inputs are set with a constant digital high or low to allow for the 'compare' function of the design to work:

- AGTB and ALTB are digital low
- AEQB is set as a digital high.

Good explanation here which offers a different method of SOC design for simpler circuits

1.5 Testing & Analysis

On completion of each design stage, each version of the adders was subsequently tested to verify the correct design and functionality.

1.5.1. *4-Bit Testing & Analysis*

The 4-bit adder and magnitude comparator are both tested in simulation method within the Vivado software. For the 4-bit adder simulation test, inputs are placed into a virtual bus prior to input and output values being assigned. By changing input 'a' and 'b' values, three simulated tests were conducted with varied 's' output values. In order to provide value clarity, binary inputs were substituted for digital numerical outputs. The output values of 'a' and 'b' are then compared by the magnitude comparator, resulting in one of three outputs to be indicated, 'ALTB', 'AEQB' or 'AGTB'.

Good work and good use of the virtual bus to display results.

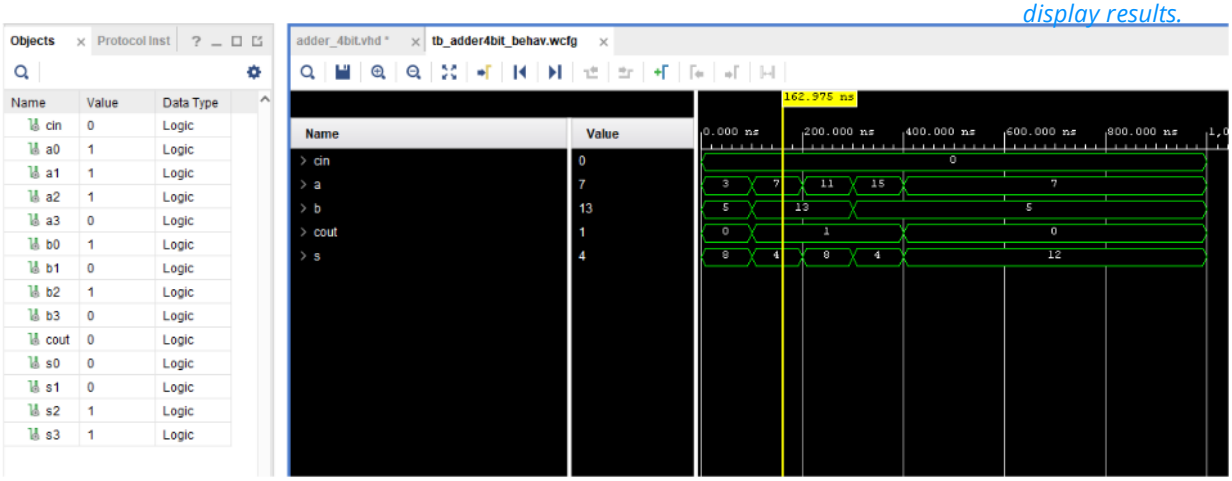


Figure 27 - Element 1 - 4-Bit Adder Simulation Testing

```
59      stimuli : process
60      begin
61          -- EDIT Adapt initialization as needed
62          cin <= '0';
63          a0 <= '1';
64          a1 <= '1';
65          a2 <= '0';
66          a3 <= '0';
67          b0 <= '1';
68          b1 <= '0';
69          b2 <= '1';
70          b3 <= '0';
71  wait for 100 ns;
72   cin <= '0';
73          a0 <= '1';
74          a1 <= '1';
75          a2 <= '1';
76          a3 <= '0';
77          b0 <= '1';
78          b1 <= '0';
79          b2 <= '1';
80          b3 <= '1';
81  wait for 100 ns;
82   cin <= '0';
```

Good example of test data

Figure 28 - Element 1 - 4-Bit Adder Programming for Simulation

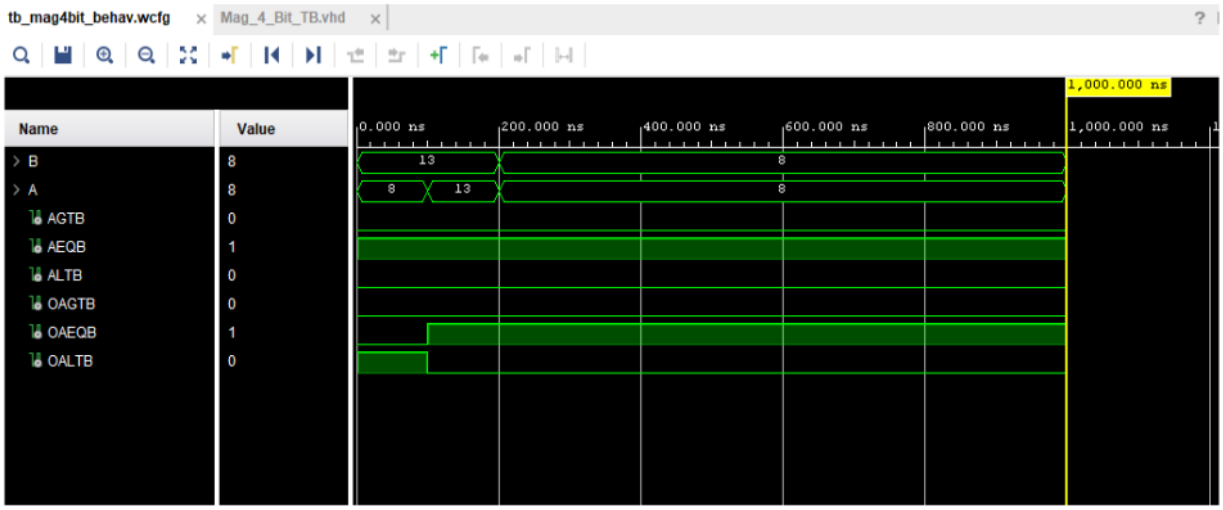


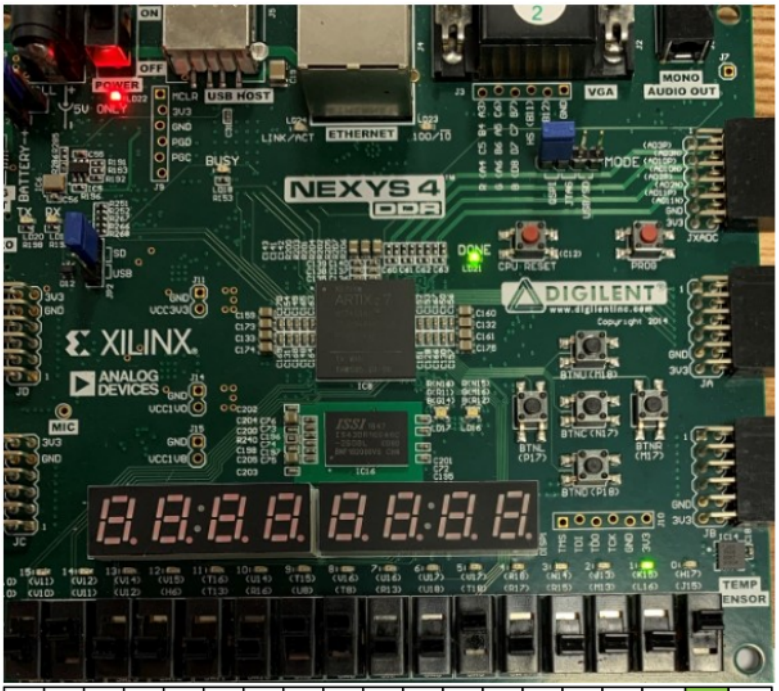
Figure 29 - Element 1 - Magnitude Comparator Simulation Testing

Good work here and good test data used to get all 3 results. You have also identified the static variable links from the Sim circuit.

```
62          B3 <= '1';
63          B2 <= '1';
64          B1 <= '0';
65          B0 <= '1';
66          A3 <= '1';
67          A2 <= '0';
68          A1 <= '0';
69          A0 <= '0';
70          AGTB <= '0';
71          AEQB <= '1';
72          ALTB <= '0';
73      wait for 100 ns;
74          B3 <= '1';
75          B2 <= '1';
76          B1 <= '0';
77          B0 <= '1';
78          A3 <= '1';
79          A2 <= '1';
80          A1 <= '0';
81          A0 <= '1';
82          AGTB <= '0';
83          AEQB <= '1';
84          ALTB <= '0';
85      wait for 100 ns;
86          B3 <= '1';
87          B2 <= '0';
88          B1 <= '0';
89          B0 <= '0';
90          A3 <= '1';
91          A2 <= '0';
92          A1 <= '0';
93          A0 <= '0';
94          AGTB <= '0';
95          AEQB <= '1';
96          ALTB <= '0';
97      wait for 100 ns;
```

Figure 30 - Element 1 - 4-Bit Magnitude Comparator Programming for Simulation

With the simulation testing proven to have been successful, the 4-bit adder and combinational logic are downloaded to a Nexys 4DDR board for functional testing. The practical testing consisted of three tests: Less than (<), greater than (>) and equal to (=). Three LED's on the Nexys 4DDR board were assigned outputs to correspond with the test results: LED 0, A greater than B; LED 1, A equal to B; LED 2, A less than B.



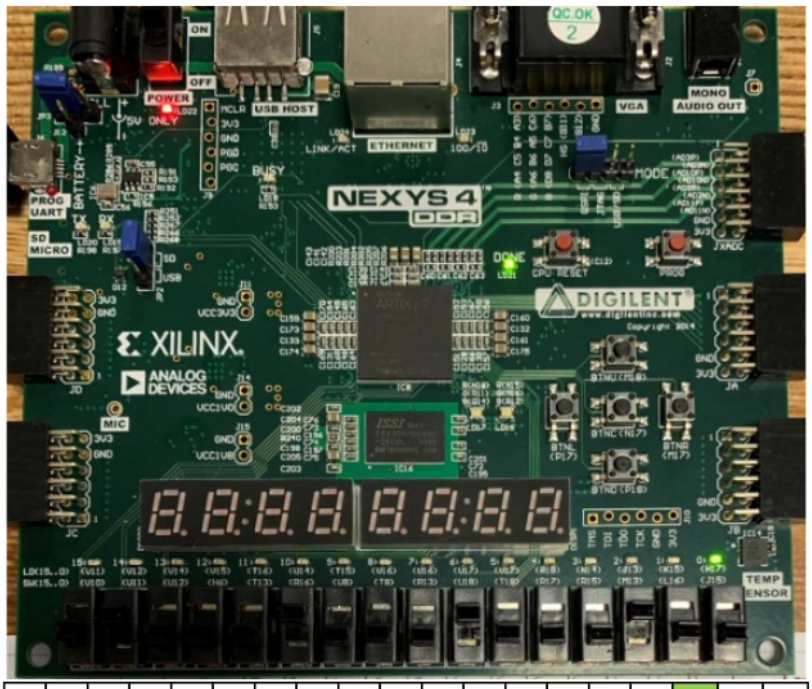
S15	S14	S13	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1	S0			
CIN	ALTB = '1'	AEQB '0'		C3	C2	C1	C0	B3	B2	B1	B0	A3	A2	A1	A0	LED 0	LED 1	LED 2
				Set Value				Sum of B				Sum of A						
Test 1				0	0	1	1	0	0	1	0	0	0	1	1	AGTB	AEQB	ALTB
Test decimal Values				3				2				1						

Test Results		
	(Sum of A + Sum of B)	3
	Set Value of C	3
		A Equal to B

Figure 31 - Element 1 - 4-Bit Functional Testing AEQB

Excellent work with the table of values indicating the settings on the FPGA board. Good test carried out

For the 'equal to' test illustrated above, the set point was assigned a binary value by selecting the on-off switches on the Nexys 4DDR board. The toggle switches for the sum of values for 'a' and 'b' are then selected to a matching binary input value of the set point, with the sum of 'a' and 'b' matching the set point value. Illumination of LED 1 indicates the test result of 'a' is equal to 'b'.



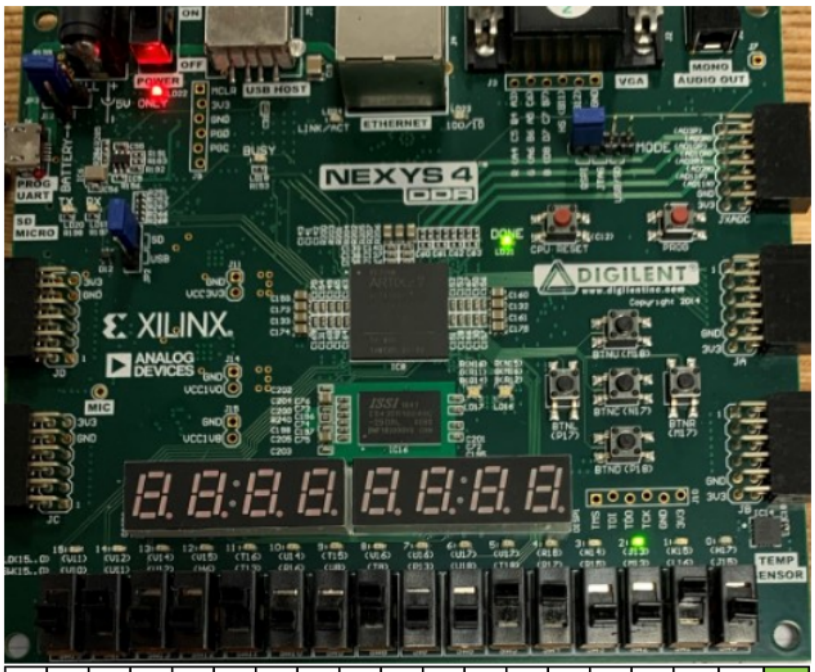
S15	S14	S13	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1	S0			
CIN	ALTB = '1'	AEQB '0'		C3	C2	C1	C0	B3	B2	B1	B0	A3	A2	A1	A0	LED 0	LED 1	LED 2
				Set Value				Sum of B				Sum of A						
Test 2				0	1	0	0	0	1	0	0	0	1	0	0	AGTB	AEQB	ALTB
Test decimal Values				4				4				4						

Test Results		
	(Sum of A + Sum of B)	8
	Set Value of C	4
		A Greater than B

Very good test result

Figure 32 - Element 1 - 4-Bit Functional Testing AGTB

For the greater than test illustrated above, the set point was assigned a binary value by selecting the on-off switches on the Nexys 4DDR board. The toggle switches for the sum of vales for ‘a’ and ‘b’ are then selected to a greater binary input value of the set point, with the sum of ‘a’ and ‘b’ being greater than the set point value, LED 0 is illuminated, indicating the test result of ‘a’ is greater than ‘b’.



S15	S14	S13	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1	S0			
CIN	ALTB = '1'	AEQB '0'		C3	C2	C1	C0	B3	B2	B1	B0	A3	A2	A1	A0	LED 0	LED 1	LED 2
				Set Value				Sum of B				Sum of A				AGTB	AEQB	ALTB
Test 3				1	0	0	1	0	0	1	1	0	0	1	0			
Test decimal Values				9				3				2						

Test Results	(Sum of A + Sum of B)	5
	Set Value of C	9
		A Less than B

A full set of good test results

Figure 33 - Element 1 - 4-Bit Functional Testing ALTB

For the 'less than' test illustrated above, the set point was assigned a binary value by selecting the on-off switches on the Nexys 4DDR board. The toggle switches for the sum of vales for 'a' and 'b' are then selected to a lesser binary input value of the set point, with the sum of 'a' and 'b' being less than the set point value. Illumination of LED 2 indicated the test result of 'a' is less than 'b'.

In conclusion, from the simulated and functional testing conducted, the 4-bit adder is functioning as required.

1.5.2. *8-Bit Testing & Analysis*

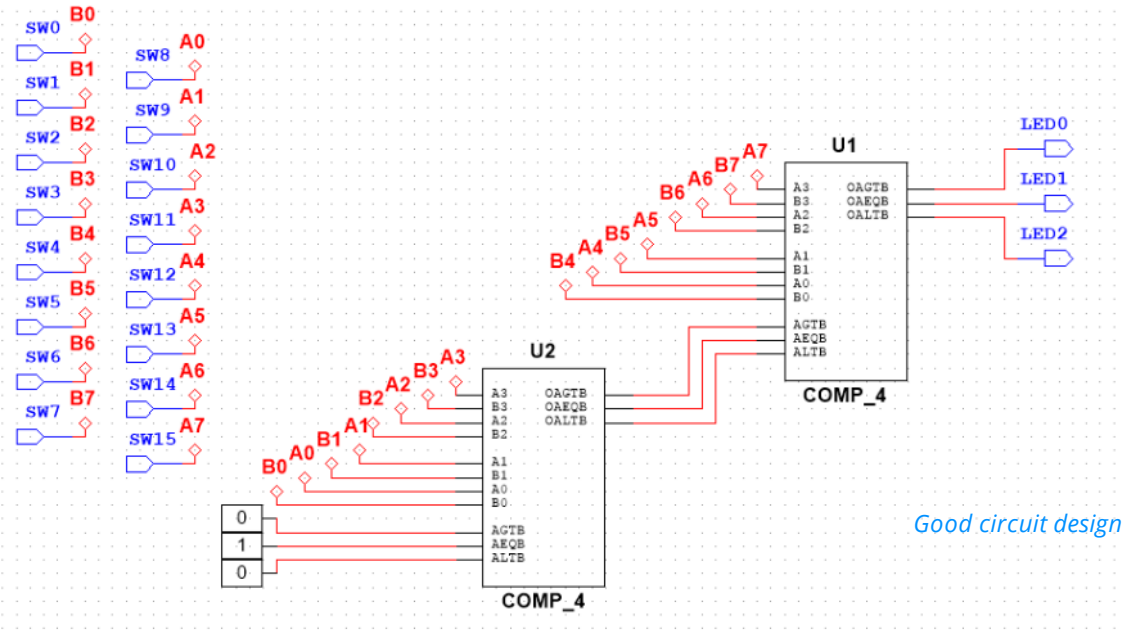
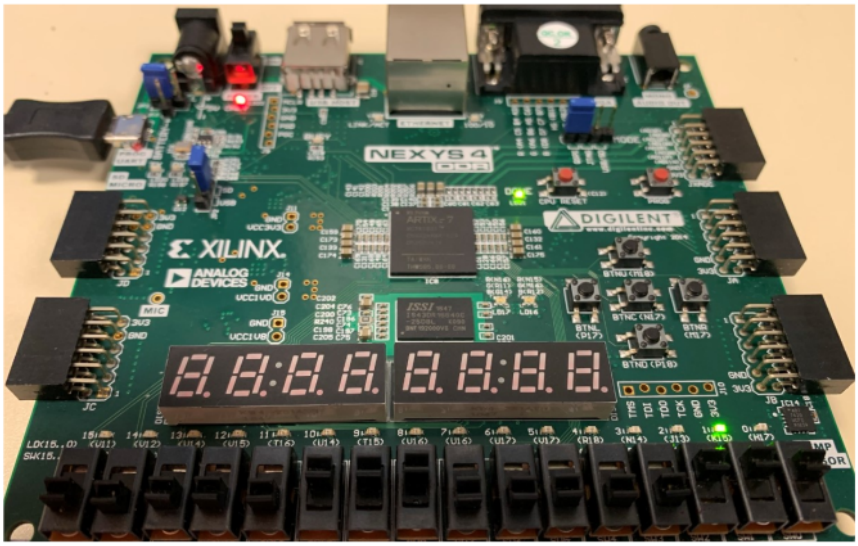


Figure 34 - Element 1 - 8-bit PLD Configuration

An 8-bit adder and logic system are built using PLD in Multisim. The system is then downloaded to the Nexys 4DDR board for functional testing.

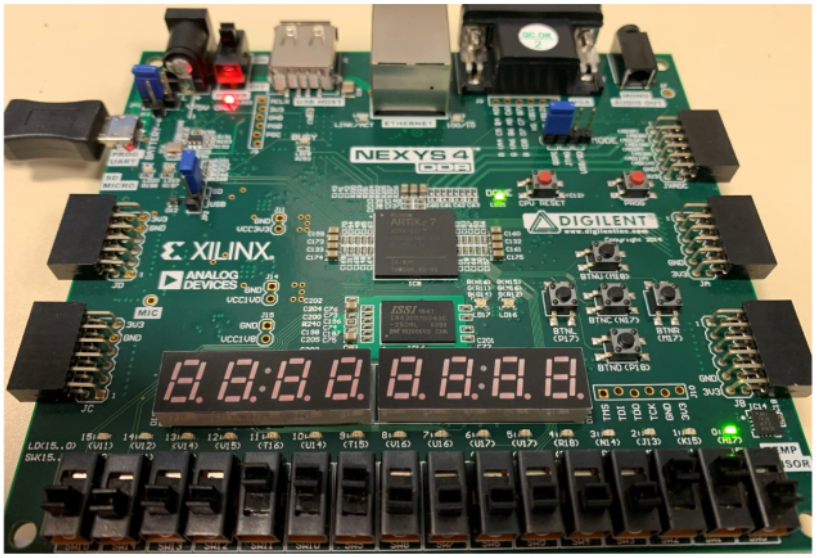


B								A										
S15	S14	S13	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1	S0			
0	0	0	0	0	1	1	1	0	0	0	0	0	1	1	1	LED 0	LED 1	LED 2
7								7								ALTB	AEQB	AGTB

Test Results	Value of A	7
	Value of B	7
		A Equal to B

Figure 35 - Element 1 - 8-Bit Functional Testing AEQB

For the 'equal to' test, illustrated in the image above, the values of inputs 'a' and 'b' are set with an equal binary value, by selecting the toggle switches on the Nexys 4DDR board. When the equal value of both 'a' and 'b' are selected, LED 1 is illuminated, signalling that 'a' is equal to 'b'.

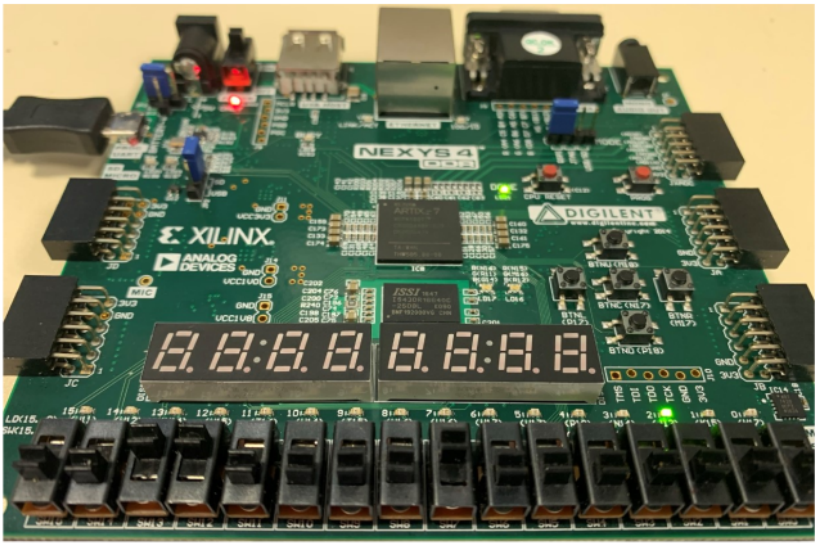


B								A										
S15	S14	S13	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1	S0			
0	0	0	0	1	0	0	1	0	0	0	0	0	1	0	1	LED 0	LED 1	LED 2
9								5										

Test Results	Value of A	5
	Value of B	9
		A Less than B

Figure 36 - Element 1 - 8-Bit Functional Testing ALTB

For the 'less than' test, illustrated in the image above, the values of inputs 'a' and 'b' are set with different binary values, by selecting the toggle switches on the Nexys 4DDR board. For the test, the binary code for the digital value of 9 was selected for 'b', whist the binary code for the digital value of 5, was selected for 'a'. LED 0 is then illuminated, signalling that 'a' is less than 'b'.



B								A										
S15	S14	S13	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1	S0			
0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	LED 0	LED 1	LED 2
49								128										

Test Results	Value of A	128
	Value of B	49
		A Greater than B

Very good set of results

Figure 37 - Element 1 - 8-Bit Functional Testing AGTB

For the 'greater than' test, illustrated in the image above, the values of inputs 'a' and 'b' are set with different binary values, by selecting the toggle switches on the Nexys 4DDR board. For the test, the binary code for the digital value of 49 was selected for 'b', whist the binary code for the digital value of 128, was selected for 'a'. LED 2 is then illuminated, signalling that 'a' is greater than 'b'.

In conclusion, from the simulated and functional testing conducted, the 8-bit adder is functioning as required

1.6 Evaluation

Using the Vivado digital hierarchy, an 8-bit magnitude comparator was designed and successfully simulated. Successful function of the 4-bit magnitude comparator was only possible following successful completion of the prior design stages, resulting in the hierarchy being able to inherit proven designs to build the 4-bit magnitude comparator.

Firstly, the half adder was designed. This was designed as a sole element using VHDL language and successfully simulated in Vivado. Using the half adder, a full adder was then created by combining two half adders into one, whilst still retaining its own architecture. On completion of the full adder, the design was completed using VHDL language and successfully simulated in Vivado.

By combining four full adders to create one entity, the 4-bit adder was then created. Once designed, it was successfully simulated in Vivado using bitstream generation to prove the test outcomes. On successful simulation tests, the program was then downloaded to a Nexys 4DDR board for functional testing. The functional testing proved to be successful by operation of the toggle switches to create the required test outcomes.

The 8-bit adder was then created which consisted of two 4-bit adders combined as one. The 8-bit magnitude comparator was built using Multisim in PLD mode, and downloaded to the Nexys 4DDR board for functional testing. The functional testing proved to be successful by operation of the toggle switches to create the required test outcomes.

Each design stage was proven to be successful, by simulation and functional testing, resulting in a functional 8-bit magnitude comparator.

Very good evaluation of the element

2. Element 2

2.1 Introduction

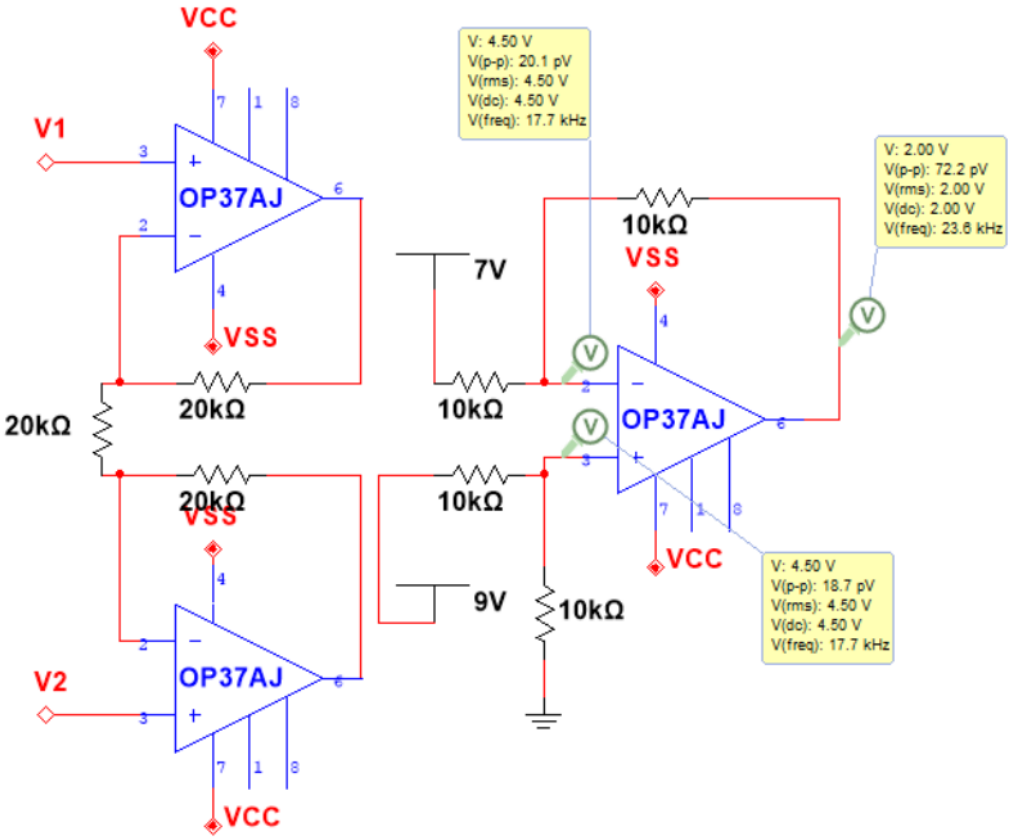
Element 2 builds on that seen with element 1, stages taken from the 8-bit magnitude comparator to develop a system for the final design. In this way, components used for the final design and implementation, such as the analogue to digital convertor with amplifier and magnitude comparator, had already been tried and tested, and successful configuration and operation established. All of the required components were designed, built, and simulated individually, and as a complete system, using Multisim and LabView. Further testing of the complete system required the design to be downloaded to Nexys4 DDR and Elvis II development boards.

Good introduction

2.2 Design requirements

2.2.1. Load Cells & Signal Conditioning

Illustrated in the image below is the unity gain amplifier, an amplifier that as a result of the feedback resistors has a gain value of one. The amplifier below does not have a connection to the buffer amplifiers and is behaving as a differential amplifier. The amplifier is loaded with two voltages, one at 7v the other at 9v, resulting in the positive and negative inputs having the differential voltage.



Good example which indicates a good understanding of op amps

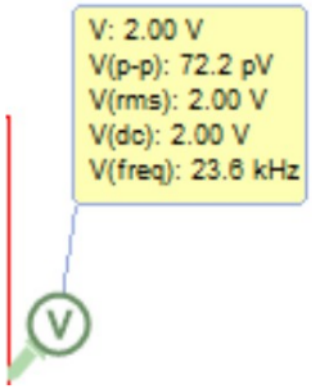
Figure 38 - Element 2 - Unity Gain Amplifier

From the resistors, the gain can be calculated:

$$Gain = \frac{Rf}{Rin} = \frac{10K}{10K} = 1$$

Equation 1 - Element 2 - Unity Gain

Shown in the image below is the voltmeter output of the differential amplifier, proving the function of the differential amplifier with a 2v output. For amplification to occur, the ratio of the resistors would have to be changed to a suitable value.



Good result and explanation

Figure 39 - Element 2 - Unity Gain Amplifier Output

Illustrated in the image below is the instrument amplifier, normally employed to magnify exceedingly small inputs from components, for example sensors. Instrument amplifiers differ from other amplifiers in that they incorporate a feedback resistor that is able to be adjusted to alter the closed-loop gain. The first amplifiers are employed as buffer amplifiers, providing gain.

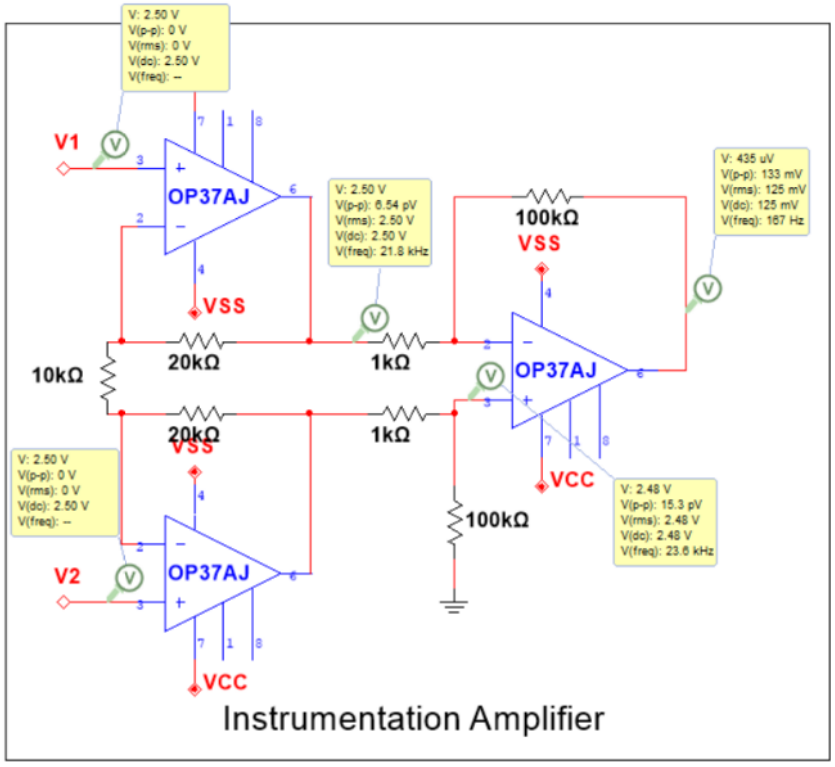


Figure 40 - Element 2 - Instrument Amplifier

From the selected values of the instrument amplifier above, the following can be calculated:

$$Buffer\ Gain = 1 + \frac{(2\ x\ R2)}{R1} = 1 + \frac{(2\ x\ 20)}{10} = 5$$

Good work

Equation 2 - Element 2 - Buffer Gain

$$Differantial\ Amplifier\ Gain = \frac{100\ x10^3}{1\ x10^3} = 100$$

Equation 3 - Element 2 - Differential Amplifier Gain

$$Amplifier\ Gain = 100\ x\ 5 = 500$$

Equation 4 - Element 2 - Amplifier Gain

The required gain is achieved and explained

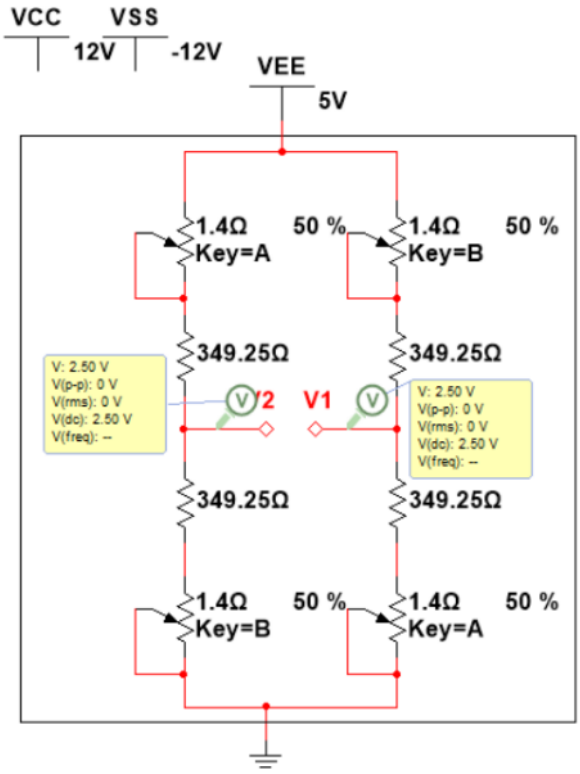


Figure 41 - Element 2 - Load Cell

Illustrated in the image above is a representation of a load cell circuit with an excitation of 1-5v, determined by varying resistance as a result of pressure applied, producing a 2mV/V output. A maximum load of 1000grams applied to the load cell will produce a 5v output with a differential of 10mV.

The gain of the load cell can be calculated as follows.

$$Gain = \frac{5}{10\ x10^{-3}} = 500$$

Equation 5 - Element 2 - Load Cell Gain

The calculated load cell gain relates to the total gain of the amplifier. Both the instrument amplifier circuit and the load cell circuit were combined for testing. Simulation of the load cell output was achieved by incorporating a bridge of variable resistors which were paired in a diagonal fashion on the circuit and adjusted to simulate the load cells output. Initial values of 50%-50%, resulting in zero output, no load, were adjusted to increase the difference between the pairs to 100%-0%, resulting in maximum output.

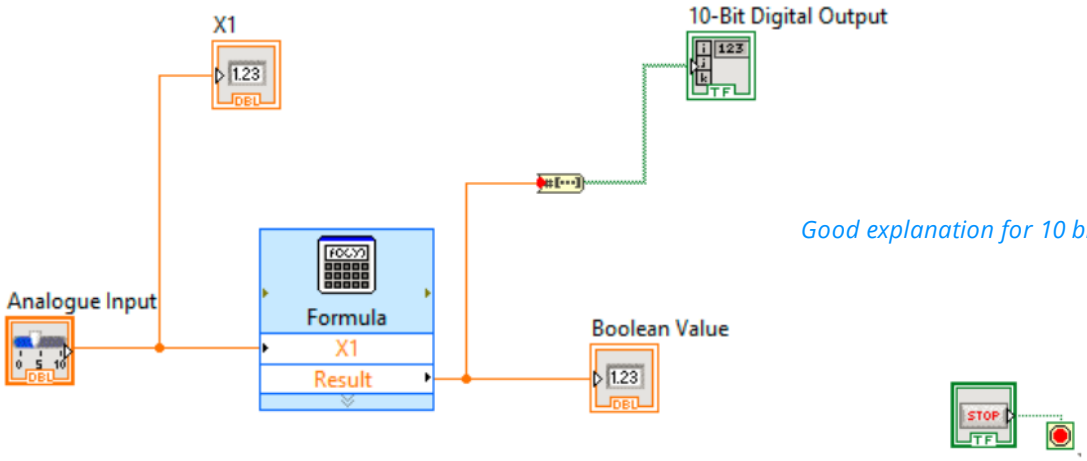
Good explanation

2.2.2. *10 & 12 Bit Analogue to Digital Convertors*

Both 10-bit and 12-bit analogue to digital convertors (ADC) are designed using LabView software. Illustrated in the image below is the design which is used to calculate the boolean value. By providing an analogue input for the formula block, the boolean value is generated, along with the 10-bit digital output from the function block. The formula shown below is inputted to the formula block.

$$\left(\frac{x1}{5}\right) x\, 2^{10} = \left(\frac{x1}{5}\right) x\, 1024$$

Equation 6 - Element 2 - 10-Bit Formula Block



Good explanation for 10 bit ADC

Figure 42 - Element 2 - LabView 10-bit ADC Design

Within LabView, a front screen for the inputs and outputs were created, as shown in the image below. The analogue input can be varied using the analogue input slider. The resolution of the 10-bit ADC has 1024 possible outputs, the first being zero which results in the maximum boolean value of 1023.

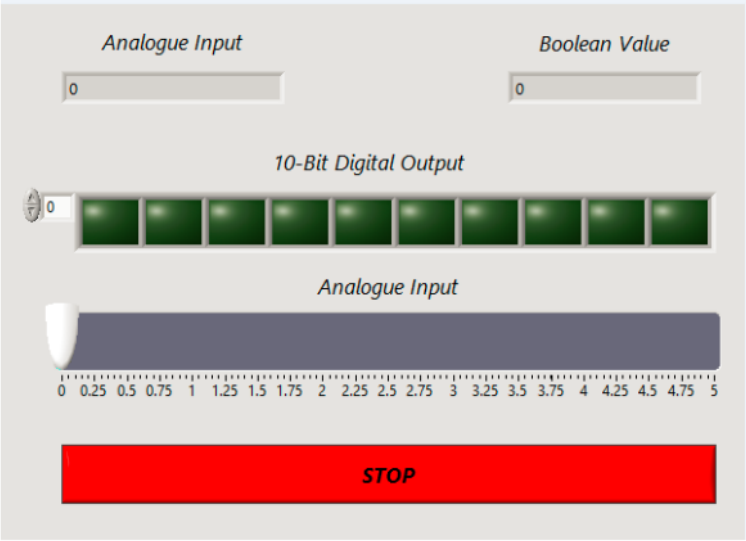


Figure 43 - Element 2 - 10-Bit ADC

Good example of front pane view for 10 bit ADC

With the design of the 10-bit ADC completed and successfully tested, alterations were made to the design, changing to a 12-bit ADC. The formula shown below is inputted to the formula block.

$$\left(\frac{x1}{5}\right) x\ 2^{12} = \left(\frac{x1}{5}\right) x\ 4096$$

Equation 7 - Element 2 - 12-Bit Formula Block

Good explanation of 12 bit ADC

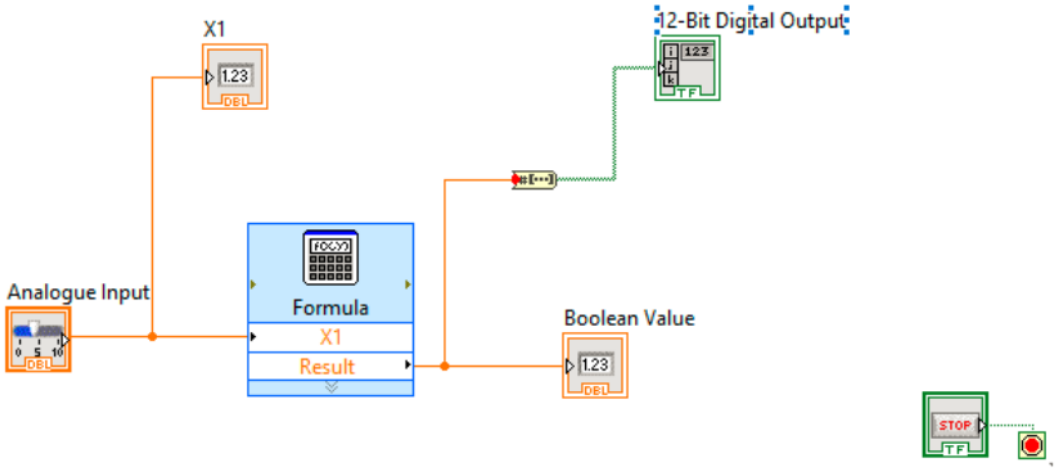
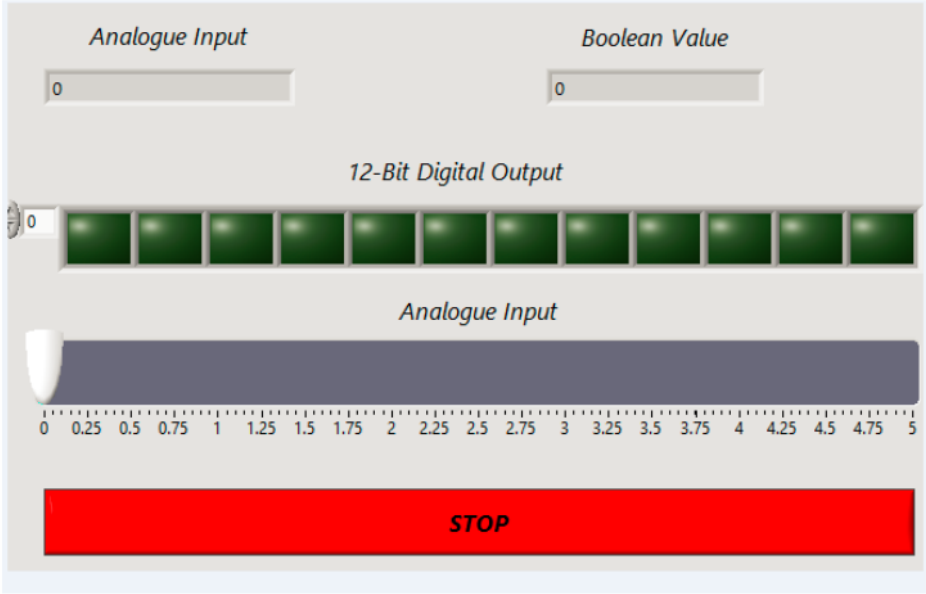


Figure 44 - Element 2 - LabView 12-bit ADC Design

Alterations were made to the front screen, adding two additional digital outputs as shown below. The resolution of the 12-bit ADC has 4096 possible outputs, the first being zero which results in the maximum boolean value of 4095.



Good front panel example of 12 bit ADC

Figure 45 - Element 2 - 12-Bit ADC

2.3 Implementation

2.3.1. *8-Bit Analogue to Digital Convertor*

With the design and testing of the 10 and 12-Bit ADC's proving successful functionality, a new 8-bit ADC circuit was constructed using the same design requirements within LabView. Additional components such as digital inputs, DAQmx create, DAQmx read, 500ms counter and task clear were added to the circuit, allowing the 8-Bit ADC to be downloaded to the Elvis II development board for implementation and testing.

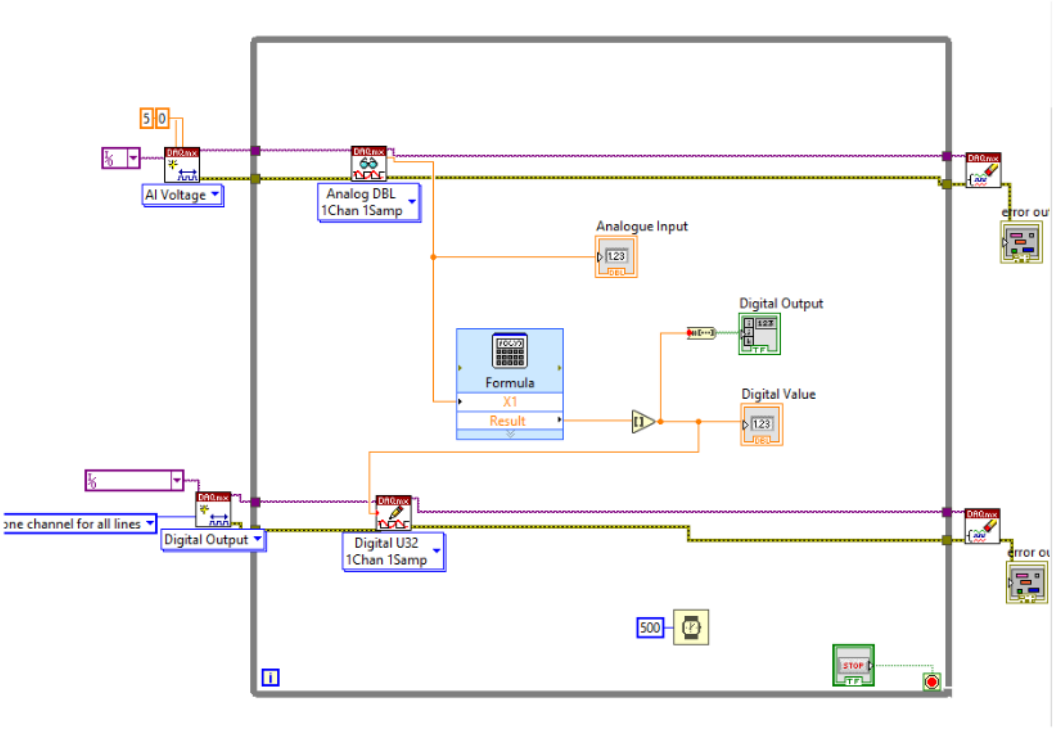


Figure 46 - Element 2 - 8-Bit ADC Design

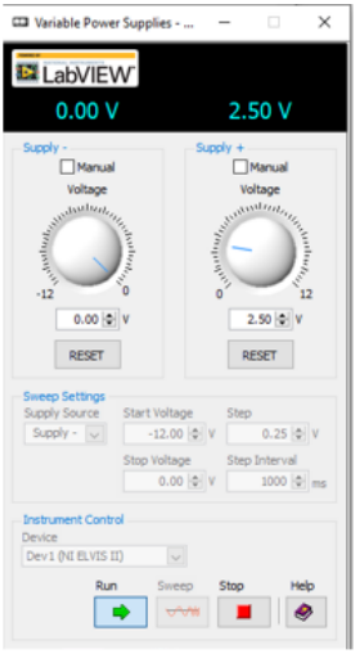
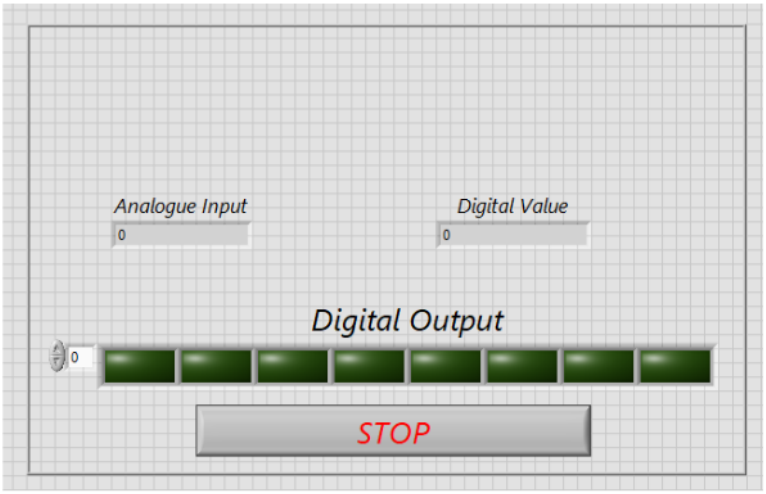


Figure 47 - Element 2 - LabView Dual Variable Power Supply

Within LabView a new front screen for the outputs, shown in the image below, was created. No inputs are added to the front screen for the 8-Bit ADC as the input was controlled via a dual variable power supply within the Elvis II software. The analogue input remains able to be varied, but from a dial on the dual variable power supply, as shown in the image above. The resolution of the 8-bit ADC has 256 possible outputs, the first being zero being the first which results in the maximum boolean value of 255.



Good design of 8 bit ADC

Figure 48 - Element 2 - 8-Bit ADC Front Page

2.3.2. *Magnitude Comparator*

Following successful implementation and testing of the 8-bit ADC, a FPGA magnitude comparator program was designed using LabView, as illustrated in the image below. The circuit consists of three parts:

- The top part contains formula block 1 and 2, with an analogue input form the load sensor/potentiometer. The formula blocks are configured to scale with 8-bit resolution and to 1000 grams, converting the input from analogue to digital.
- The middle part of the circuit, containing formula block 3 and 4, is designed for 16-bit word output to FPGA magnitude comparator. The formula blocks are configured to scale input signal to grams, 0 to 1000.
- The final lower formula block is configured to create the required 16-bit for the FPGA. The bottom part of the circuit is designed for the digital input result from the FPGA magnitude comparator.

The block achieves this by multiplying the 8 bit value by 256. The lower 8 spaces are then used to add the set point value

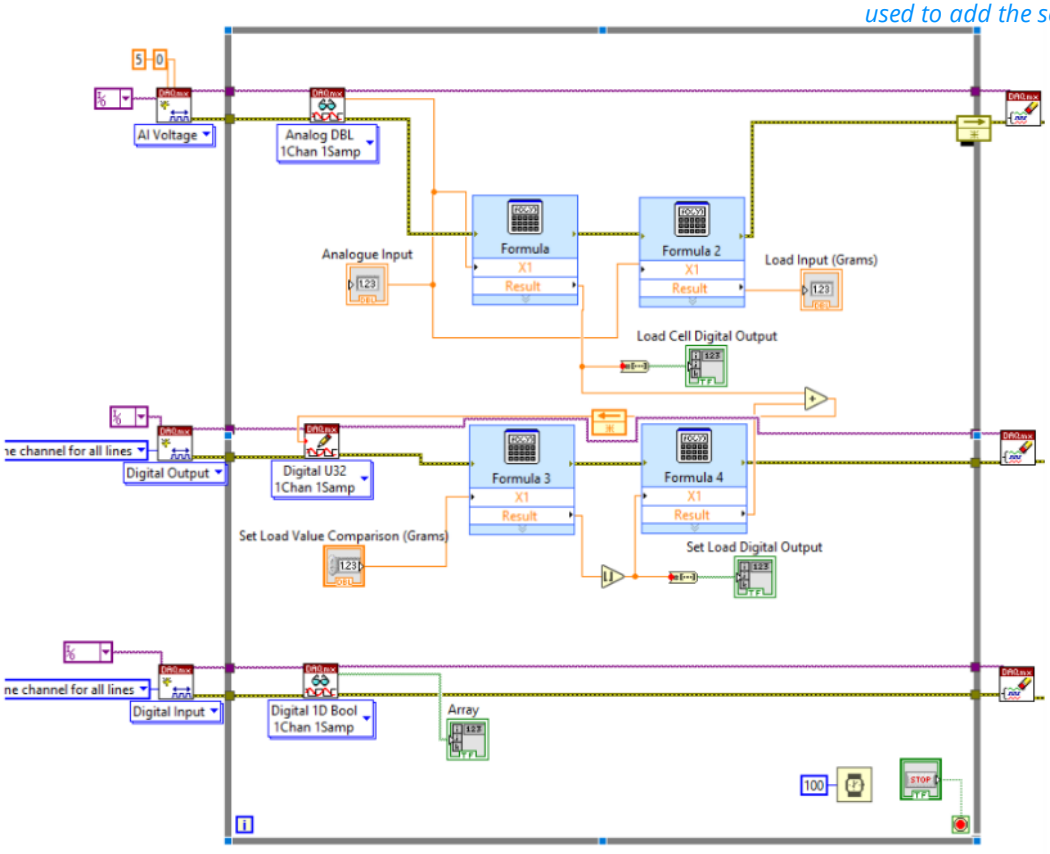
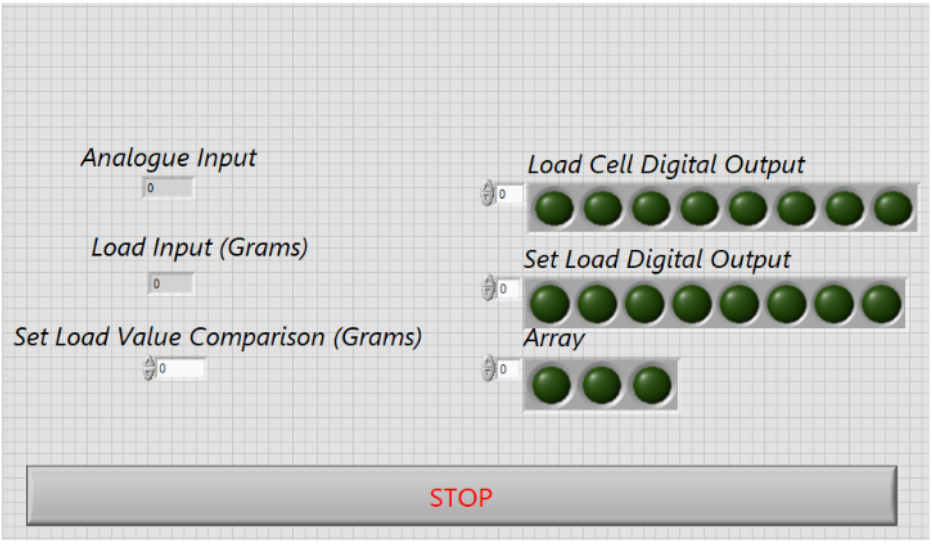


Figure 49 - Element 2 - FPGA Magnitude Comparator

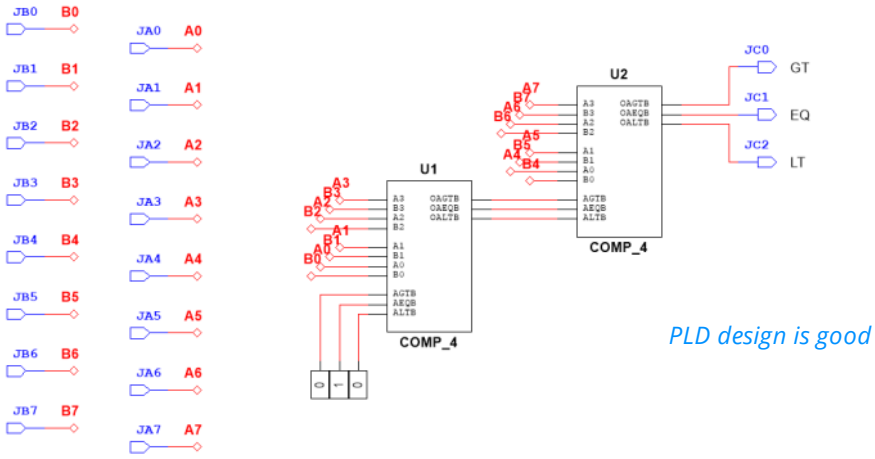


Front panel view is good

Figure 50 - Element 2 - Magnitude Comparator LabView Front Page

Within LabView a new front screen for the outputs as shown in the image above, was created. On the left hand side are the analogue input, representative of the input voltage from the load sensor/potentiometer, and the load input representative of the analogue input in terms of mass. The right hand side of the screen displays the load cell digital output, representative of the converted digital value of analogue input, the set load digital output representative of the digital value of the set load value, and the array which will indicate one of three values, less than, equal to or greater than, representing the difference/comparison between the set load value and the load input value.

Good explanation



PLD design is good

Figure 51 - Element 2 - Multisim PLD

Combining the designed LabView magnitude comparator circuit with the PLD circuit designed in element 1, as shown below, creates a fully functional system. Both the Nexys DDR4 and the Elvis II boards are also required for the operational circuit, with Pmod ports located along the left-hand side of the PLD board, as shown below, used to communicate between the PLD and the Elvis II boards.

11 Pmod Ports

The Pmod ports are arranged in a 2×6 right-angle, and are 100-mil female connectors that mate with standard 2×6 pin headers. Each 12-pin Pmod port provides two 3.3V VCC signals (pins 6 and 12), two Ground signals (pins 5 and 11), and eight logic signals, as shown in Figure 20. The VCC and Ground pins can deliver up to 1A of current. Pmod data signals are not matched pairs, and they are routed using best-available tracks without impedance control or delay matching. Pin assignments for the Pmod I/O connected to the FPGA are shown in Table 5.

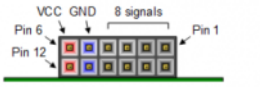


Figure 20. PMOD connectors; front view, as loaded on PCB.

Table 5. Nexys4 DDR Pmod pin assignments.

Pmod JA	Pmod JB	Pmod JC	Pmod JD	Pmod XDAC
JA1: C17	JB1: D14	JC1: K1	JD1: H4	JXADC1: A13 (AD3P)
JA2: D18	JB2: F16	JC2: F6	JD2: H1	JXADC2: A15 (AD10P)
JA3: E18	JB3: G16	JC3: J2	JD3: G1	JXADC3: B16 (AD2P)
JA4: G17	JB4: H14	JC4: G6	JD4: G3	JXADC4: B18 (AD11P)
JA7: D17	JB7: E16	JC7: E7	JD7: H2	JXADC7: A14 (AD3N)
JA8: E17	JB8: F13	JC8: J3	JD8: G4	JXADC8: A16 (AD10N)
JA9: F18	JB9: G13	JC9: J4	JD9: G2	JXADC9: B17 (AD2N)
JA10: G18	JB10: H16	JC10: E6	JD10: F3	JXADC10: A18 (AD11N)

FPGA ports are identified here

Digilent produces a large collection of Pmod accessory boards that can attach to the Pmod expansion connectors to add ready-made functions like A/D's, D/A's, motor drivers, sensors, as well as other functions. See www.digilentinc.com for more information.

Figure 52 - Element 2 - PMOD Ports

2.4 *Testing and Analysis*

2.4.1. *Load Cells and Signal Conditioning*

Illustrated in the image below, the variable resistors of the load cell circuit are all set to 50%, resulting in 0v output. The output shown on the voltmeter is 435µV. True zero is not possible as there will always be an offset.

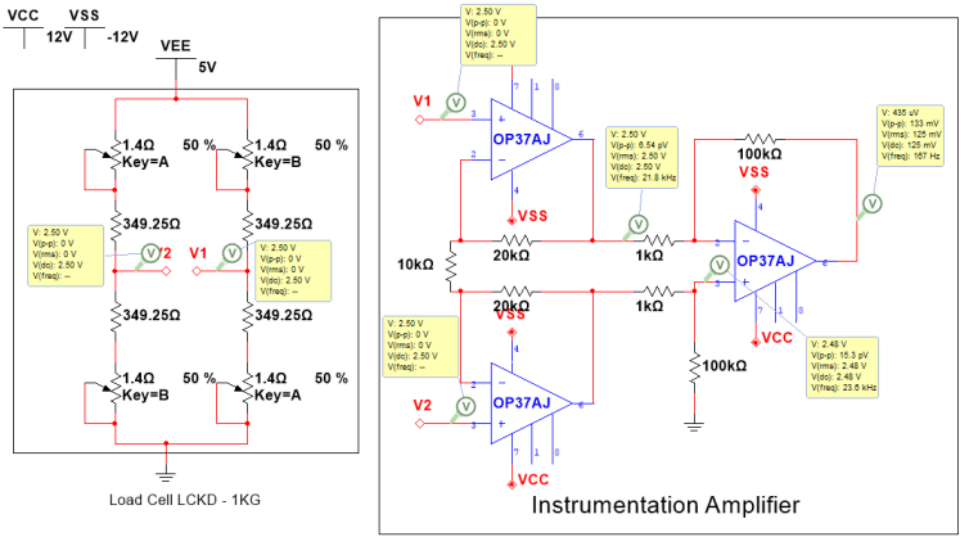


Figure 53 - Element 2 - Load Cell 50% Load Test

When the variable resistors are set to 75% and 25%, the expected voltage output should be 50% of the output range. Shown in the image below, the output voltage can be seen as 2.5v, exactly 50% of the load cell output range (0-5v).

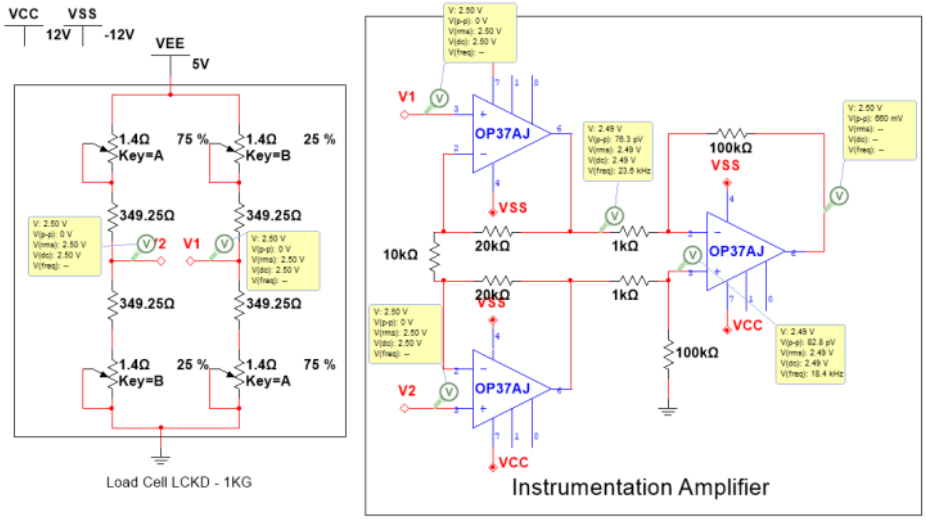


Figure 54 - Element 2 - Load Cell 75% Load Test

When the variable resistors are set to 100% and 0%, the expected voltage output should be 100% of the output range. Shown in the image below, the output voltage can be seen as 5v, exactly 100% of the load cell output range.

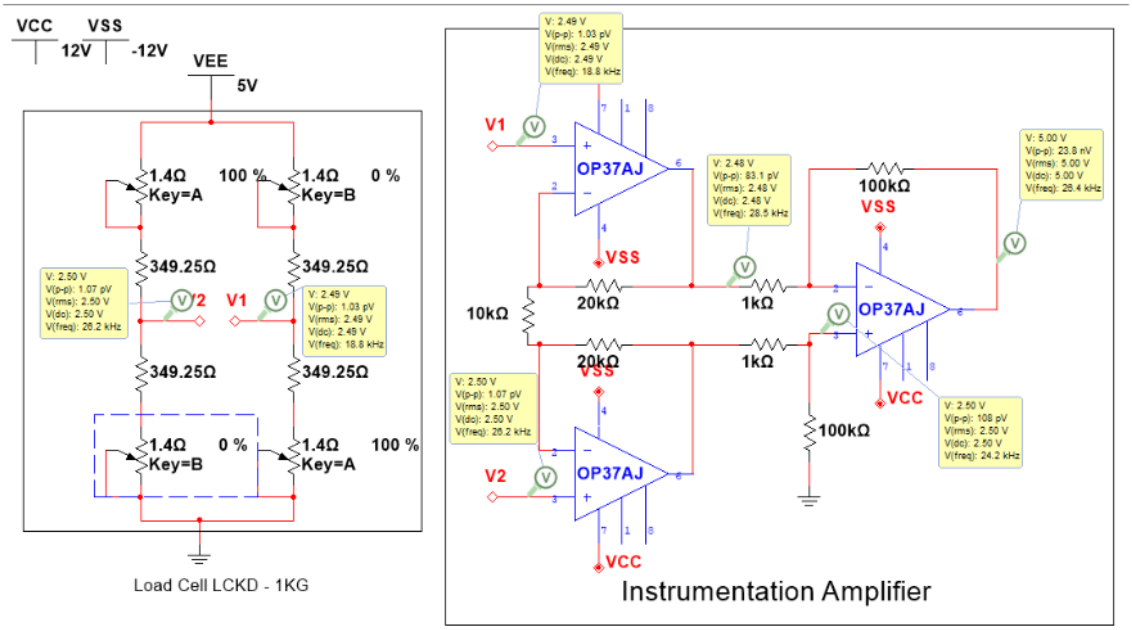


Figure 55 - Element 2 - Load Cell 100% Load Test

% Resistance	Grams	Voltage
50	0	435µV
55	100	500mV
60	200	1v
65	300	1.5v
70	400	2v
75	500	2.5v
80	600	3v
85	700	3.5v
90	800	4v
95	900	4.5v
100	1000	5v

Good table of results

Table 3 - Element 2 - Load Cell Testing

Demonstrated in the table above are all of the load test results (see appendix 6.1 for further testing result images). Data gathered from the table of results are inputted onto a graph comparing output voltage with load (mass). A positive linear

(proportional) response is seen i.e. as the load increases, a proportional increase in the output value is seen, as illustrated in the image below.

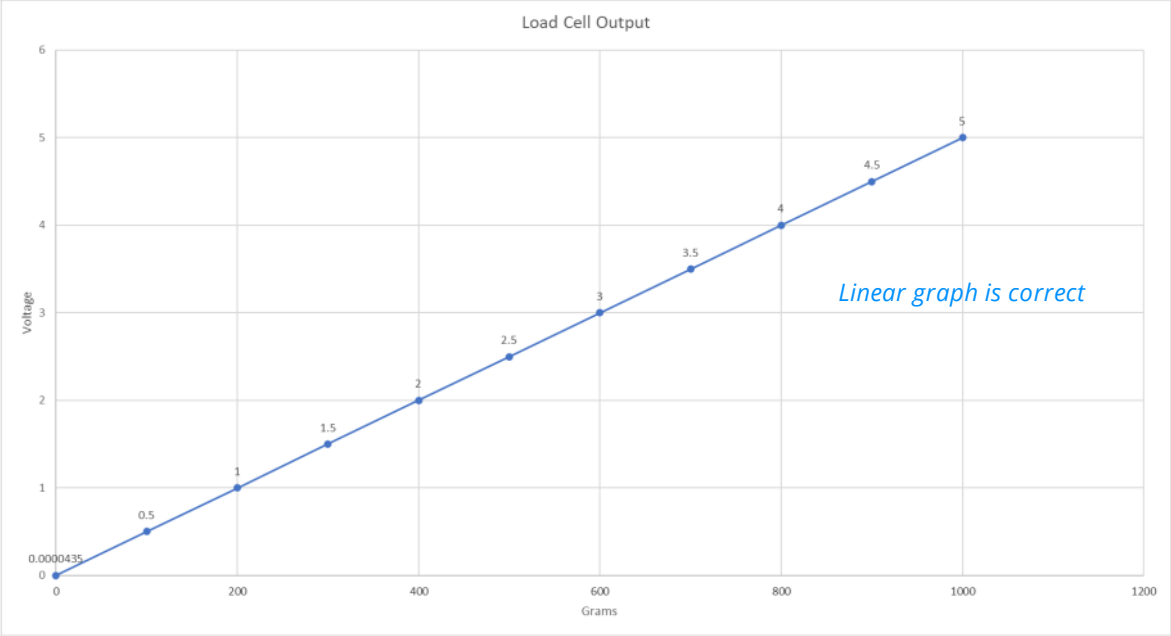


Figure 56 - Element 2 - Load Cell Output

2.4.2. *10 & 12 Analogue to Digital Convertors*

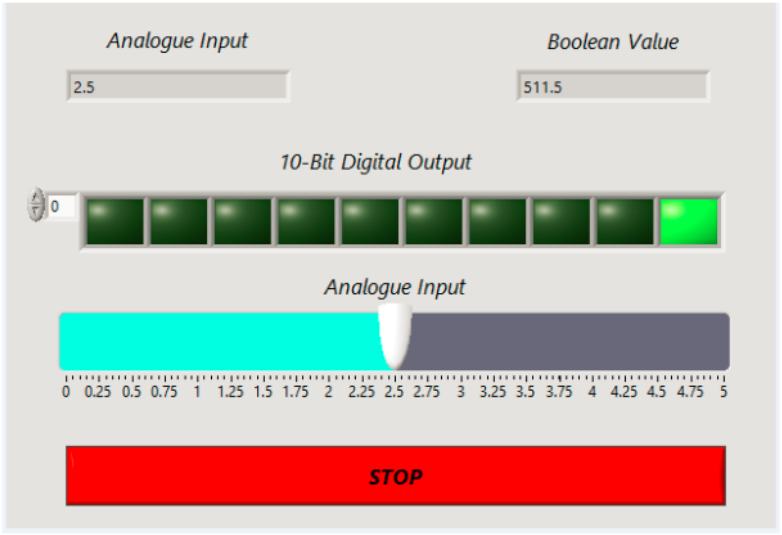


Figure 57 - Element 2 - 10-Bit ADC Test

Illustrated in the image above is the 10-bit ADC front page displayed during testing. With the analogue input selector set to 2.5, the analogue input corresponds to the equivalent boolean value, which is also proven by the illuminated LED's on the 10-bit digital output. Illustrated in the image below, when the analogue input selector is set to 5, again the analogue input corresponds to the equivalent boolean value, and proven by the illuminated LED's on the 10-bit digital output.

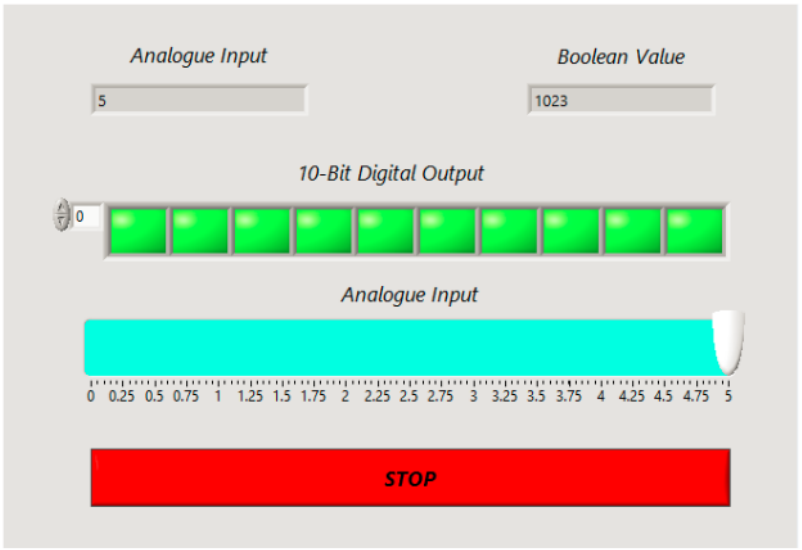


Figure 58 - Element 2 - Element 2 -10-Bit ADC Test

10 bit ADC tests are good

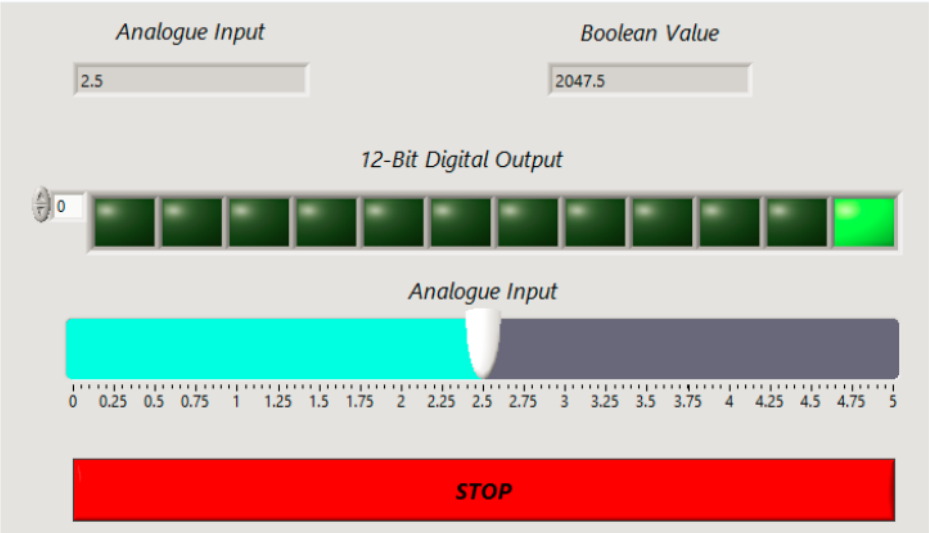


Figure 59 - Element 2 - 12-Bit ADC Test

Illustrated in the image above is the 12-bit ADC front page displayed during testing. With the analogue selector set to 2.5, the analogue input corresponds to the equivalent boolean value, which is also proven by the illuminated LED's on the 10-bit digital output. Illustrated in the image below, when the analogue selector is set to 5, the analogue input again corresponds to the equivalent boolean value, and proven by the illuminated LED's on the 12-bit digital output.

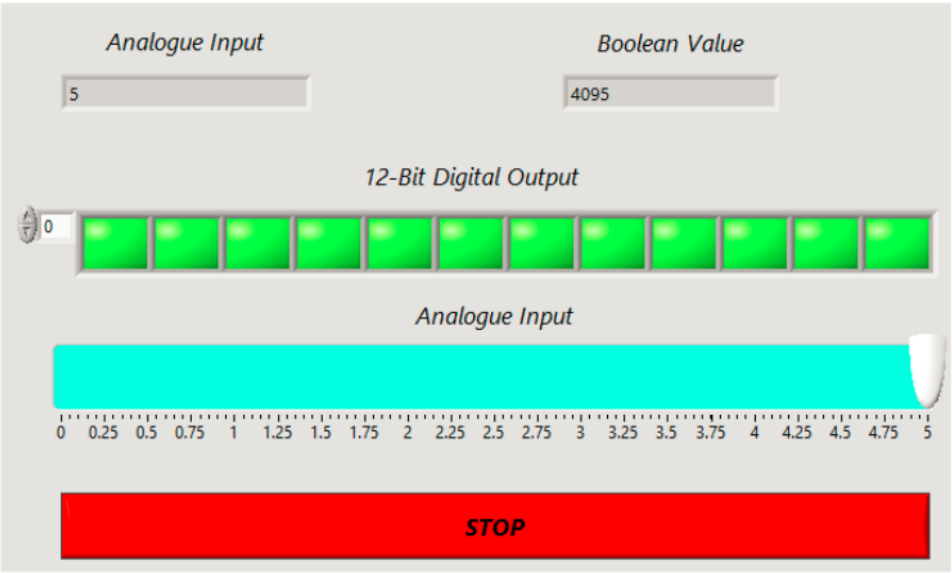
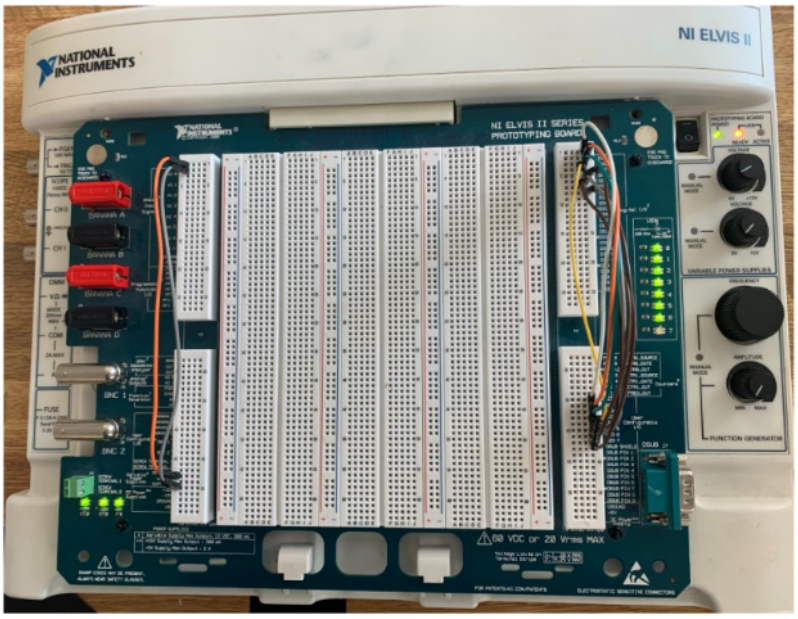


Figure 60 - Element 2 - 12-Bit ADC Test

12 bit ADC tests are good

2.4.3. *8-Bit Analogue to Digital Convertor*



DAQ board output result is good

Figure 61 - Element 2 - National Instruments Elvis II Board - Test

Illustrated in the image above is the Elvis II board used during testing. Shown in the image below, the variable power supply was set to 2.5v, the analogue input value corresponding to the equivalent boolean value. As well as the numerical values corresponding to each other, the visual LED indication on both front page of LabView and the Elvis II board illuminate to the correct output, confirming successful implementation and testing.

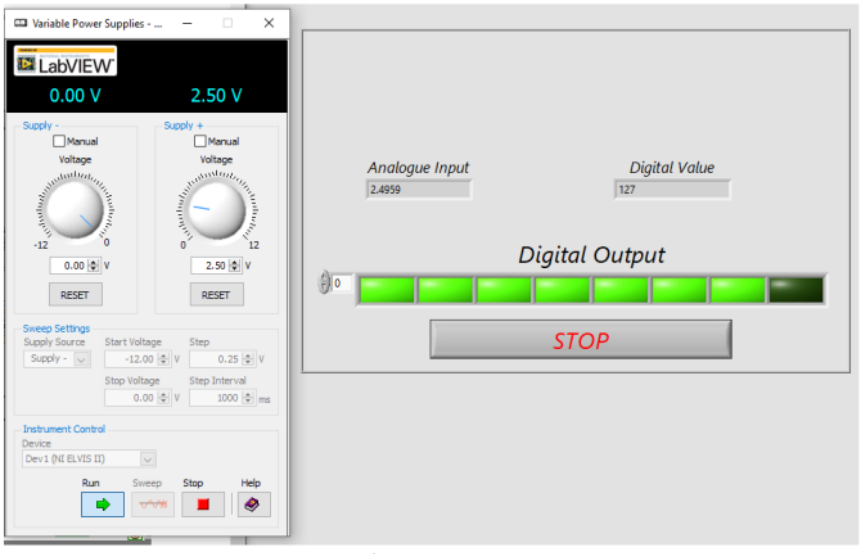


Figure 62 - Element 2 - 8-Bit ADC Test

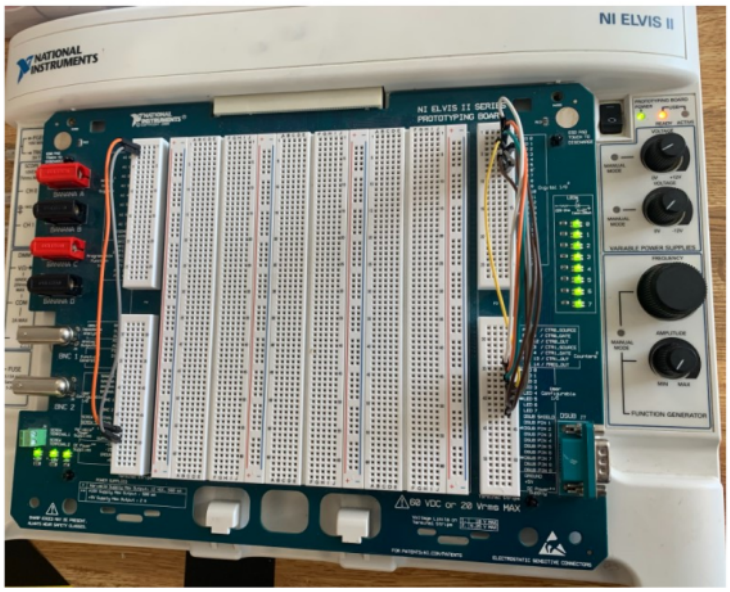


Figure 63 - Element 2 - National Instruments Elvis II Board - Test

Illustrated in the image above is the Elvis II board used during testing. Shown in the image below, the variable power supply was set to 5v, the analogue input value corresponding to equivalent boolean value. As well as the numerical values corresponding to each other, the visual LED indication on both front page of LabView and the Elvis II board illumine to the correct output, confirming successful implementation and testing.

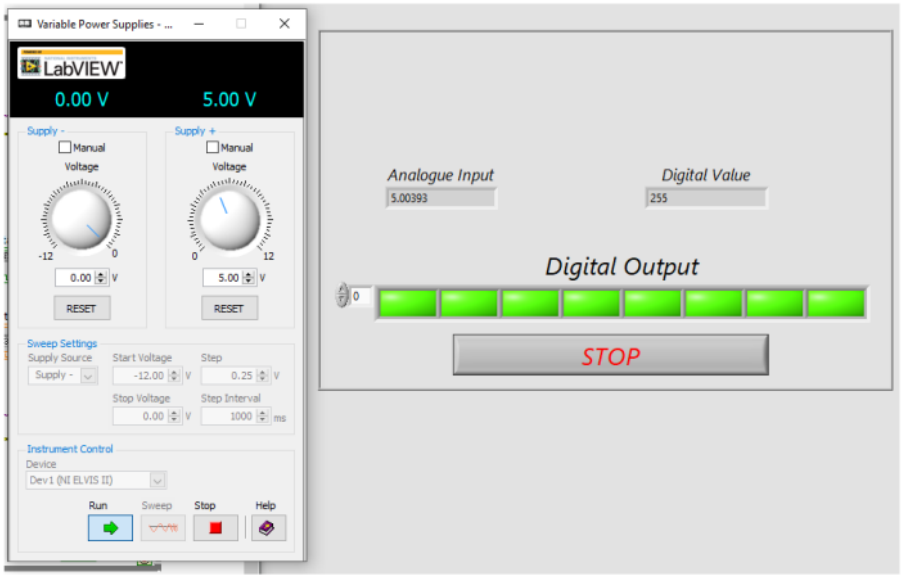
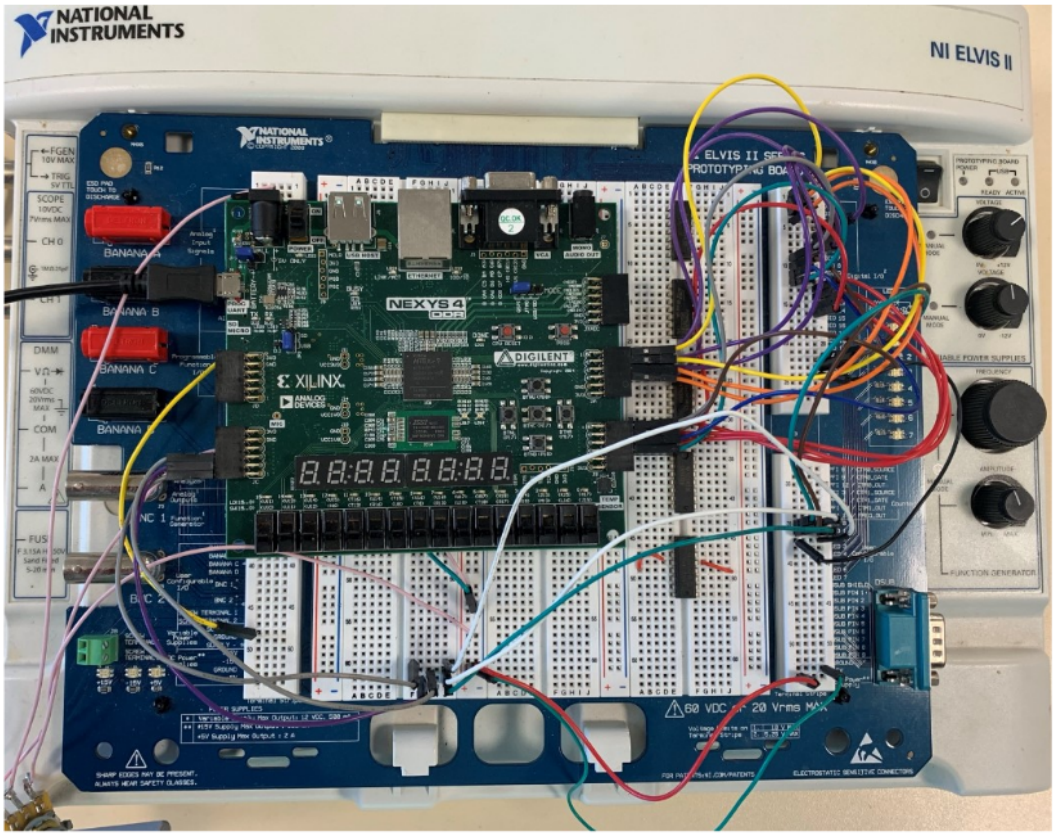


Figure 64 - Element 2 - 8-Bit ADC Test

Good results

2.4.4. *Magnitude Comparator*



Good clear image of equipment setup

Figure 65 - Element 2 - FPGA & Nexys Boards

With the FPGA and Nexys boards combined, the designed magnitude comparator was able to be tested. In order to test the correct functionality of the circuits, three tests were conducted to verify each of the three possible outputs of less than, equal to or greater than.

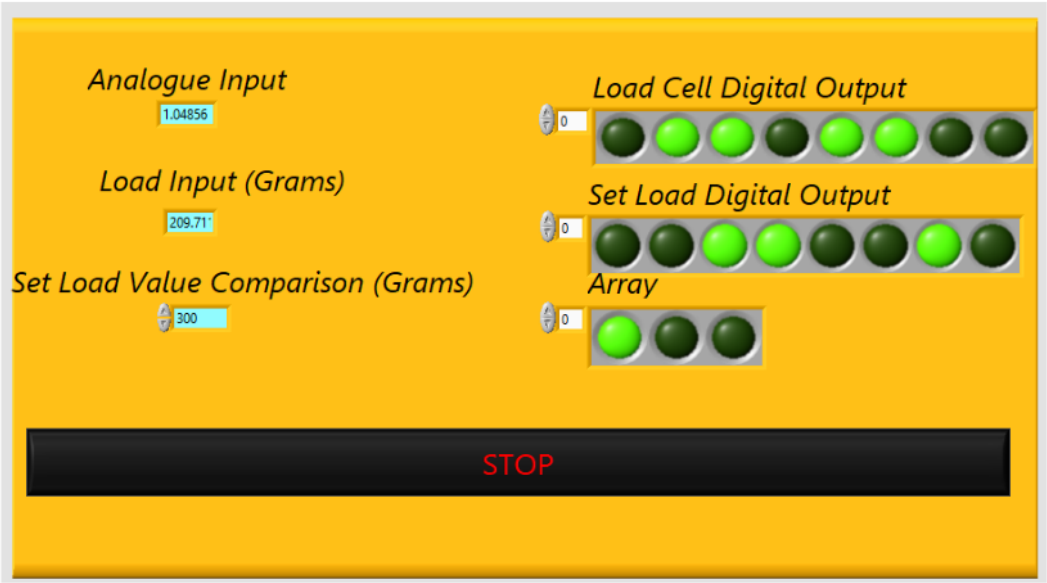


Figure 66 - Element 2 - LabView - Less Than

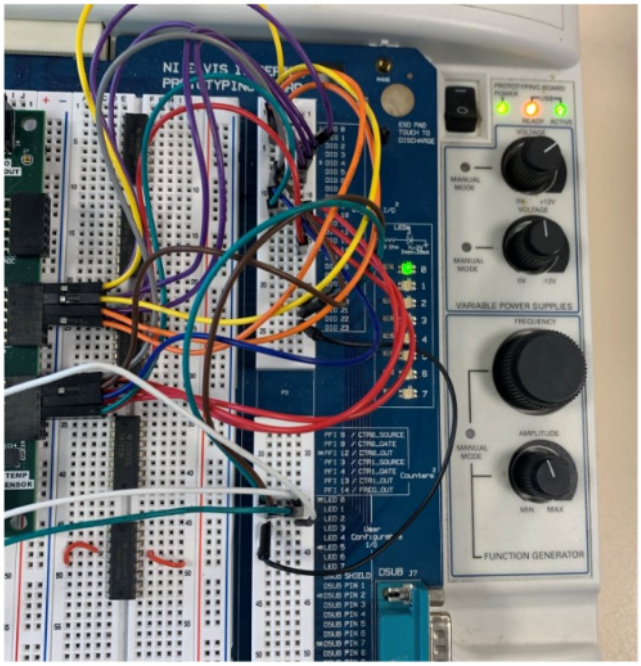


Figure 67 - Element 2 - FPGA - Less Than

Illustrated in the images above, a set load value of 300 grams was selected and an input load value of 209.71 grams simulated. As demonstrated on both circuits, the "Less Than" LED is illuminated, proving the "Less Than", functionality operates correctly as designed.

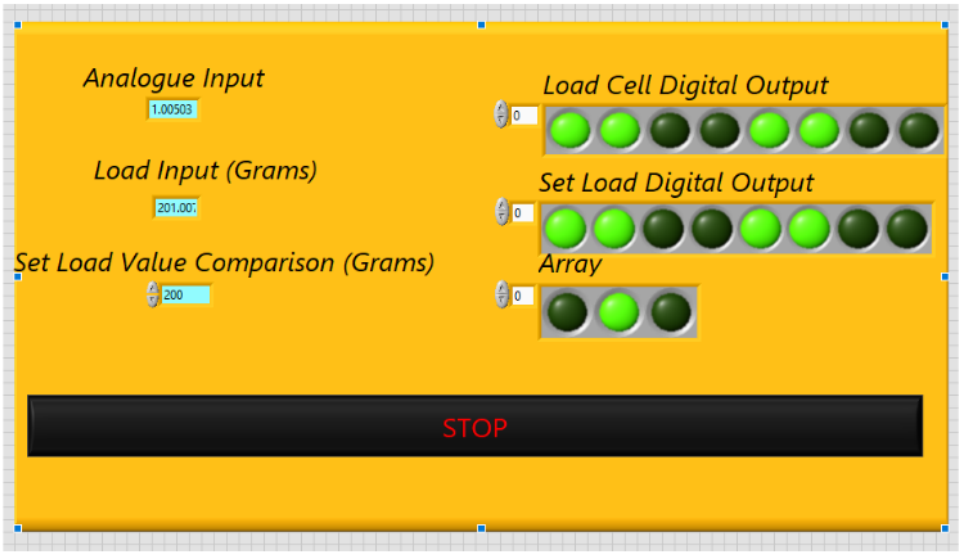


Figure 68 - Element 2 - LabView - Equal to

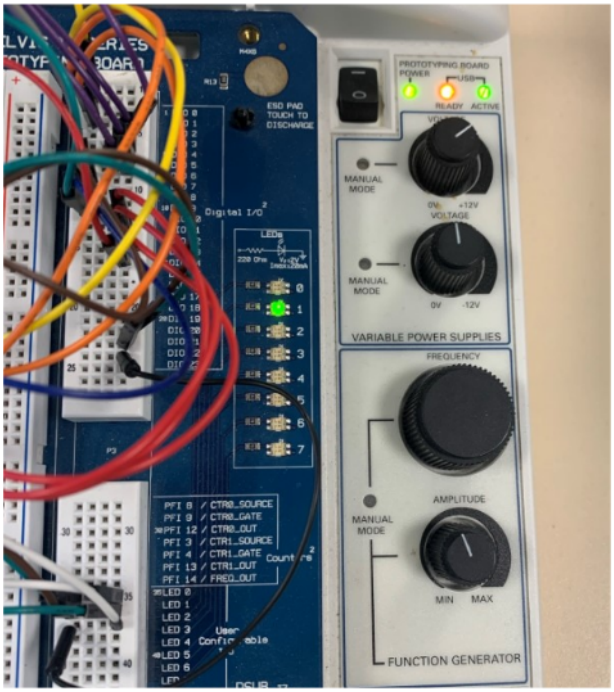


Figure 69 - Element 2 - FPGA - Equal to

Illustrated in the images above, the set load value was changed to 200 grams and an input load value of 201.00 grams simulated. As demonstrated on both circuits, the "Equal to" LED is illuminated, proving the "Equal to", functionality operates correctly as designed.

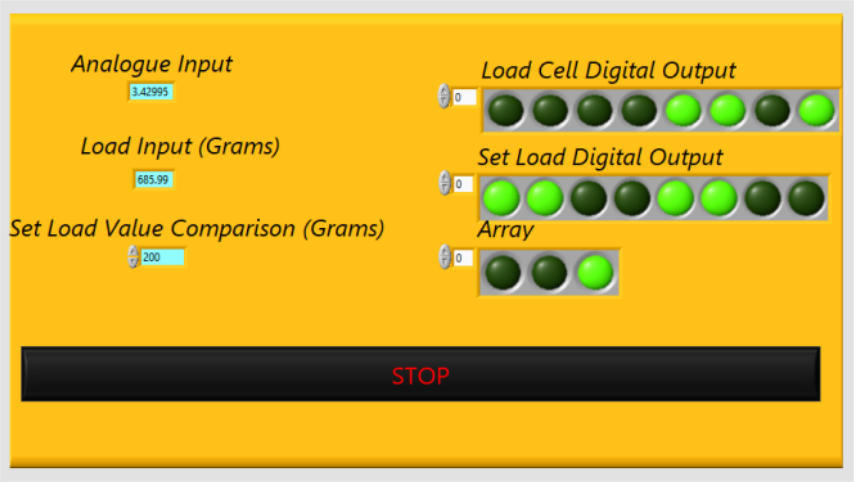


Figure 70 - Element 2 - LabView - Greater Than



Figure 71 - Element 2 - FPGA - Greater Than

Illustrated in the images above, keeping the set load value at 200 grams, an input load value of 685.99 grams is simulated. As demonstrated on both circuits, the "Greater Than" LED is illuminated, proving the "Greater Than", functionality operates correctly as designed.

Very good set of results

2.5 Evaluation

The requirement of element 2 was the design and testing of individual circuit prototypes, namely instrument amplifier, analogue to digital convertor and digital magnitude comparator, prior to proceeding to finished designs.

Multisim software was used to design and test the instrument amplifier, representation of load achieved by combining it with a bridge circuit. Altering bridge circuit resistor values, thus representing various loads, caused the amplifier output to change to represent altering load values. As resistance values increased, the voltage output of the amplifier also increased in a liner scale. Results of the test were proven to be successful, as each of the load and amplified results displayed exact values with no error shown.

An analogue to digital convertor was designed using LabView. Three circuits, an 8-bit ADC circuit with a virtual input, 10-bit circuit and 12-bit circuit with software inputs, were designed and simulated. Testing for the 10-bit and 12-bit circuits required the use of a slider on the LabView home page, adjusting the analogue input which would then display the correct digital output and boolean value, with no errors identified. Testing of the 8-bit required a virtual variable input from the LabView software, with the designed circuit also connected to the Elvis II board. Altering the variable power supply to a set value would result in the 8-bit circuit displaying the corresponding analogue and digital values as well as the boolean value. The digital values displayed by LEDs demonstrated successfully correspondence between the LabView programme and the Elvis II board. Negligible error was displayed for the analogue input values.

A digital magnitude comparator was then designed using LabView. Combining the designed circuit with the PLD circuit designed in element 1, the circuits were then uploaded to the Elvis II board that had been configured with a Nexys DDR4 board. Selecting a set point value for the load value, a load sensor/potentiometer was then used to simulate three possible test outcomes for the set point, “Less than”, “Equal to” and “Greater Than”. The digital values displayed by LEDs showed successful correspondence between the LabView programme and the Elvis II board. Negligible error was displayed for the analogue input and load input value for the “Equal to” test.

When used individually or as a combined system, the analogue to digital convertors utilised formula blocks to enable conversion of the signal from analogue to digital dependant on resolution. These required a scaled input signal as a fraction of the maximum input, that was then divided by the required resolution. From this a boolean value was obtained, allowing a change of state, through comparison, of the digital outputs. Each design stage was proven to be successful by simulation and functional testing, allowing advancement to the final design.

Evaluation i good

3. Element 3

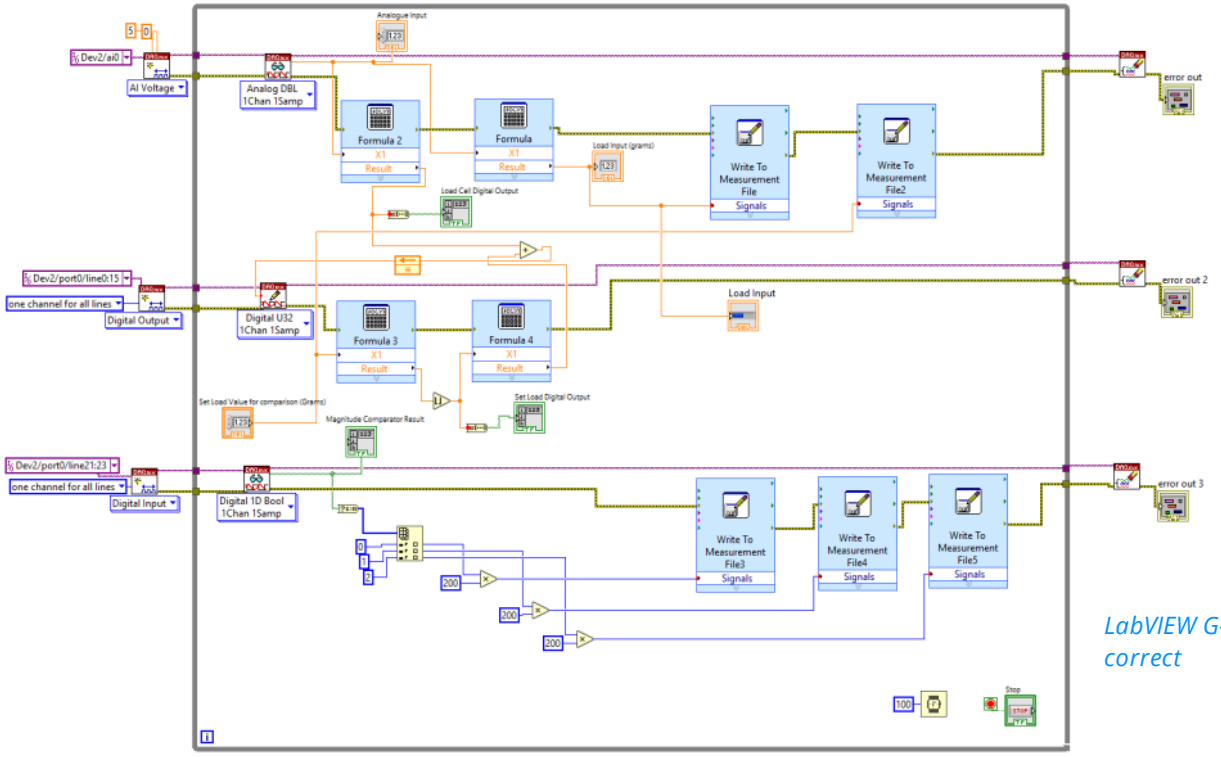
3.1 Introduction

Element 3 builds on that seen with element 2, with additions made to the developed magnitude comparator to incorporate methods of data logging. The magnitude comparator was tested under three different set points, simulating a load placed on a load cell, with the data recorded for each test identifying whether the analogue input is less than, greater than or equal to, that of the simulated load and set point values.

Good introduction

3.2 Design requirements

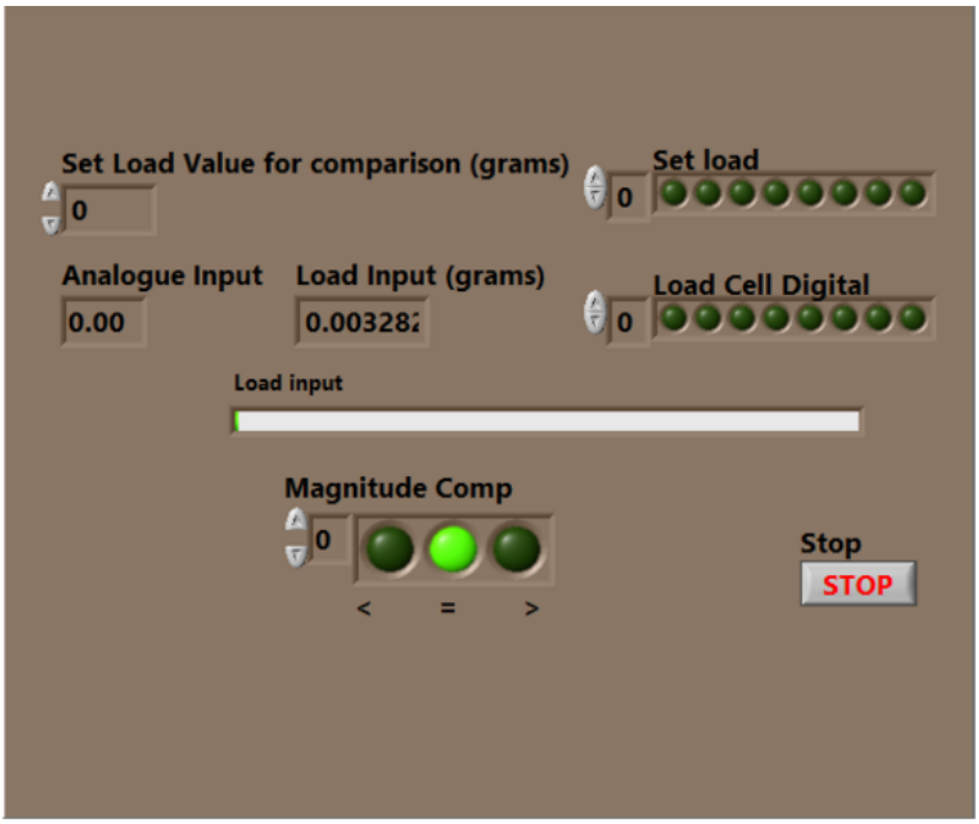
Illustrated in the image below, the amended FPGA magnitude comparator circuit with the addition of five 'write to measure' functions, that are used for data logging. The addition of these blocks will allow the LabView software to record and save the data produced.



LabVIEW G-code is correct

Figure 72 - Element 3 - FPGA Magnitude Comparator with Data Logging

'Write to measure' file one is used to record the analogue input and time, with the recording spanning the duration of the test analysis period. The time is recorded by using the one column only option, and is the only 'write to' file using the command. This is implemented for the testing phase and results in only one x axis when extracting the recorded data for analysis. The second 'write to measure' file is configured to record the test values. 'Write to measure' files three, four and five are configured for the comparator conditions of less than, equal to or greater than. Each of the less than, equal to and greater than signals are produced as 1 or 0. In order for these output signals to be displayed on the logs, multiplication by a factor of 200 is required, resulting in the signals being produced as 0 or 200.



LabVIEW front panel view is a good design

Figure 73 - Element 3 - FPGA Magnitude Comparator Front Page

Within LabView alterations were made to the front screen, aesthetic alterations and the addition of a load input indicator demonstrated in the image above.

3.3 Implementation

Illustrated in the image below, file and file two, with both 'write to measure' functions connected to the required data line. 'Write to measure' file implements the x axis and records the actual input from analogue value, while 'write to measure' file 2 records the set point values. Each 'write to measure' function is connected to the required data line and automatically records to the pre-set test files, as shown in appendix 5.3.1.

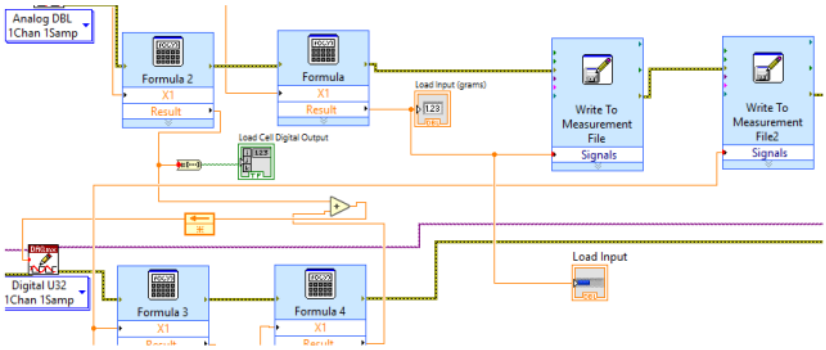


Figure 74 - Element 3 - File & File 2 Connections

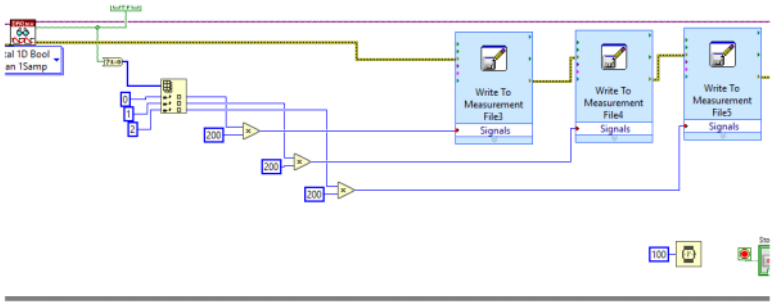


Figure 75 - Element 3 - File 3, File 4 & File 5 Connections

Illustrated in the image above, the implementation of 'write to' files three, four and five. Firstly, the data is recorded from the magnitude comparator. A binary to decimal converter is used as input to index array, with elements 0, 1 and 2 extracted from channels 21 – 23 on the Elvis II board. 'Write to measure' file three (Less than) is on channel 0 with the output multiplied by 200, 'write to measure' file four (Equal to) on channel 1, with the output multiplied by 200, and 'write to measure' file 5 (Greater Than) on channel 2 with the output multiplied by 200. All files' writes will create .lvm text files which are then plotted on an Excel® graph for each set point trend, the trend values for each set point recorded on the Excel® graphs.

Good explanation

3.4 Testing and Analysis

Shown in the image below, the LabView front page 'Equal to' test result of the implemented magnitude comparator with data logging. The magnitude comparator set point was set at 200grams, with the analogue input provided by a potentiometer. The potentiometer is then adjusted to represent three different masses placed onto a load cell with the magnitude comparator producing the required outputs; less than, equal to and greater than. LabView produces a file for each of the 'write to measure' functions during the testing period, data from the files then used to produce the data obtained. See appendix 5.3.2 for further 200gram set point test images

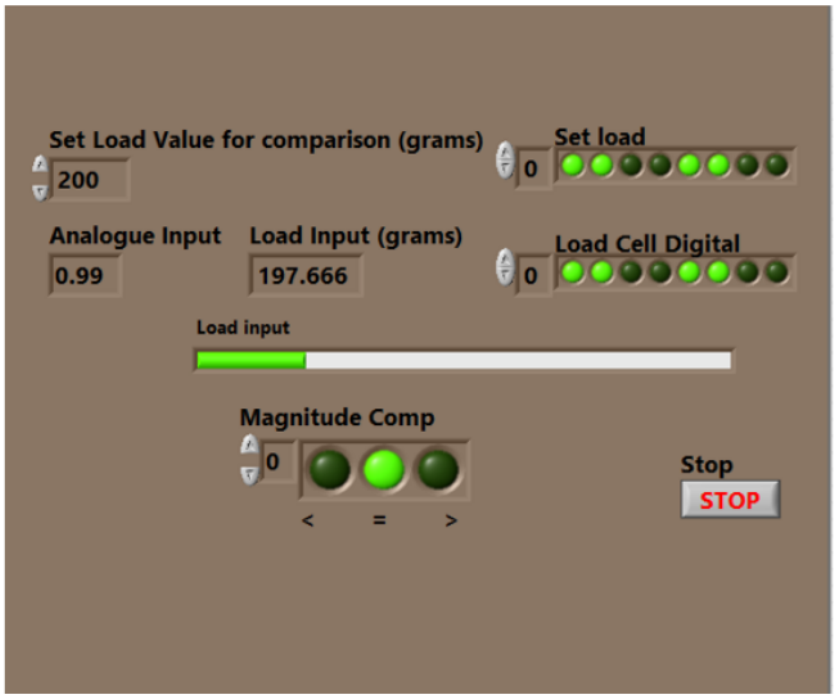


Figure 76 - Element 3 - 200g Equal to Test

Good test result

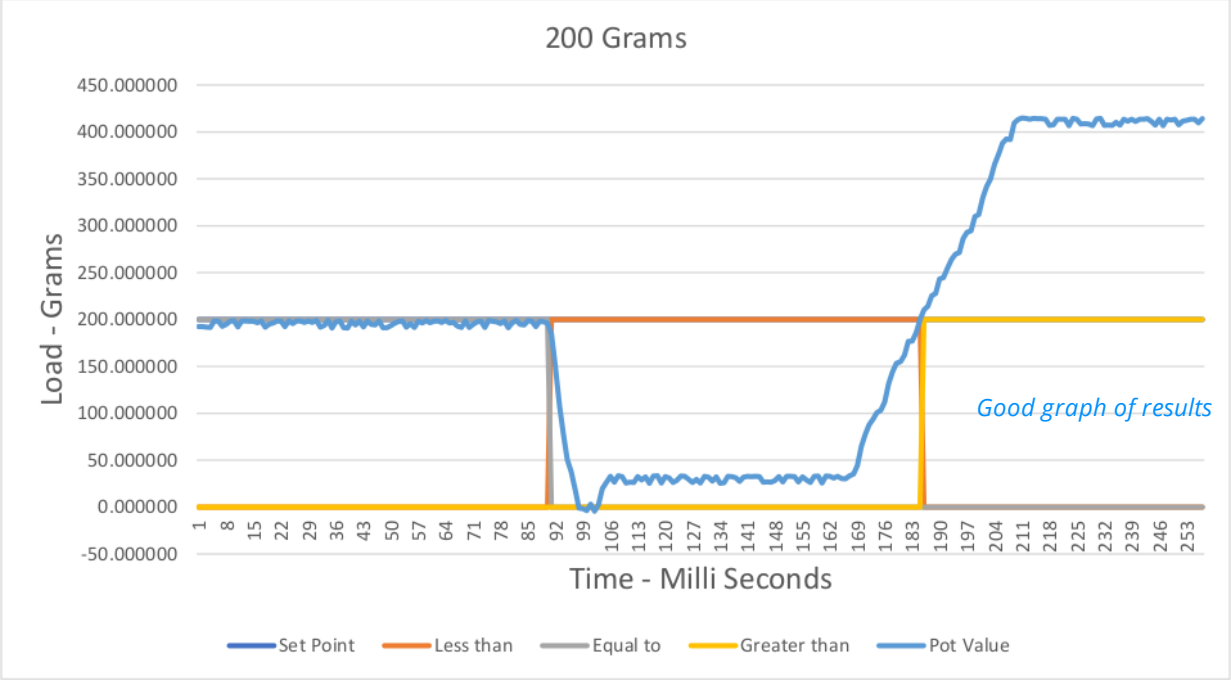


Figure 77 - Element 3 - 200g Test Result

Illustrated on the graph above, the set point value of 200 is not visible as each of the set outputs are a multiple of 200, resulting in the trend-line overlapping the setpoint data. The pot value (input) represented by the light blue line shows that the first test was carried out at equal to the set point of 200, followed by less than, finishing with greater than.

When input and set point values are equal, the 'equal to output', depicted in grey, is measured at 200. When the input value is less than, the 'equal to output' reduces down to 0 and the 'less than output', depicted in orange, rises to 200. Finally, when the input value is greater than, the 'less than output' reduces down to 0 and the 'greater than output', depicted in yellow, increases to 200.

Shown in the image below, the LabView front page 'Less Than' test result of implemented magnitude comparator with data logging. The magnitude comparator set point was set at 500grams, with the analogue input provided by a potentiometer. The potentiometer is then adjusted to represent three different masses placed onto a load cell with the magnitude comparator producing the required outputs; less than, equal to and greater than. LabView produces a file for each of the 'write to measurement' function during the testing period, data from the files are then used to produce the data obtained. See appendix 5.3.3 for further 500gram set point test images

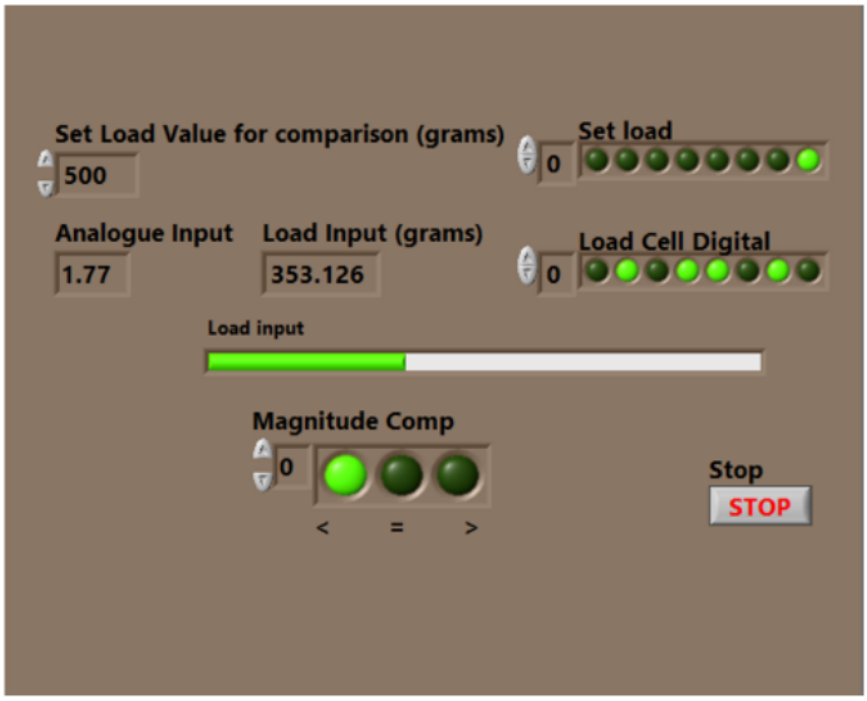


Figure 78 - Element 3 - 500g Less Than Test

Good result

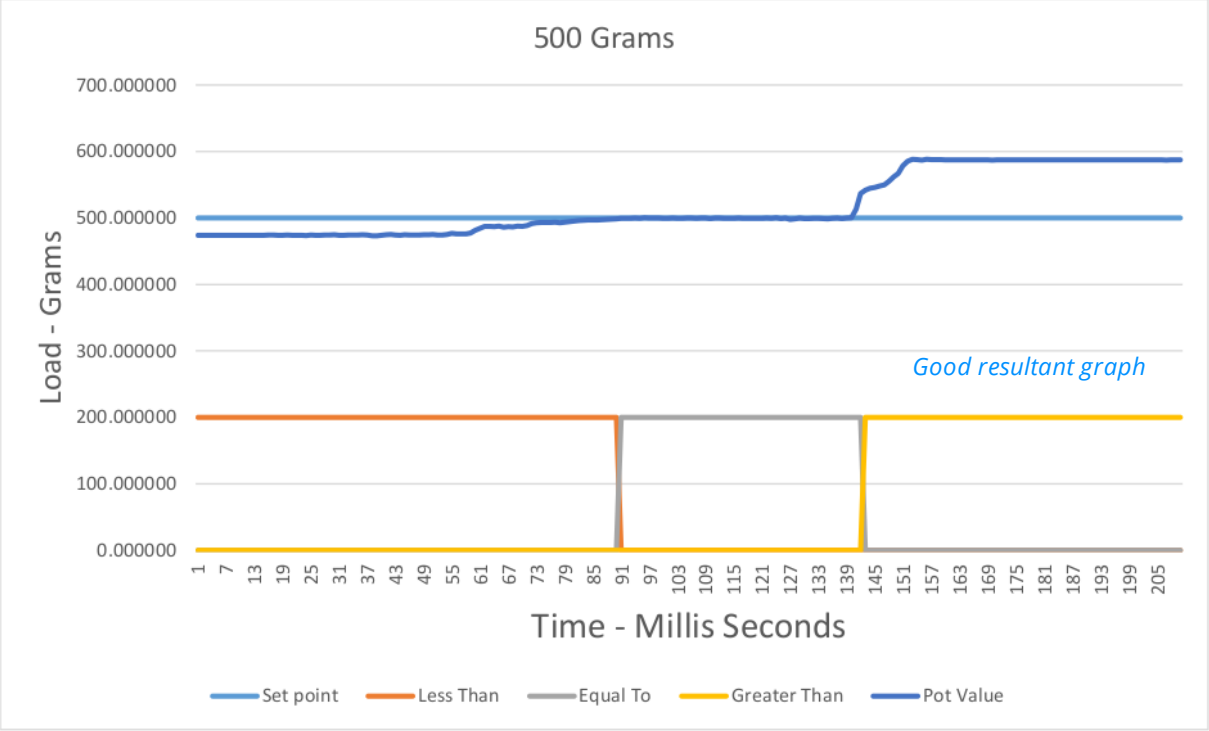


Figure 79 - Element 3 - 500g Test Result

Illustrated on the graph above, the pot value (input) represented by the dark blue line shows the first test was carried out at less than the setpoint of 500, the setpoint value of 500 represented by the light blue line, followed by equal to, finishing with greater than.

When the input value is less than the set point, the 'less than output', depicted in orange, is at 200. When the input value is equal to, the 'less than output' reduces to 0 and 'equal to output', depicted in grey, rises to 200. Finally, when the input value is greater than, the 'equal to output' reduces to 0 and the 'greater than output', depicted in yellow rises to 200.

Shown in the image below, the LabView front page Greater Than test results of implemented magnitude comparator with data logging. The magnitude comparator set point was set at 700grams, with the analogue input provided by a potentiometer. The potentiometer is then adjusted to represent three different masses placed onto a load cell with the magnitude comparator producing the required outputs; less than, equal to and greater than. LabView produces a file for each of the 'write to measurement' functions during the testing period, data from the files are then used to produce the data obtained. 5.3.4 for further 700gram set point test images

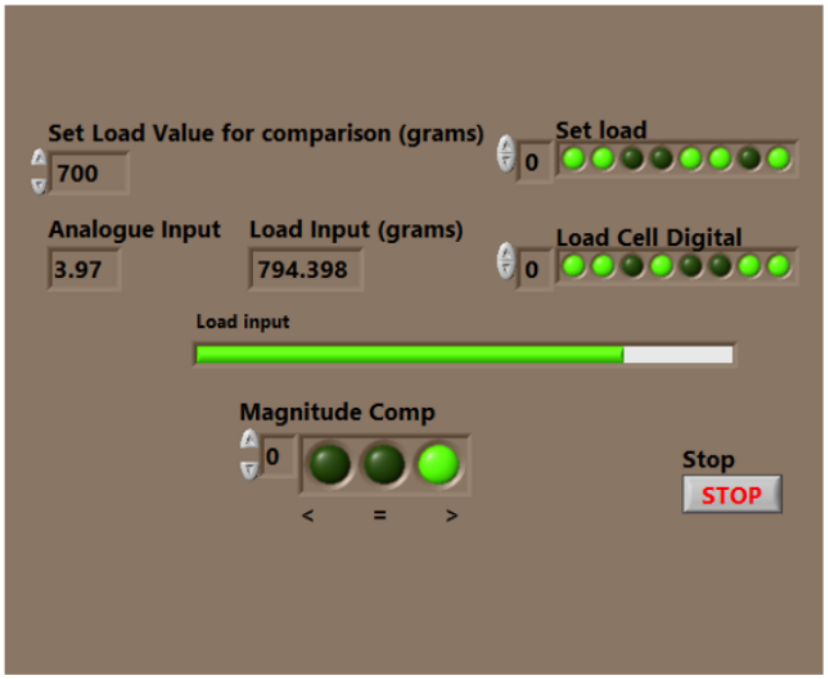


Figure 80 - Element 3 - 700g Greater Than Test

Good result

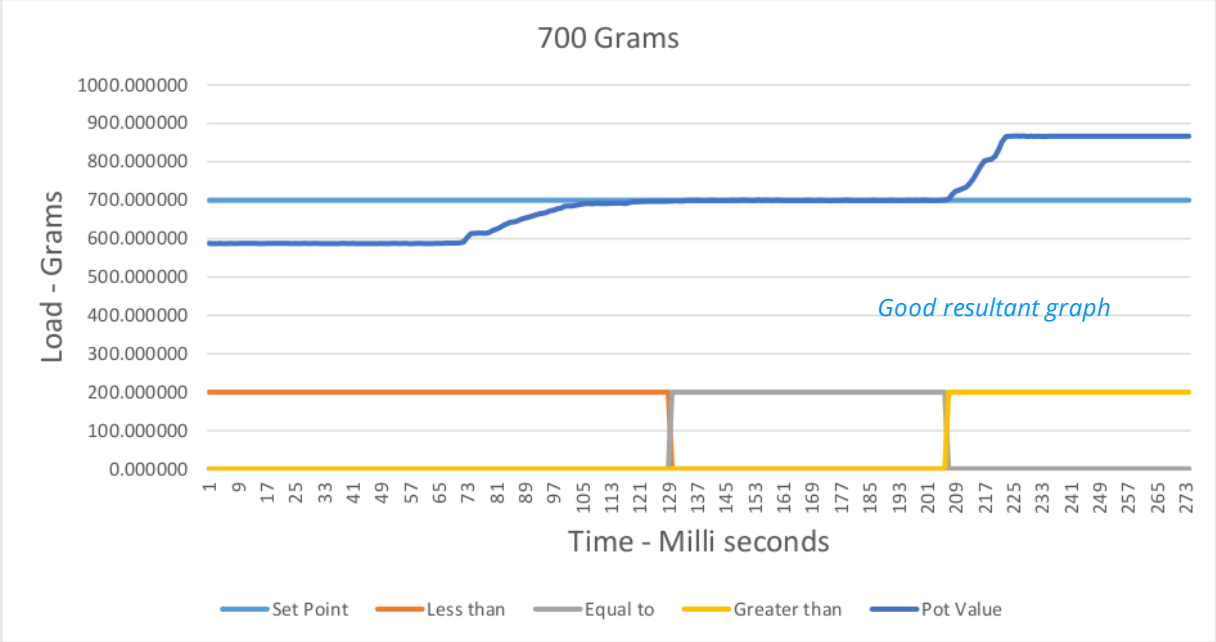


Figure 81 - Element 3 - 700g Test Result

Illustrated on the graph above, the pot value (input) represented by the dark blue line shows that the first test was carried out at less than the set point of 700, the set point value (700) represented by the light blue line, followed by equal, finishing with greater than.

When the input value is less than the set point, the 'less than output', depicted in orange, is at 200. When the input value is equal to, the 'less than output' reduces down to 0 and the 'equal to output', depicted in grey, rises to 200. Finally, when the input value is greater than, the 'equal to output' reduces down to 0 and the 'greater than output', depicted in yellow rises to 200.

3.5 Conclusions and Recommendations

The aim for element 3 was the implementation of a data logger into the previously designed magnitude comparator, allowing for the recording and extraction of data which could then be compared. Addition and configuration of 'the write to' measure blocks allowed recording of analogue input, load set point and the three outputs, with the data automatically placed and saved into test files. Utilising the recorded data, response graphs were able to be produced to display the operation of the magnitude comparator, ensuring that the outputs change when the analogue input varies to the set point value. The outputs of less than, equal to and greater than were proven to be functioning correctly when the circuit was tested at three different set points, resulting in a successful design, implementation and testing of an 8-bit magnitude comparator.

Despite the successful operation of the magnitude comparator, improvements to the system could be made by increasing the number of bits on the magnitude comparator, resulting in greater accuracy for the equal to function. Another improvement to the magnitude comparator would be the design and implementation of a real time data logger, able to produce plotted graphs displaying the real time output data, allowing for better monitoring of the system while the magnitude comparator is in operation.

Good evaluation

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An extensive reference list

5. *Appendix*

5.1. *Element 1*

Intentionally left blank

5.2. *Element 2*

5.2.1. *Load Cell Testing*

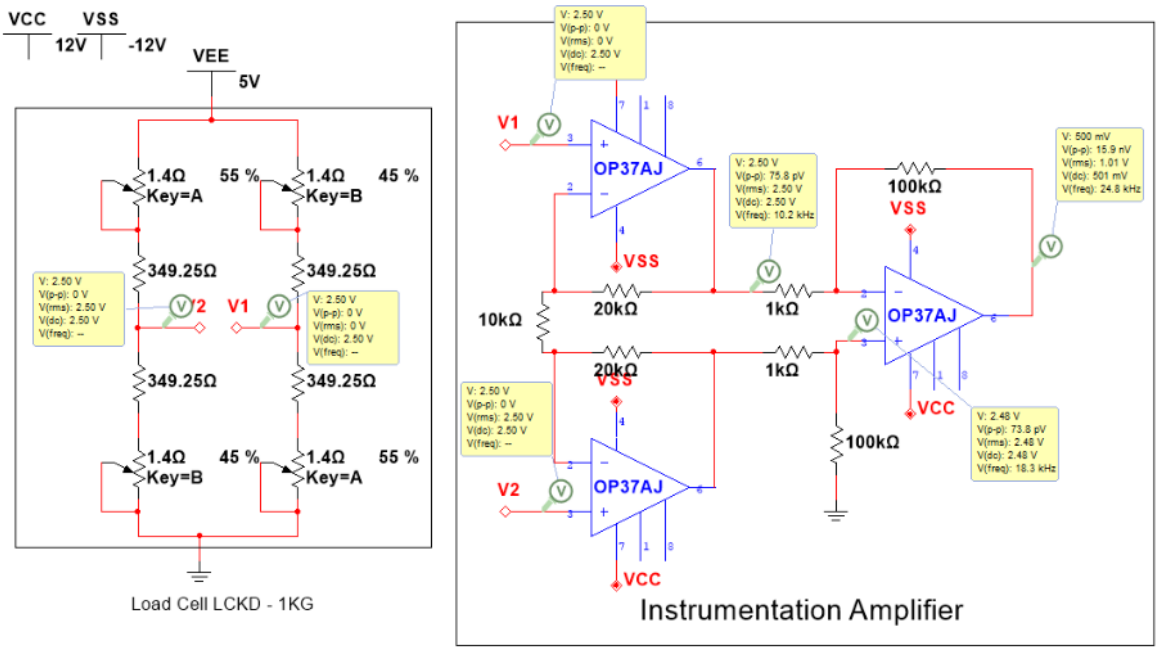


Figure 82 - Element 2 - Load Cell 55% Load Test

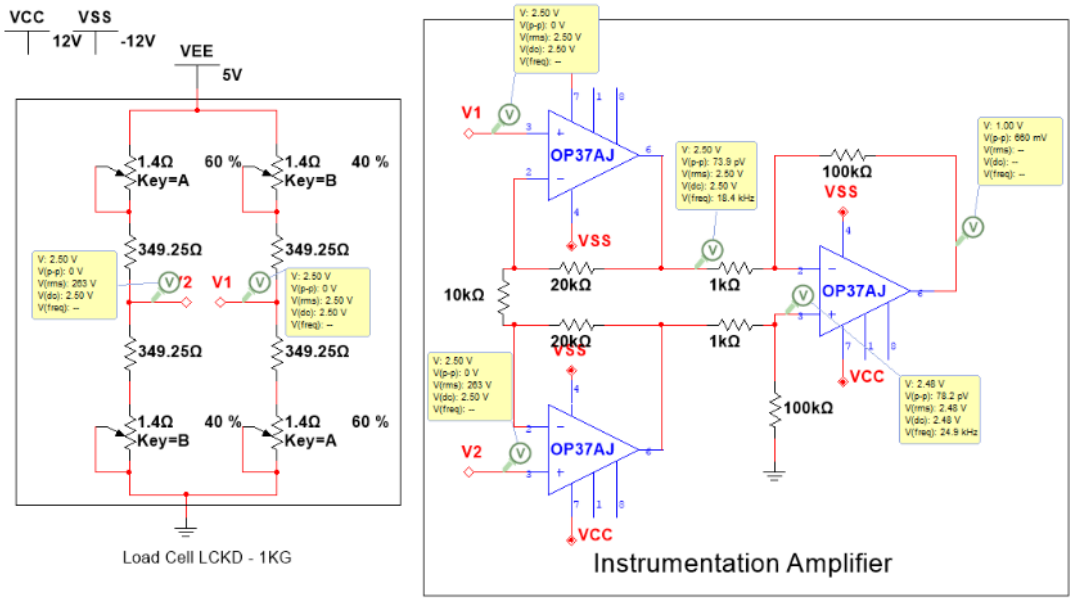


Figure 83 - Element 2 - Load Cell 60% Load Test

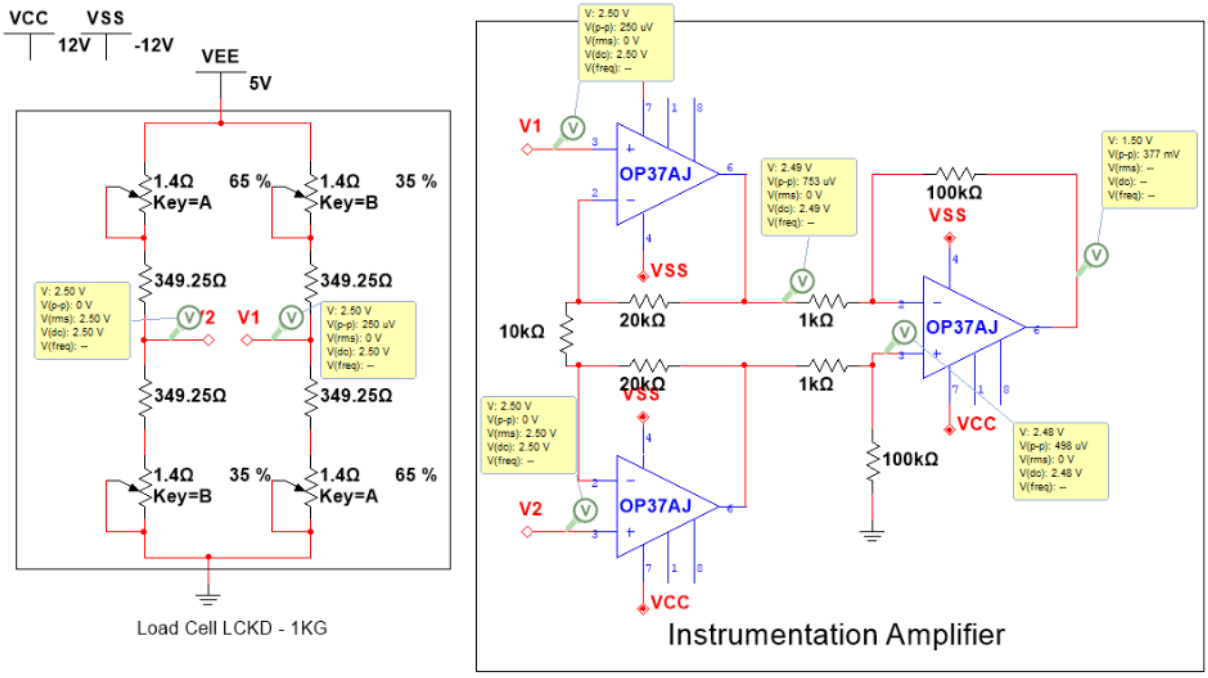


Figure 84 - Element 2 - Load Cell 65% Load Test

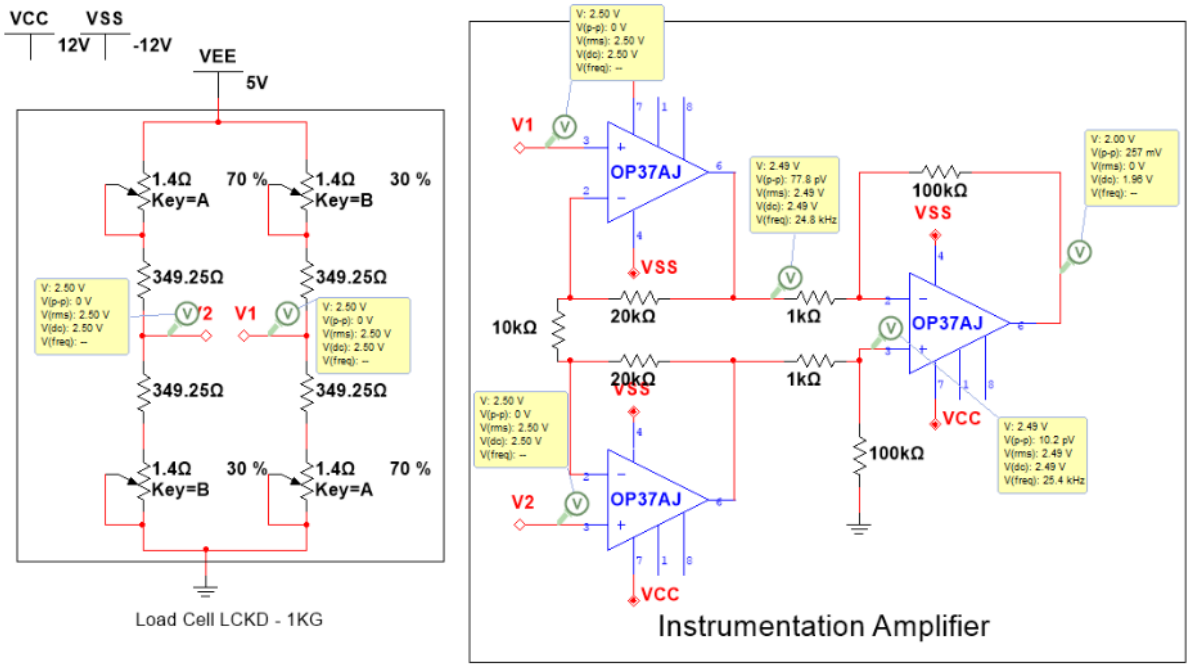


Figure 85 - Element 2 - Load Cell 70% Load Test

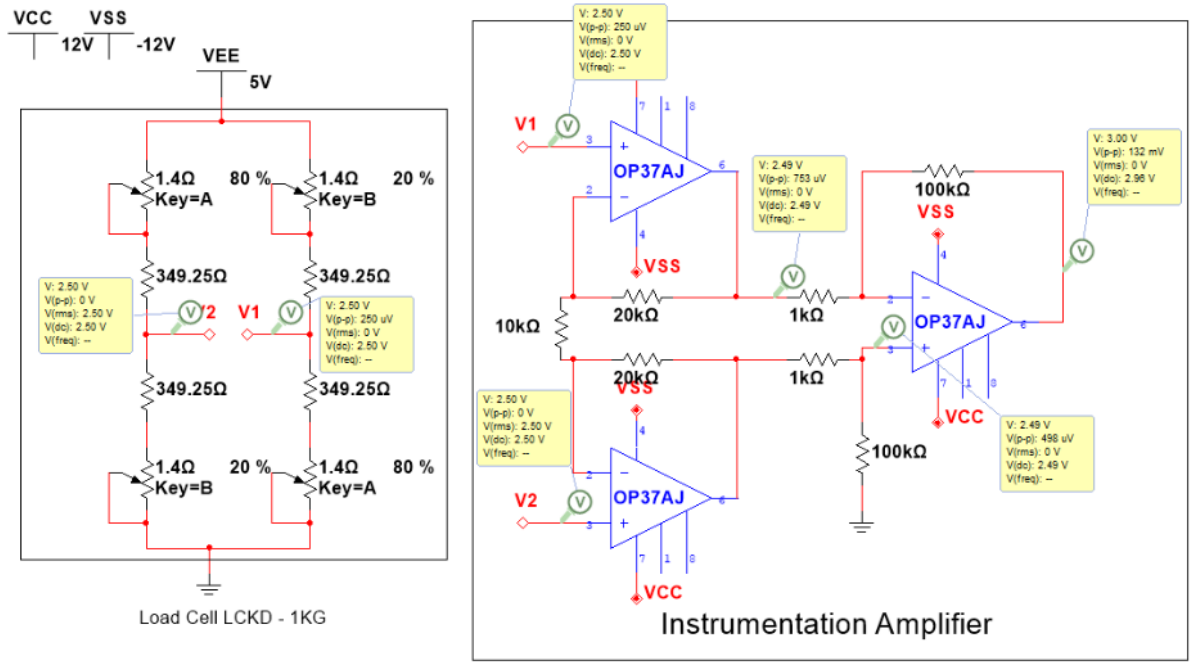


Figure 86 - Element 2 - Load Cell 80% Load Test

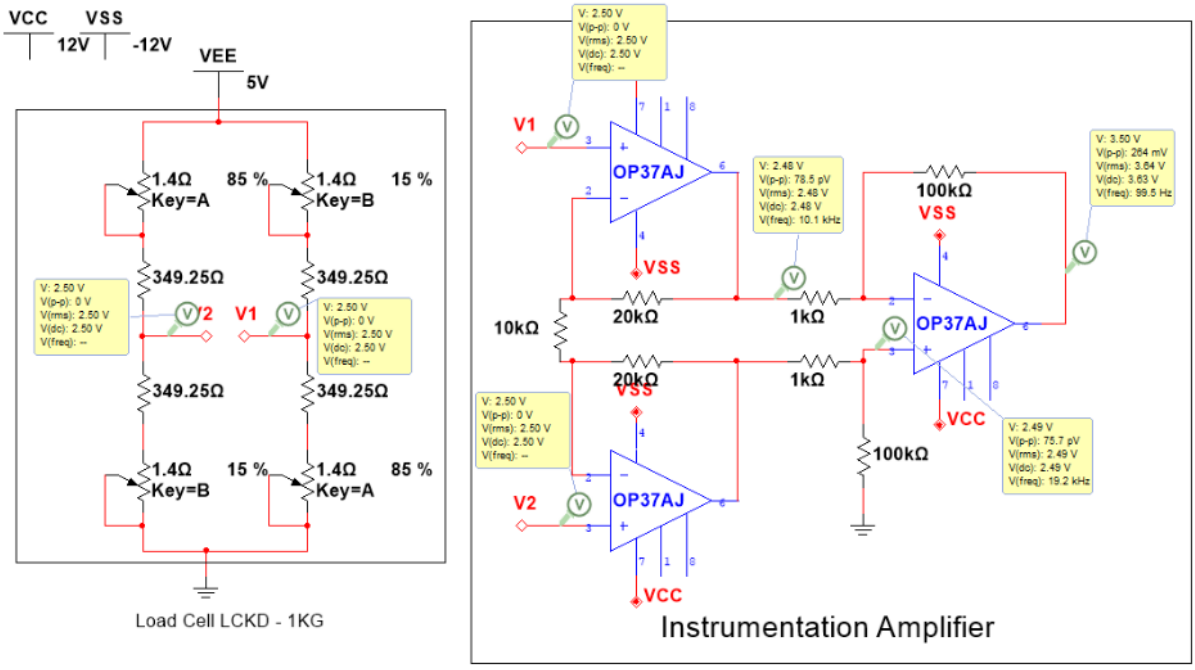


Figure 87 - Element 2 - Load Cell 85% Load Test

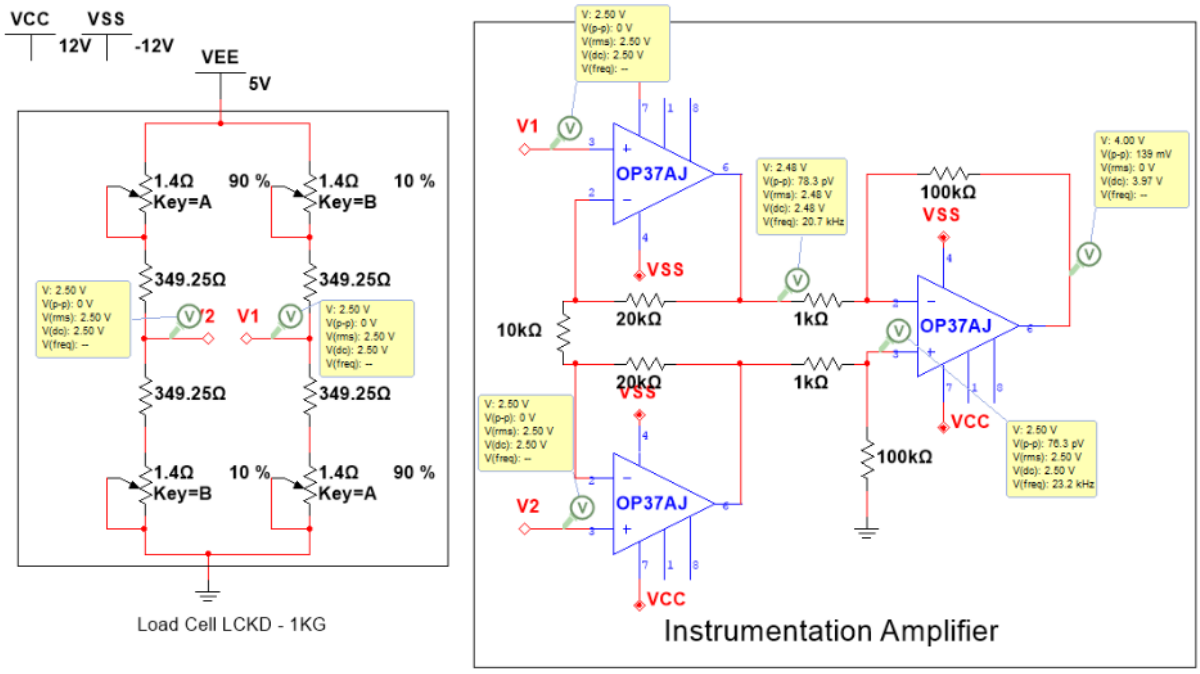


Figure 88 - Element 2 - Load Cell 90% Load Test

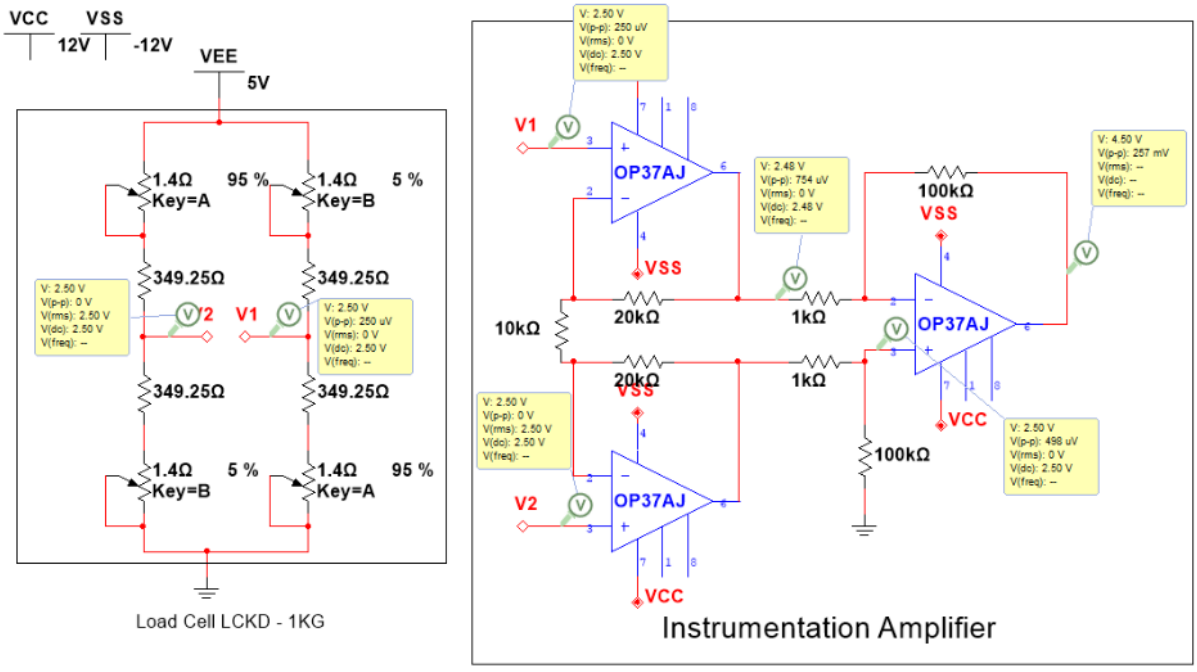


Figure 89 - Element 2 - Load Cell 95% Load Test

Good set of results for load cell and instrumentation amplifier

5.3. *Element 3*

5.3.1. *Data Logging*

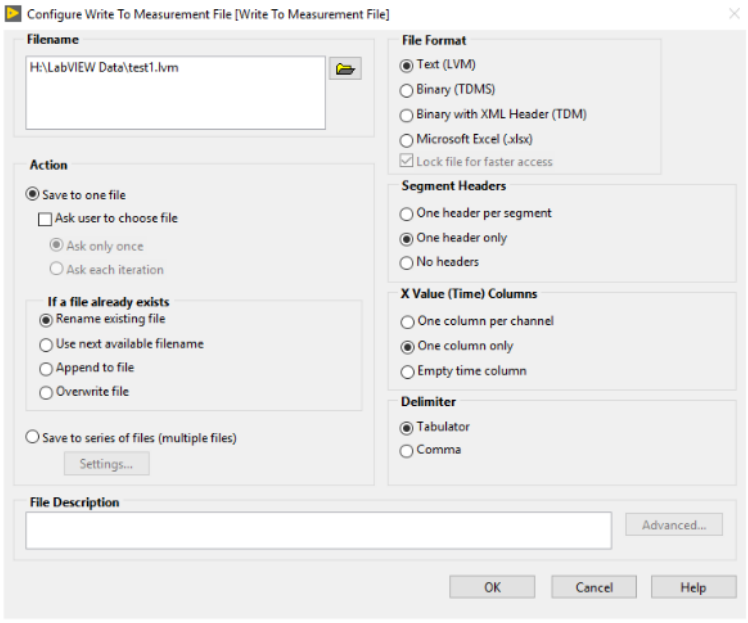


Figure 90 - Element 3 - Data Logging File 1

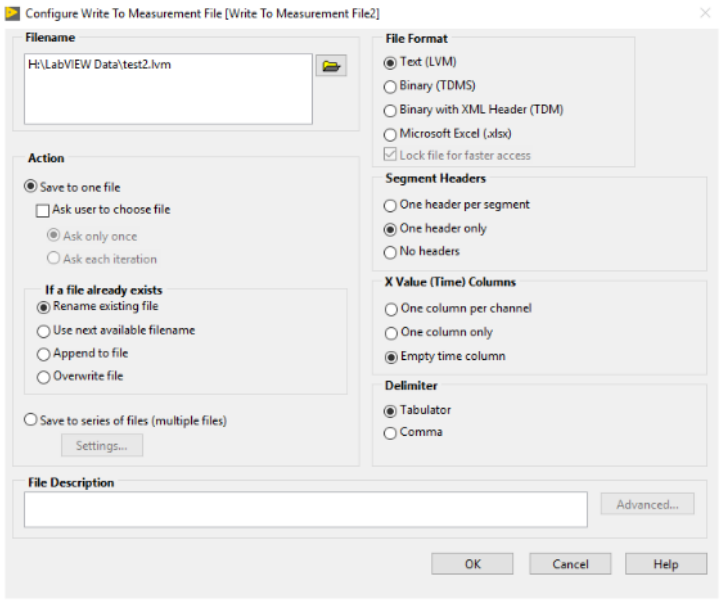


Figure 91 - Element 3 - Data Logging File 2

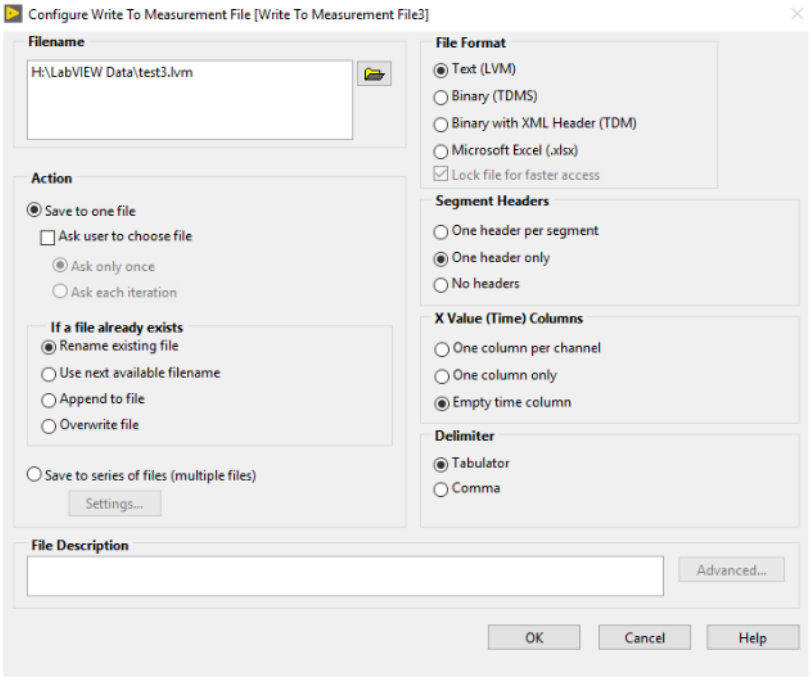


Figure 92 - Element 3 - Data Logging File 3

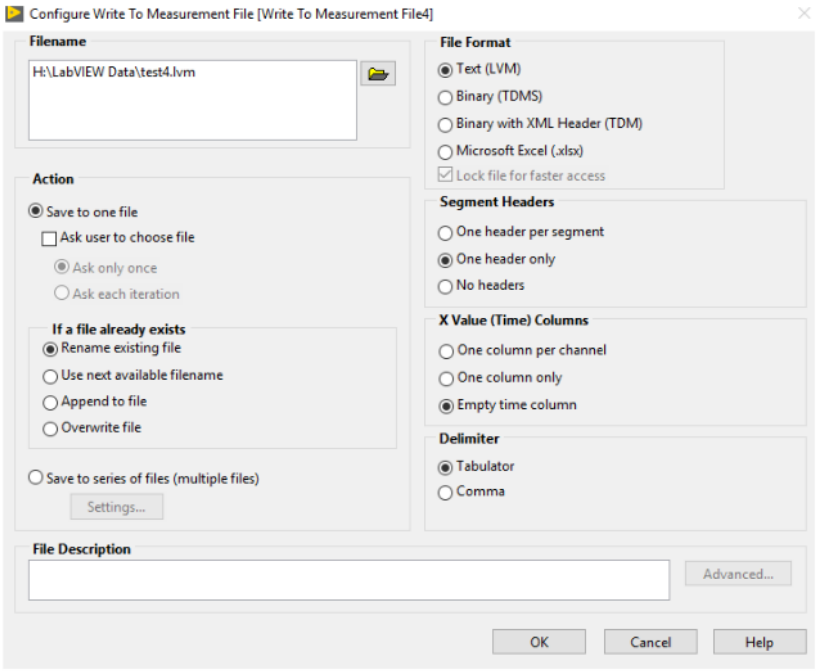


Figure 93 - Element 3 - Data Logging File 4

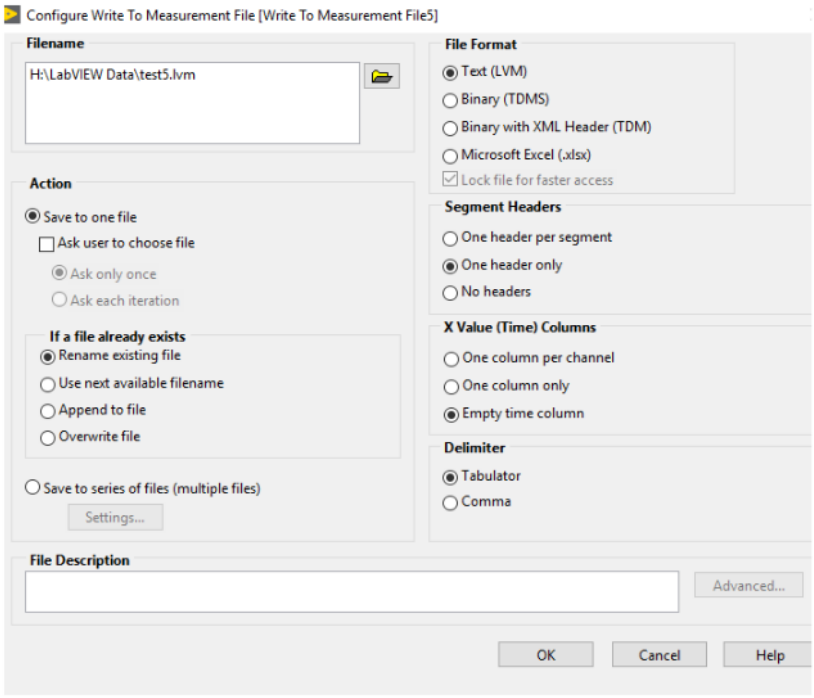


Figure 94 - Element 3 - Data Logging File 5

Text file configuration

5.3.2. *200 Gram Test Images*

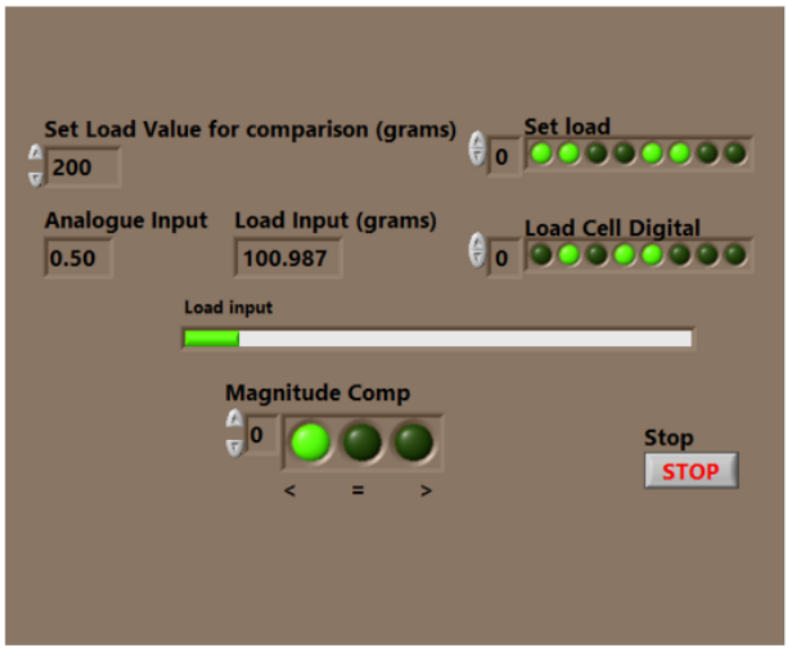


Figure 95 - Element 3 - 200g Less Than Test

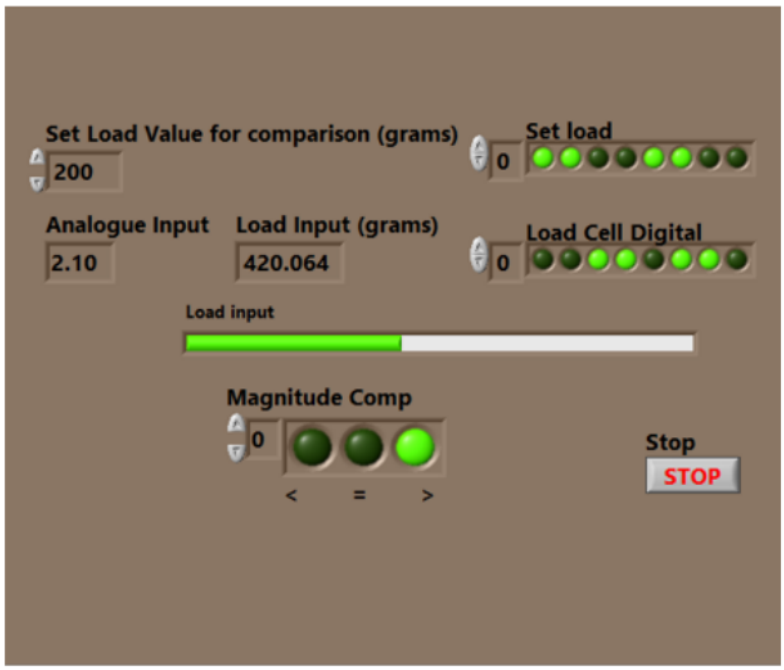


Figure 96 - Element 3 - 200g Greater Than Test

5.3.3. *500 Gram Test images*

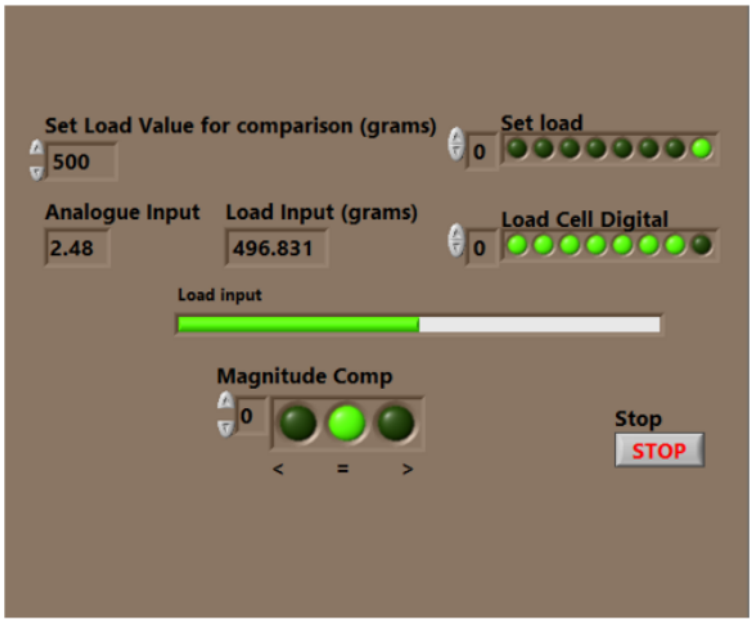


Figure 97 - Element 3 - 500g Equal to Test

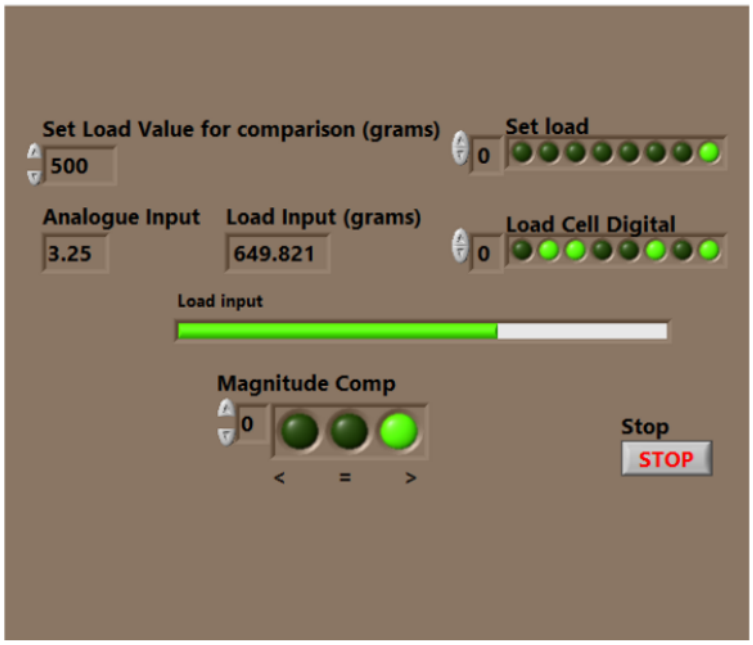


Figure 98 - Element 3 - 500g Greater Than Test

5.3.4. *700 Gram Test Images*

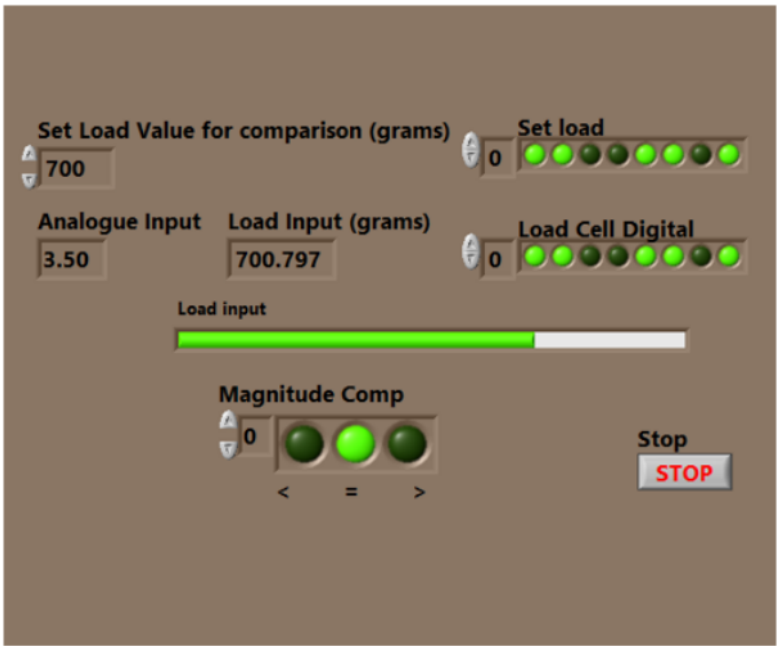


Figure 99 - Element 3 - 700g Equal to Test

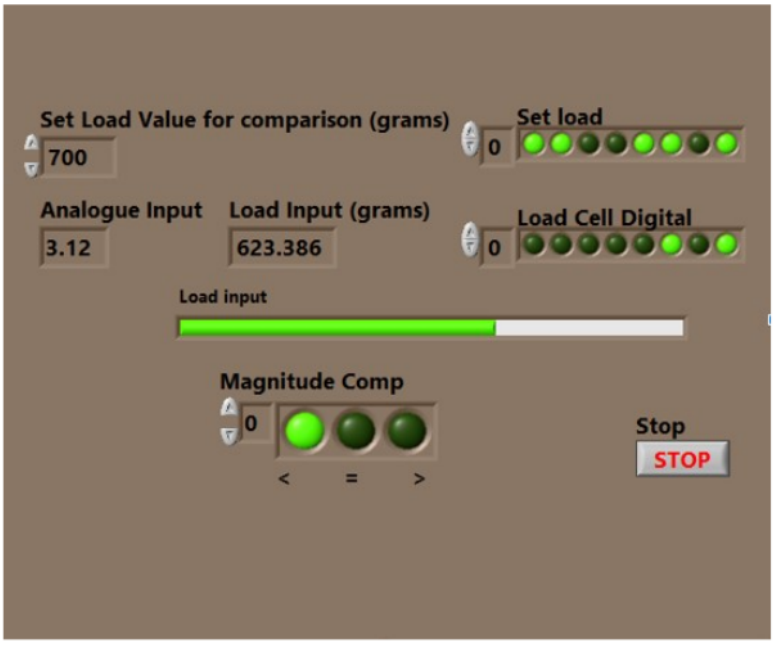


Figure 100 - Element 3 - 700g Less Than Test

Very good set of results

5.3.5. *200 Gram Data*

Set Point	Less than	Equal to	Greater than	X Axis	Pot Value
200.000000	0.000000	200.000000	0.000000	0.000000	192.430951
200.000000	0.000000	200.000000	0.000000	0.097350	192.398832
200.000000	0.000000	200.000000	0.000000	0.197093	191.724320
200.000000	0.000000	200.000000	0.000000	0.297626	191.499483
200.000000	0.000000	200.000000	0.000000	0.397429	198.405196
200.000000	0.000000	200.000000	0.000000	0.497087	198.180359
200.000000	0.000000	200.000000	0.000000	0.597285	192.720028
200.000000	0.000000	200.000000	0.000000	0.698545	194.839921
200.000000	0.000000	200.000000	0.000000	0.798225	198.180359
200.000000	0.000000	200.000000	0.000000	0.898552	198.726392
200.000000	0.000000	200.000000	0.000000	0.998129	192.206114
200.000000	0.000000	200.000000	0.000000	1.099135	198.340957
200.000000	0.000000	200.000000	0.000000	1.199143	198.276718
200.000000	0.000000	200.000000	0.000000	1.301150	198.212479
200.000000	0.000000	200.000000	0.000000	1.401920	198.148239
200.000000	0.000000	200.000000	0.000000	1.500231	196.542259
200.000000	0.000000	200.000000	0.000000	1.600502	198.437316
200.000000	0.000000	200.000000	0.000000	1.700259	191.949157
200.000000	0.000000	200.000000	0.000000	1.801206	195.257475
200.000000	0.000000	200.000000	0.000000	1.901672	196.317422
200.000000	0.000000	200.000000	0.000000	2.001525	198.276718
200.000000	0.000000	200.000000	0.000000	2.102111	198.212479
200.000000	0.000000	200.000000	0.000000	2.201138	192.527310
200.000000	0.000000	200.000000	0.000000	2.301167	198.244598
200.000000	0.000000	200.000000	0.000000	2.401952	195.739269
200.000000	0.000000	200.000000	0.000000	2.501900	198.308837
200.000000	0.000000	200.000000	0.000000	2.600604	198.244598
200.000000	0.000000	200.000000	0.000000	2.703089	196.831336
200.000000	0.000000	200.000000	0.000000	2.803117	198.469435
200.000000	0.000000	200.000000	0.000000	2.904122	197.024053
200.000000	0.000000	200.000000	0.000000	3.005118	198.951229
200.000000	0.000000	200.000000	0.000000	3.102766	191.852799
200.000000	0.000000	200.000000	0.000000	3.202669	193.683615
200.000000	0.000000	200.000000	0.000000	3.302786	198.886990
200.000000	0.000000	200.000000	0.000000	3.402776	191.114048
200.000000	0.000000	200.000000	0.000000	3.503130	197.634326
200.000000	0.000000	200.000000	0.000000	3.603071	198.244598
200.000000	0.000000	200.000000	0.000000	3.703496	191.210407

200.000000	0.000000	200.000000	0.000000	3.803513	191.114048
200.000000	0.000000	200.000000	0.000000	3.903330	198.116120
200.000000	0.000000	200.000000	0.000000	4.004052	194.165409
200.000000	0.000000	200.000000	0.000000	4.104085	198.212479
200.000000	0.000000	200.000000	0.000000	4.205225	192.302473
200.000000	0.000000	200.000000	0.000000	4.303626	198.244598
200.000000	0.000000	200.000000	0.000000	4.403838	194.904160
200.000000	0.000000	200.000000	0.000000	4.504271	194.165409
200.000000	0.000000	200.000000	0.000000	4.604270	198.276718
200.000000	0.000000	200.000000	0.000000	4.704301	191.403124
200.000000	0.000000	200.000000	0.000000	4.805322	191.403124
200.000000	0.000000	200.000000	0.000000	4.907335	193.458778
200.000000	0.000000	200.000000	0.000000	5.006581	195.867748
200.000000	0.000000	200.000000	0.000000	5.106506	197.698565
200.000000	0.000000	200.000000	0.000000	5.206447	198.244598
200.000000	0.000000	200.000000	0.000000	5.306218	191.724320
200.000000	0.000000	200.000000	0.000000	5.406469	195.289595
200.000000	0.000000	200.000000	0.000000	5.508477	191.499483
200.000000	0.000000	200.000000	0.000000	5.607586	198.212479
200.000000	0.000000	200.000000	0.000000	5.707567	196.349542
200.000000	0.000000	200.000000	0.000000	5.806913	198.790631
200.000000	0.000000	200.000000	0.000000	5.907992	196.702857
200.000000	0.000000	200.000000	0.000000	6.007920	198.084000
200.000000	0.000000	200.000000	0.000000	6.107162	198.533675
200.000000	0.000000	200.000000	0.000000	6.209170	196.959814
200.000000	0.000000	200.000000	0.000000	6.309176	199.079708
200.000000	0.000000	200.000000	0.000000	6.407139	196.381661
200.000000	0.000000	200.000000	0.000000	6.508151	196.895575
200.000000	0.000000	200.000000	0.000000	6.609173	193.169702
200.000000	0.000000	200.000000	0.000000	6.708763	191.595842
200.000000	0.000000	200.000000	0.000000	6.809294	198.308837
200.000000	0.000000	200.000000	0.000000	6.911302	191.499483
200.000000	0.000000	200.000000	0.000000	7.011694	194.807801
200.000000	0.000000	200.000000	0.000000	7.111634	197.634326
200.000000	0.000000	200.000000	0.000000	7.211314	198.084000
200.000000	0.000000	200.000000	0.000000	7.311157	191.435244
200.000000	0.000000	200.000000	0.000000	7.411088	198.951229
200.000000	0.000000	200.000000	0.000000	7.511170	198.212479
200.000000	0.000000	200.000000	0.000000	7.613163	197.537967
200.000000	0.000000	200.000000	0.000000	7.712132	195.578671
200.000000	0.000000	200.000000	0.000000	7.812496	198.244598

200.000000	0.000000	200.000000	0.000000	7.912792	191.210407
200.000000	0.000000	200.000000	0.000000	8.014096	196.670738
200.000000	0.000000	200.000000	0.000000	8.114496	198.983349
200.000000	0.000000	200.000000	0.000000	8.216503	194.743562
200.000000	0.000000	200.000000	0.000000	8.316058	194.326007
200.000000	0.000000	200.000000	0.000000	8.415054	198.694273
200.000000	0.000000	200.000000	0.000000	8.515084	198.019761
200.000000	0.000000	200.000000	0.000000	8.615530	192.527310
200.000000	0.000000	200.000000	0.000000	8.715313	198.051881
200.000000	0.000000	200.000000	0.000000	8.815045	197.409489
200.000000	0.000000	200.000000	0.000000	8.916033	196.124705
200.000000	200.000000	0.000000	0.000000	9.016215	185.107686
200.000000	200.000000	0.000000	0.000000	9.115108	150.450689
200.000000	200.000000	0.000000	0.000000	9.214462	108.438389
200.000000	200.000000	0.000000	0.000000	9.317133	77.828556
200.000000	200.000000	0.000000	0.000000	9.415518	50.655533
200.000000	200.000000	0.000000	0.000000	9.515092	37.775657
200.000000	200.000000	0.000000	0.000000	9.616117	19.178539
200.000000	200.000000	0.000000	0.000000	9.715106	-0.960298
200.000000	200.000000	0.000000	0.000000	9.817119	-1.570566
200.000000	200.000000	0.000000	0.000000	9.918141	-3.754681
200.000000	200.000000	0.000000	0.000000	10.018146	3.150979
200.000000	200.000000	0.000000	0.000000	10.119118	-4.364949
200.000000	200.000000	0.000000	0.000000	10.218625	2.540711
200.000000	200.000000	0.000000	0.000000	10.318630	19.820926
200.000000	200.000000	0.000000	0.000000	10.419255	26.437516
200.000000	200.000000	0.000000	0.000000	10.519755	32.700794
200.000000	200.000000	0.000000	0.000000	10.619708	26.501755
200.000000	200.000000	0.000000	0.000000	10.719654	33.535898
200.000000	200.000000	0.000000	0.000000	10.819077	32.604436
200.000000	200.000000	0.000000	0.000000	10.920391	25.730890
200.000000	200.000000	0.000000	0.000000	11.020385	26.630232
200.000000	200.000000	0.000000	0.000000	11.119720	26.212680
200.000000	200.000000	0.000000	0.000000	11.220667	32.540198
200.000000	200.000000	0.000000	0.000000	11.321802	28.942827
200.000000	200.000000	0.000000	0.000000	11.421469	32.315362
200.000000	200.000000	0.000000	0.000000	11.522211	25.506054
200.000000	200.000000	0.000000	0.000000	11.622161	33.086227
200.000000	200.000000	0.000000	0.000000	11.723169	33.503779
200.000000	200.000000	0.000000	0.000000	11.822512	25.730890
200.000000	200.000000	0.000000	0.000000	11.922485	32.379601

200.000000	200.000000	0.000000	0.000000	12.024469	31.126945
200.000000	200.000000	0.000000	0.000000	12.122249	26.244800
200.000000	200.000000	0.000000	0.000000	12.223512	28.717992
200.000000	200.000000	0.000000	0.000000	12.322817	33.150466
200.000000	200.000000	0.000000	0.000000	12.422844	32.861391
200.000000	200.000000	0.000000	0.000000	12.523312	29.392499
200.000000	200.000000	0.000000	0.000000	12.623670	26.180561
200.000000	200.000000	0.000000	0.000000	12.722683	29.617334
200.000000	200.000000	0.000000	0.000000	12.822850	25.730890
200.000000	200.000000	0.000000	0.000000	12.926033	32.700794
200.000000	200.000000	0.000000	0.000000	13.023429	32.026287
200.000000	200.000000	0.000000	0.000000	13.124415	27.625933
200.000000	200.000000	0.000000	0.000000	13.224442	32.154765
200.000000	200.000000	0.000000	0.000000	13.326449	25.506054
200.000000	200.000000	0.000000	0.000000	13.428437	26.084203
200.000000	200.000000	0.000000	0.000000	13.528462	32.700794
200.000000	200.000000	0.000000	0.000000	13.628569	32.379601
200.000000	200.000000	0.000000	0.000000	13.729375	31.319661
200.000000	200.000000	0.000000	0.000000	13.831382	27.497455
200.000000	200.000000	0.000000	0.000000	13.931270	32.026287
200.000000	200.000000	0.000000	0.000000	14.033035	32.765033
200.000000	200.000000	0.000000	0.000000	14.132918	32.540198
200.000000	200.000000	0.000000	0.000000	14.233478	32.732914
200.000000	200.000000	0.000000	0.000000	14.333058	32.604436
200.000000	200.000000	0.000000	0.000000	14.433954	26.501755
200.000000	200.000000	0.000000	0.000000	14.533980	26.758710
200.000000	200.000000	0.000000	0.000000	14.634320	26.533874
200.000000	200.000000	0.000000	0.000000	14.734059	28.428917
200.000000	200.000000	0.000000	0.000000	14.834046	32.572317
200.000000	200.000000	0.000000	0.000000	14.934025	26.951426
200.000000	200.000000	0.000000	0.000000	15.033969	32.893511
200.000000	200.000000	0.000000	0.000000	15.134138	32.732914
200.000000	200.000000	0.000000	0.000000	15.234126	32.604436
200.000000	200.000000	0.000000	0.000000	15.334138	26.790829
200.000000	200.000000	0.000000	0.000000	15.434286	32.283243
200.000000	200.000000	0.000000	0.000000	15.534545	28.814350
200.000000	200.000000	0.000000	0.000000	15.634486	26.180561
200.000000	200.000000	0.000000	0.000000	15.734686	32.668675
200.000000	200.000000	0.000000	0.000000	15.835149	33.118346
200.000000	200.000000	0.000000	0.000000	15.935174	25.666651
200.000000	200.000000	0.000000	0.000000	16.034500	33.086227

200.000000	200.000000	0.000000	0.000000	16.134486	32.893511
200.000000	200.000000	0.000000	0.000000	16.234393	31.159064
200.000000	200.000000	0.000000	0.000000	16.334589	32.765033
200.000000	200.000000	0.000000	0.000000	16.434515	30.484557
200.000000	200.000000	0.000000	0.000000	16.535306	30.227602
200.000000	200.000000	0.000000	0.000000	16.636318	33.375301
200.000000	200.000000	0.000000	0.000000	16.736340	35.173987
200.000000	200.000000	0.000000	0.000000	16.835345	44.392251
200.000000	200.000000	0.000000	0.000000	16.936352	64.466877
200.000000	200.000000	0.000000	0.000000	17.036934	77.378884
200.000000	200.000000	0.000000	0.000000	17.136877	87.592864
200.000000	200.000000	0.000000	0.000000	17.236246	93.631319
200.000000	200.000000	0.000000	0.000000	17.338253	100.697599
200.000000	200.000000	0.000000	0.000000	17.436656	103.202916
200.000000	200.000000	0.000000	0.000000	17.537181	111.907291
200.000000	200.000000	0.000000	0.000000	17.637463	131.178982
200.000000	200.000000	0.000000	0.000000	17.736753	143.962546
200.000000	200.000000	0.000000	0.000000	17.838106	153.277207
200.000000	200.000000	0.000000	0.000000	17.938245	155.204379
200.000000	200.000000	0.000000	0.000000	18.040409	161.917362
200.000000	200.000000	0.000000	0.000000	18.139260	176.756597
200.000000	200.000000	0.000000	0.000000	18.239008	177.013553
200.000000	200.000000	0.000000	0.000000	18.339146	185.782197
200.000000	200.000000	0.000000	0.000000	18.439109	199.754220
200.000000	0.000000	0.000000	200.000000	18.539793	210.289453
200.000000	0.000000	0.000000	200.000000	18.639800	214.047449
200.000000	0.000000	0.000000	200.000000	18.739791	225.482040
200.000000	0.000000	0.000000	200.000000	18.840805	227.891014
200.000000	0.000000	0.000000	200.000000	18.941041	243.308455
200.000000	0.000000	0.000000	200.000000	19.041781	244.689601
200.000000	0.000000	0.000000	200.000000	19.142125	255.096382
200.000000	0.000000	0.000000	200.000000	19.243351	263.929303
200.000000	0.000000	0.000000	200.000000	19.345360	269.518136
200.000000	0.000000	0.000000	200.000000	19.444557	271.316841
200.000000	0.000000	0.000000	200.000000	19.543682	286.477364
200.000000	0.000000	0.000000	200.000000	19.643911	293.190397
200.000000	0.000000	0.000000	200.000000	19.744086	294.571548
200.000000	0.000000	0.000000	200.000000	19.844571	309.603614
200.000000	0.000000	0.000000	200.000000	19.944619	312.141080
200.000000	0.000000	0.000000	200.000000	20.045628	329.453674
200.000000	0.000000	0.000000	200.000000	20.145977	341.627107

200.000000	0.000000	0.000000	200.000000	20.244997	349.689201
200.000000	0.000000	0.000000	200.000000	20.344987	365.717044
200.000000	0.000000	0.000000	200.000000	20.443133	376.123910
200.000000	0.000000	0.000000	200.000000	20.544150	387.879824
200.000000	0.000000	0.000000	200.000000	20.644174	392.537225
200.000000	0.000000	0.000000	200.000000	20.746163	391.766344
200.000000	0.000000	0.000000	200.000000	20.845472	409.271761
200.000000	0.000000	0.000000	200.000000	20.945561	413.254648
200.000000	0.000000	0.000000	200.000000	21.045482	414.828532
200.000000	0.000000	0.000000	200.000000	21.147327	414.282490
200.000000	0.000000	0.000000	200.000000	21.246770	413.511609
200.000000	0.000000	0.000000	200.000000	21.347466	414.539451
200.000000	0.000000	0.000000	200.000000	21.447474	414.218250
200.000000	0.000000	0.000000	200.000000	21.547695	414.154010
200.000000	0.000000	0.000000	200.000000	21.647659	413.575849
200.000000	0.000000	0.000000	200.000000	21.747313	407.023358
200.000000	0.000000	0.000000	200.000000	21.846745	407.601518
200.000000	0.000000	0.000000	200.000000	21.947234	413.543729
200.000000	0.000000	0.000000	200.000000	22.047562	413.640089
200.000000	0.000000	0.000000	200.000000	22.147565	413.543729
200.000000	0.000000	0.000000	200.000000	22.247513	406.670037
200.000000	0.000000	0.000000	200.000000	22.346489	414.346731
200.000000	0.000000	0.000000	200.000000	22.447221	413.415249
200.000000	0.000000	0.000000	200.000000	22.547064	408.404520
200.000000	0.000000	0.000000	200.000000	22.647369	408.854200
200.000000	0.000000	0.000000	200.000000	22.748431	408.340280
200.000000	0.000000	0.000000	200.000000	22.849438	406.702157
200.000000	0.000000	0.000000	200.000000	22.950443	413.736449
200.000000	0.000000	0.000000	200.000000	23.047717	414.410971
200.000000	0.000000	0.000000	200.000000	23.147914	406.991238
200.000000	0.000000	0.000000	200.000000	23.248691	407.248198
200.000000	0.000000	0.000000	200.000000	23.348345	406.959118
200.000000	0.000000	0.000000	200.000000	23.449580	410.331723
200.000000	0.000000	0.000000	200.000000	23.551570	407.280318
200.000000	0.000000	0.000000	200.000000	23.649306	413.640089
200.000000	0.000000	0.000000	200.000000	23.750353	411.359565
200.000000	0.000000	0.000000	200.000000	23.851361	413.607969
200.000000	0.000000	0.000000	200.000000	23.951402	411.070484
200.000000	0.000000	0.000000	200.000000	24.051248	413.672209
200.000000	0.000000	0.000000	200.000000	24.151465	413.672209
200.000000	0.000000	0.000000	200.000000	24.250788	414.089770

200.000000	0.000000	0.000000	200.000000	24.352150	411.102604
200.000000	0.000000	0.000000	200.000000	24.451737	407.248198
200.000000	0.000000	0.000000	200.000000	24.551274	413.447369
200.000000	0.000000	0.000000	200.000000	24.650333	406.702157
200.000000	0.000000	0.000000	200.000000	24.751405	413.575849
200.000000	0.000000	0.000000	200.000000	24.851234	412.644367
200.000000	0.000000	0.000000	200.000000	24.953336	413.607969
200.000000	0.000000	0.000000	200.000000	25.052550	407.633639
200.000000	0.000000	0.000000	200.000000	25.153891	411.488045
200.000000	0.000000	0.000000	200.000000	25.253514	412.483767
200.000000	0.000000	0.000000	200.000000	25.354045	413.511609
200.000000	0.000000	0.000000	200.000000	25.453374	413.607969
200.000000	0.000000	0.000000	200.000000	25.555375	409.657202
200.000000	0.000000	0.000000	200.000000	25.655661	414.250370

Table 4 - Element 3 - 200 Gram Data

5.3.3. *500 Gram Data*

Set point	Less Than	Equal To	Greater Than	X Axis	Pot Value
500.000000	200.000000	0.000000	0.000000	0.000000	473.929602
500.000000	200.000000	0.000000	0.000000	0.103275	473.897482
500.000000	200.000000	0.000000	0.000000	0.205554	473.801122
500.000000	200.000000	0.000000	0.000000	0.303808	473.833242
500.000000	200.000000	0.000000	0.000000	0.406079	473.801122
500.000000	200.000000	0.000000	0.000000	0.507355	473.961723
500.000000	200.000000	0.000000	0.000000	0.604619	473.865362
500.000000	200.000000	0.000000	0.000000	0.704020	473.865362
500.000000	200.000000	0.000000	0.000000	0.807147	473.865362
500.000000	200.000000	0.000000	0.000000	0.906412	473.897482
500.000000	200.000000	0.000000	0.000000	1.005675	473.865362
500.000000	200.000000	0.000000	0.000000	1.105972	473.961723
500.000000	200.000000	0.000000	0.000000	1.208217	473.865362
500.000000	200.000000	0.000000	0.000000	1.309483	473.961723
500.000000	200.000000	0.000000	0.000000	1.408774	474.058083
500.000000	200.000000	0.000000	0.000000	1.508012	474.315045
500.000000	200.000000	0.000000	0.000000	1.609280	474.315045
500.000000	200.000000	0.000000	0.000000	1.708569	474.058083
500.000000	200.000000	0.000000	0.000000	1.808811	474.025963
500.000000	200.000000	0.000000	0.000000	1.909078	474.282925
500.000000	200.000000	0.000000	0.000000	2.010350	473.929602
500.000000	200.000000	0.000000	0.000000	2.108612	473.865362
500.000000	200.000000	0.000000	0.000000	2.209880	474.122324
500.000000	200.000000	0.000000	0.000000	2.310150	473.576280
500.000000	200.000000	0.000000	0.000000	2.411416	474.154444
500.000000	200.000000	0.000000	0.000000	2.510679	473.833242
500.000000	200.000000	0.000000	0.000000	2.610945	474.025963
500.000000	200.000000	0.000000	0.000000	2.710210	474.315045
500.000000	200.000000	0.000000	0.000000	2.810488	474.315045
500.000000	200.000000	0.000000	0.000000	2.911746	474.893209
500.000000	200.000000	0.000000	0.000000	3.012012	473.993843
500.000000	200.000000	0.000000	0.000000	3.112282	473.736881
500.000000	200.000000	0.000000	0.000000	3.212549	474.347165
500.000000	200.000000	0.000000	0.000000	3.310807	474.282925
500.000000	200.000000	0.000000	0.000000	3.413079	474.250805
500.000000	200.000000	0.000000	0.000000	3.513352	474.636247
500.000000	200.000000	0.000000	0.000000	3.612614	474.154444
500.000000	200.000000	0.000000	0.000000	3.712884	473.190837

500.000000	200.000000	0.000000	0.000000	3.813143	473.255078
500.000000	200.000000	0.000000	0.000000	3.914412	473.961723
500.000000	200.000000	0.000000	0.000000	4.013678	474.668368
500.000000	200.000000	0.000000	0.000000	4.115949	475.214412
500.000000	200.000000	0.000000	0.000000	4.216215	474.154444
500.000000	200.000000	0.000000	0.000000	4.316482	473.929602
500.000000	200.000000	0.000000	0.000000	4.414743	474.572007
500.000000	200.000000	0.000000	0.000000	4.515035	474.250805
500.000000	200.000000	0.000000	0.000000	4.616280	474.347165
500.000000	200.000000	0.000000	0.000000	4.717551	474.443526
500.000000	200.000000	0.000000	0.000000	4.816814	474.925330
500.000000	200.000000	0.000000	0.000000	4.918208	474.957450
500.000000	200.000000	0.000000	0.000000	5.019353	474.989570
500.000000	200.000000	0.000000	0.000000	5.120622	474.282925
500.000000	200.000000	0.000000	0.000000	5.220889	474.507767
500.000000	200.000000	0.000000	0.000000	5.320153	475.214412
500.000000	200.000000	0.000000	0.000000	5.419419	476.724063
500.000000	200.000000	0.000000	0.000000	5.519684	475.921057
500.000000	200.000000	0.000000	0.000000	5.619951	475.985297
500.000000	200.000000	0.000000	0.000000	5.720218	475.921057
500.000000	200.000000	0.000000	0.000000	5.821489	477.398588
500.000000	200.000000	0.000000	0.000000	5.920775	481.445739
500.000000	200.000000	0.000000	0.000000	6.020015	484.432922
500.000000	200.000000	0.000000	0.000000	6.121287	487.163145
500.000000	200.000000	0.000000	0.000000	6.220548	487.227385
500.000000	200.000000	0.000000	0.000000	6.321818	486.809822
500.000000	200.000000	0.000000	0.000000	6.420187	487.548588
500.000000	200.000000	0.000000	0.000000	6.520348	486.135296
500.000000	200.000000	0.000000	0.000000	6.619611	486.970423
500.000000	200.000000	0.000000	0.000000	6.720880	486.552860
500.000000	200.000000	0.000000	0.000000	6.820143	487.612828
500.000000	200.000000	0.000000	0.000000	6.921413	487.516468
500.000000	200.000000	0.000000	0.000000	7.021680	488.512196
500.000000	200.000000	0.000000	0.000000	7.123953	491.370901
500.000000	200.000000	0.000000	0.000000	7.222214	492.848434
500.000000	200.000000	0.000000	0.000000	7.322479	493.169636
500.000000	200.000000	0.000000	0.000000	7.422761	493.137516
500.000000	200.000000	0.000000	0.000000	7.522011	493.169636
500.000000	200.000000	0.000000	0.000000	7.621274	493.490839
500.000000	200.000000	0.000000	0.000000	7.723547	492.944794
500.000000	200.000000	0.000000	0.000000	7.821808	493.458719

500.000000	200.000000	0.000000	0.000000	7.923078	494.358087
500.000000	200.000000	0.000000	0.000000	8.022342	495.193215
500.000000	200.000000	0.000000	0.000000	8.121605	496.028342
500.000000	200.000000	0.000000	0.000000	8.222876	496.510147
500.000000	200.000000	0.000000	0.000000	8.322142	496.991951
500.000000	200.000000	0.000000	0.000000	8.422418	496.767109
500.000000	200.000000	0.000000	0.000000	8.525681	497.152552
500.000000	200.000000	0.000000	0.000000	8.621937	497.409515
500.000000	200.000000	0.000000	0.000000	8.722203	497.634357
500.000000	200.000000	0.000000	0.000000	8.822471	498.308883
500.000000	200.000000	0.000000	0.000000	8.921736	498.790688
500.000000	0.000000	200.000000	0.000000	9.022003	499.465214
500.000000	0.000000	200.000000	0.000000	9.122267	499.625816
500.000000	0.000000	200.000000	0.000000	9.223540	499.304613
500.000000	0.000000	200.000000	0.000000	9.322803	499.754297
500.000000	0.000000	200.000000	0.000000	9.423068	499.465214
500.000000	0.000000	200.000000	0.000000	9.524338	500.460944
500.000000	0.000000	200.000000	0.000000	9.623601	500.043380
500.000000	0.000000	200.000000	0.000000	9.724871	499.979139
500.000000	0.000000	200.000000	0.000000	9.824135	500.043380
500.000000	0.000000	200.000000	0.000000	9.927412	499.593695
500.000000	0.000000	200.000000	0.000000	10.025686	499.465214
500.000000	0.000000	200.000000	0.000000	10.126940	499.818537
500.000000	0.000000	200.000000	0.000000	10.227207	499.529455
500.000000	0.000000	200.000000	0.000000	10.329480	499.272492
500.000000	0.000000	200.000000	0.000000	10.426742	500.011259
500.000000	0.000000	200.000000	0.000000	10.528008	499.947019
500.000000	0.000000	200.000000	0.000000	10.628276	499.336733
500.000000	0.000000	200.000000	0.000000	10.729558	499.850658
500.000000	0.000000	200.000000	0.000000	10.829814	499.690056
500.000000	0.000000	200.000000	0.000000	10.928077	499.176131
500.000000	0.000000	200.000000	0.000000	11.029367	499.786417
500.000000	0.000000	200.000000	0.000000	11.128606	499.947019
500.000000	0.000000	200.000000	0.000000	11.228871	499.368853
500.000000	0.000000	200.000000	0.000000	11.328137	499.593695
500.000000	0.000000	200.000000	0.000000	11.430408	499.465214
500.000000	0.000000	200.000000	0.000000	11.529696	499.979139
500.000000	0.000000	200.000000	0.000000	11.630946	499.400973
500.000000	0.000000	200.000000	0.000000	11.730206	499.272492
500.000000	0.000000	200.000000	0.000000	11.831478	499.433094
500.000000	0.000000	200.000000	0.000000	11.930742	499.465214

500.000000	0.000000	200.000000	0.000000	12.032008	499.561575
500.000000	0.000000	200.000000	0.000000	12.131274	499.914898
500.000000	0.000000	200.000000	0.000000	12.232542	499.593695
500.000000	0.000000	200.000000	0.000000	12.332810	500.396703
500.000000	0.000000	200.000000	0.000000	12.434079	498.983410
500.000000	0.000000	200.000000	0.000000	12.533345	499.914898
500.000000	0.000000	200.000000	0.000000	12.632607	497.827079
500.000000	0.000000	200.000000	0.000000	12.732873	498.662207
500.000000	0.000000	200.000000	0.000000	12.934410	500.075500
500.000000	0.000000	200.000000	0.000000	13.033675	499.015530
500.000000	0.000000	200.000000	0.000000	13.133940	498.887049
500.000000	0.000000	200.000000	0.000000	13.235210	499.272492
500.000000	0.000000	200.000000	0.000000	13.334474	499.336733
500.000000	0.000000	200.000000	0.000000	13.433741	499.079770
500.000000	0.000000	200.000000	0.000000	13.534006	498.822808
500.000000	0.000000	200.000000	0.000000	13.635274	499.529455
500.000000	0.000000	200.000000	0.000000	13.736547	499.786417
500.000000	0.000000	200.000000	0.000000	13.834805	499.208252
500.000000	0.000000	200.000000	0.000000	13.936075	499.947019
500.000000	0.000000	200.000000	0.000000	14.036355	500.493064
500.000000	0.000000	200.000000	0.000000	14.135634	513.212713
500.000000	0.000000	200.000000	0.000000	14.235872	536.917554
500.000000	0.000000	0.000000	200.000000	14.336139	541.928340
500.000000	0.000000	0.000000	200.000000	14.437411	544.851300
500.000000	0.000000	0.000000	200.000000	14.536672	545.782793
500.000000	0.000000	0.000000	200.000000	14.636939	548.063345
500.000000	0.000000	0.000000	200.000000	14.736233	549.797850
500.000000	0.000000	0.000000	200.000000	14.836471	555.290450
500.000000	0.000000	0.000000	200.000000	14.935735	562.035752
500.000000	0.000000	0.000000	200.000000	15.036004	566.725346
500.000000	0.000000	0.000000	200.000000	15.136267	578.642063
500.000000	0.000000	0.000000	200.000000	15.237537	585.130417
500.000000	0.000000	0.000000	200.000000	15.336802	588.117630
500.000000	0.000000	0.000000	200.000000	15.438074	587.732183
500.000000	0.000000	0.000000	200.000000	15.537334	586.929169
500.000000	0.000000	0.000000	200.000000	15.636599	588.310354
500.000000	0.000000	0.000000	200.000000	15.736865	587.796425
500.000000	0.000000	0.000000	200.000000	15.838135	587.828545
500.000000	0.000000	0.000000	200.000000	15.937399	587.635822
500.000000	0.000000	0.000000	200.000000	16.037673	587.443098
500.000000	0.000000	0.000000	200.000000	16.137933	587.314616

500.000000	0.000000	0.000000	200.000000	16.238293	587.346737
500.000000	0.000000	0.000000	200.000000	16.339468	587.346737
500.000000	0.000000	0.000000	200.000000	16.437730	587.218254
500.000000	0.000000	0.000000	200.000000	16.539016	587.475219
500.000000	0.000000	0.000000	200.000000	16.639268	587.443098
500.000000	0.000000	0.000000	200.000000	16.738533	587.346737
500.000000	0.000000	0.000000	200.000000	16.837794	587.250375
500.000000	0.000000	0.000000	200.000000	16.939064	587.378857
500.000000	0.000000	0.000000	200.000000	17.039331	587.154013
500.000000	0.000000	0.000000	200.000000	17.138741	587.218254
500.000000	0.000000	0.000000	200.000000	17.238861	587.218254
500.000000	0.000000	0.000000	200.000000	17.340134	587.218254
500.000000	0.000000	0.000000	200.000000	17.439423	587.314616
500.000000	0.000000	0.000000	200.000000	17.539661	587.410978
500.000000	0.000000	0.000000	200.000000	17.640931	587.282495
500.000000	0.000000	0.000000	200.000000	17.741283	587.410978
500.000000	0.000000	0.000000	200.000000	17.842467	587.314616
500.000000	0.000000	0.000000	200.000000	17.939726	587.378857
500.000000	0.000000	0.000000	200.000000	18.043001	587.282495
500.000000	0.000000	0.000000	200.000000	18.142264	587.282495
500.000000	0.000000	0.000000	200.000000	18.243534	587.314616
500.000000	0.000000	0.000000	200.000000	18.341797	587.346737
500.000000	0.000000	0.000000	200.000000	18.442063	587.314616
500.000000	0.000000	0.000000	200.000000	18.544343	587.314616
500.000000	0.000000	0.000000	200.000000	18.642603	587.282495
500.000000	0.000000	0.000000	200.000000	18.742905	587.314616
500.000000	0.000000	0.000000	200.000000	18.843130	587.410978
500.000000	0.000000	0.000000	200.000000	18.944398	587.410978
500.000000	0.000000	0.000000	200.000000	19.043663	587.475219
500.000000	0.000000	0.000000	200.000000	19.142927	587.378857
500.000000	0.000000	0.000000	200.000000	19.245203	587.314616
500.000000	0.000000	0.000000	200.000000	19.345466	587.250375
500.000000	0.000000	0.000000	200.000000	19.445734	587.378857
500.000000	0.000000	0.000000	200.000000	19.546001	587.282495
500.000000	0.000000	0.000000	200.000000	19.647269	587.218254
500.000000	0.000000	0.000000	200.000000	19.747536	587.314616
500.000000	0.000000	0.000000	200.000000	19.846799	587.282495
500.000000	0.000000	0.000000	200.000000	19.948068	587.282495
500.000000	0.000000	0.000000	200.000000	20.047333	587.218254
500.000000	0.000000	0.000000	200.000000	20.146597	587.250375
500.000000	0.000000	0.000000	200.000000	20.246865	587.282495

500.000000	0.000000	0.000000	200.000000	20.347131	587.218254
500.000000	0.000000	0.000000	200.000000	20.447399	587.250375
500.000000	0.000000	0.000000	200.000000	20.546661	587.314616
500.000000	0.000000	0.000000	200.000000	20.646942	587.443098
500.000000	0.000000	0.000000	200.000000	20.748205	587.186134
500.000000	0.000000	0.000000	200.000000	20.848464	587.282495
500.000000	0.000000	0.000000	200.000000	20.947728	587.218254
500.000000	0.000000	0.000000	200.000000	21.046992	587.314616

Table 5 - Element 3 - 500 Gram Data

5.3.4. *700 Gram Data*

Set Point	Less than	Equal to	Greater than	X Axis	Pot Value
700.000000	200.000000	0.000000	0.000000	0.203626	587.282495
700.000000	200.000000	0.000000	0.000000	0.301827	587.218254
700.000000	200.000000	0.000000	0.000000	0.403073	587.250375
700.000000	200.000000	0.000000	0.000000	0.504344	587.282495
700.000000	200.000000	0.000000	0.000000	0.602605	587.250375
700.000000	200.000000	0.000000	0.000000	0.703874	587.250375
700.000000	200.000000	0.000000	0.000000	0.803137	587.346737
700.000000	200.000000	0.000000	0.000000	0.906412	587.186134
700.000000	200.000000	0.000000	0.000000	1.005684	587.314616
700.000000	200.000000	0.000000	0.000000	1.104972	587.378857
700.000000	200.000000	0.000000	0.000000	1.206211	587.346737
700.000000	200.000000	0.000000	0.000000	1.307481	587.282495
700.000000	200.000000	0.000000	0.000000	1.405741	587.282495
700.000000	200.000000	0.000000	0.000000	1.506009	587.410978
700.000000	200.000000	0.000000	0.000000	1.606275	587.057651
700.000000	200.000000	0.000000	0.000000	1.706542	587.218254
700.000000	200.000000	0.000000	0.000000	1.807814	587.410978
700.000000	200.000000	0.000000	0.000000	1.907073	587.667942
700.000000	200.000000	0.000000	0.000000	2.009348	587.764304
700.000000	200.000000	0.000000	0.000000	2.107628	587.314616
700.000000	200.000000	0.000000	0.000000	2.207875	587.635822
700.000000	200.000000	0.000000	0.000000	2.307141	587.667942
700.000000	200.000000	0.000000	0.000000	2.407405	587.314616
700.000000	200.000000	0.000000	0.000000	2.507674	587.218254
700.000000	200.000000	0.000000	0.000000	2.606936	587.571581
700.000000	200.000000	0.000000	0.000000	2.708206	587.250375
700.000000	200.000000	0.000000	0.000000	2.807469	587.378857
700.000000	200.000000	0.000000	0.000000	2.907737	587.507339
700.000000	200.000000	0.000000	0.000000	3.007000	586.993410
700.000000	200.000000	0.000000	0.000000	3.108270	587.828545
700.000000	200.000000	0.000000	0.000000	3.209551	587.507339
700.000000	200.000000	0.000000	0.000000	3.307801	586.897048
700.000000	200.000000	0.000000	0.000000	3.408094	587.218254
700.000000	200.000000	0.000000	0.000000	3.509509	587.250375
700.000000	200.000000	0.000000	0.000000	3.608601	587.186134
700.000000	200.000000	0.000000	0.000000	3.708869	587.218254
700.000000	200.000000	0.000000	0.000000	3.810141	586.897048
700.000000	200.000000	0.000000	0.000000	3.910406	587.282495

700.000000	200.000000	0.000000	0.000000	4.009669	587.346737
700.000000	200.000000	0.000000	0.000000	4.110938	586.961290
700.000000	200.000000	0.000000	0.000000	4.211205	587.796425
700.000000	200.000000	0.000000	0.000000	4.312474	586.672204
700.000000	200.000000	0.000000	0.000000	4.410822	586.768566
700.000000	200.000000	0.000000	0.000000	4.513007	586.961290
700.000000	200.000000	0.000000	0.000000	4.613279	586.864928
700.000000	200.000000	0.000000	0.000000	4.714547	586.736445
700.000000	200.000000	0.000000	0.000000	4.814928	586.993410
700.000000	200.000000	0.000000	0.000000	4.914074	586.800687
700.000000	200.000000	0.000000	0.000000	5.016351	587.346737
700.000000	200.000000	0.000000	0.000000	5.115620	586.929169
700.000000	200.000000	0.000000	0.000000	5.214874	587.218254
700.000000	200.000000	0.000000	0.000000	5.317147	587.571581
700.000000	200.000000	0.000000	0.000000	5.416410	587.282495
700.000000	200.000000	0.000000	0.000000	5.515675	586.832807
700.000000	200.000000	0.000000	0.000000	5.616946	587.443098
700.000000	200.000000	0.000000	0.000000	5.717210	587.539460
700.000000	200.000000	0.000000	0.000000	5.818541	586.447360
700.000000	200.000000	0.000000	0.000000	5.917744	586.768566
700.000000	200.000000	0.000000	0.000000	6.018011	587.282495
700.000000	200.000000	0.000000	0.000000	6.119281	587.314616
700.000000	200.000000	0.000000	0.000000	6.220553	586.736445
700.000000	200.000000	0.000000	0.000000	6.318811	586.993410
700.000000	200.000000	0.000000	0.000000	6.418075	586.961290
700.000000	200.000000	0.000000	0.000000	6.520351	587.924907
700.000000	200.000000	0.000000	0.000000	6.619611	587.764304
700.000000	200.000000	0.000000	0.000000	6.720004	587.732183
700.000000	200.000000	0.000000	0.000000	6.820250	588.278233
700.000000	200.000000	0.000000	0.000000	6.921415	587.989148
700.000000	200.000000	0.000000	0.000000	7.019703	588.342475
700.000000	200.000000	0.000000	0.000000	7.120947	588.149751
700.000000	200.000000	0.000000	0.000000	7.221213	589.113369
700.000000	200.000000	0.000000	0.000000	7.322482	592.325428
700.000000	200.000000	0.000000	0.000000	7.421749	604.017332
700.000000	200.000000	0.000000	0.000000	7.521009	613.300201
700.000000	200.000000	0.000000	0.000000	7.623285	613.557167
700.000000	200.000000	0.000000	0.000000	7.723594	614.199580
700.000000	200.000000	0.000000	0.000000	7.822813	614.263821
700.000000	200.000000	0.000000	0.000000	7.924094	613.525046
700.000000	200.000000	0.000000	0.000000	8.023345	615.869855

700.000000	200.000000	0.000000	0.000000	8.124617	620.784320
700.000000	200.000000	0.000000	0.000000	8.223879	624.606683
700.000000	200.000000	0.000000	0.000000	8.323144	628.621773
700.000000	200.000000	0.000000	0.000000	8.424440	634.242901
700.000000	200.000000	0.000000	0.000000	8.523677	638.482840
700.000000	200.000000	0.000000	0.000000	8.625949	642.690660
700.000000	200.000000	0.000000	0.000000	8.724211	643.333076
700.000000	200.000000	0.000000	0.000000	8.824478	646.384550
700.000000	200.000000	0.000000	0.000000	8.924744	650.688736
700.000000	200.000000	0.000000	0.000000	9.024010	653.419004
700.000000	200.000000	0.000000	0.000000	9.125281	655.956549
700.000000	200.000000	0.000000	0.000000	9.224544	658.975906
700.000000	200.000000	0.000000	0.000000	9.323806	661.866782
700.000000	200.000000	0.000000	0.000000	9.424073	664.147362
700.000000	200.000000	0.000000	0.000000	9.525342	665.881888
700.000000	200.000000	0.000000	0.000000	9.624609	668.258831
700.000000	200.000000	0.000000	0.000000	9.725878	672.306061
700.000000	200.000000	0.000000	0.000000	9.825153	673.719380
700.000000	200.000000	0.000000	0.000000	9.927413	677.156315
700.000000	200.000000	0.000000	0.000000	10.027679	678.730240
700.000000	200.000000	0.000000	0.000000	10.127947	683.837465
700.000000	200.000000	0.000000	0.000000	10.229214	684.576246
700.000000	200.000000	0.000000	0.000000	10.329483	684.961697
700.000000	200.000000	0.000000	0.000000	10.427743	686.182292
700.000000	200.000000	0.000000	0.000000	10.528011	688.495000
700.000000	200.000000	0.000000	0.000000	10.628277	689.908321
700.000000	200.000000	0.000000	0.000000	10.729554	691.385885
700.000000	200.000000	0.000000	0.000000	10.827808	691.353764
700.000000	200.000000	0.000000	0.000000	10.932088	690.807708
700.000000	200.000000	0.000000	0.000000	11.030349	692.124667
700.000000	200.000000	0.000000	0.000000	11.131659	691.450127
700.000000	200.000000	0.000000	0.000000	11.231888	691.418006
700.000000	200.000000	0.000000	0.000000	11.332149	691.257401
700.000000	200.000000	0.000000	0.000000	11.432415	691.931941
700.000000	200.000000	0.000000	0.000000	11.531680	691.899820
700.000000	200.000000	0.000000	0.000000	11.631947	692.413755
700.000000	200.000000	0.000000	0.000000	11.733216	691.835578
700.000000	200.000000	0.000000	0.000000	11.832484	691.578611
700.000000	200.000000	0.000000	0.000000	11.932750	693.248900
700.000000	200.000000	0.000000	0.000000	12.032011	695.433126
700.000000	200.000000	0.000000	0.000000	12.132277	695.947061

700.000000	200.000000	0.000000	0.000000	12.233558	696.685844
700.000000	200.000000	0.000000	0.000000	12.333814	696.589481
700.000000	200.000000	0.000000	0.000000	12.433078	696.782206
700.000000	200.000000	0.000000	0.000000	12.534347	696.814327
700.000000	200.000000	0.000000	0.000000	12.634614	697.007053
700.000000	200.000000	0.000000	0.000000	12.733878	696.750085
700.000000	200.000000	0.000000	0.000000	12.836277	697.167658
700.000000	200.000000	0.000000	0.000000	12.935414	697.424626
700.000000	200.000000	0.000000	0.000000	13.034680	697.617352
700.000000	0.000000	200.000000	0.000000	13.334476	697.970682
700.000000	0.000000	200.000000	0.000000	13.536015	698.291892
700.000000	0.000000	200.000000	0.000000	13.635280	697.874320
700.000000	0.000000	200.000000	0.000000	13.736667	698.002803
700.000000	0.000000	200.000000	0.000000	13.835810	699.127038
700.000000	0.000000	200.000000	0.000000	13.936090	699.994304
700.000000	0.000000	200.000000	0.000000	14.038390	699.544610
700.000000	0.000000	200.000000	0.000000	14.136611	699.930062
700.000000	0.000000	200.000000	0.000000	14.237879	699.287643
700.000000	0.000000	200.000000	0.000000	14.336226	699.319764
700.000000	0.000000	200.000000	0.000000	14.438414	699.512489
700.000000	0.000000	200.000000	0.000000	14.535671	700.026425
700.000000	0.000000	200.000000	0.000000	14.636943	699.351885
700.000000	0.000000	200.000000	0.000000	14.739213	699.448247
700.000000	0.000000	200.000000	0.000000	14.839481	699.191280
700.000000	0.000000	200.000000	0.000000	14.939747	699.480368
700.000000	0.000000	200.000000	0.000000	15.040014	699.255522
700.000000	0.000000	200.000000	0.000000	15.140281	699.769457
700.000000	0.000000	200.000000	0.000000	15.241553	699.544610
700.000000	0.000000	200.000000	0.000000	15.339811	699.801578
700.000000	0.000000	200.000000	0.000000	15.441195	699.865820
700.000000	0.000000	200.000000	0.000000	15.541370	699.833699
700.000000	0.000000	200.000000	0.000000	15.642632	699.255522
700.000000	0.000000	200.000000	0.000000	15.742883	699.191280
700.000000	0.000000	200.000000	0.000000	15.845156	700.572482
700.000000	0.000000	200.000000	0.000000	15.944420	699.544610
700.000000	0.000000	200.000000	0.000000	16.044686	699.833699
700.000000	0.000000	200.000000	0.000000	16.143950	699.962183
700.000000	0.000000	200.000000	0.000000	16.245243	699.287643
700.000000	0.000000	200.000000	0.000000	16.345490	699.897941
700.000000	0.000000	200.000000	0.000000	16.444753	699.737336
700.000000	0.000000	200.000000	0.000000	16.547023	699.512489

700.000000	0.000000	200.000000	0.000000	16.645284	699.255522
700.000000	0.000000	200.000000	0.000000	16.747557	699.127038
700.000000	0.000000	200.000000	0.000000	16.846820	699.351885
700.000000	0.000000	200.000000	0.000000	16.948090	699.576731
700.000000	0.000000	200.000000	0.000000	17.048357	699.159159
700.000000	0.000000	200.000000	0.000000	17.146667	699.255522
700.000000	0.000000	200.000000	0.000000	17.247888	699.673094
700.000000	0.000000	200.000000	0.000000	17.348155	699.319764
700.000000	0.000000	200.000000	0.000000	17.448420	699.191280
700.000000	0.000000	200.000000	0.000000	17.548688	700.315514
700.000000	0.000000	200.000000	0.000000	17.647953	699.416127
700.000000	0.000000	200.000000	0.000000	17.750224	699.512489
700.000000	0.000000	200.000000	0.000000	17.849513	698.484618
700.000000	0.000000	200.000000	0.000000	17.949757	699.416127
700.000000	0.000000	200.000000	0.000000	18.050022	699.448247
700.000000	0.000000	200.000000	0.000000	18.151291	699.319764
700.000000	0.000000	200.000000	0.000000	18.251562	699.769457
700.000000	0.000000	200.000000	0.000000	18.350822	699.769457
700.000000	0.000000	200.000000	0.000000	18.453094	699.384006
700.000000	0.000000	200.000000	0.000000	18.551355	699.062796
700.000000	0.000000	200.000000	0.000000	18.652625	699.480368
700.000000	0.000000	200.000000	0.000000	18.750888	699.223401
700.000000	0.000000	200.000000	0.000000	18.852157	699.159159
700.000000	0.000000	200.000000	0.000000	18.953435	699.319764
700.000000	0.000000	200.000000	0.000000	19.052691	699.705215
700.000000	0.000000	200.000000	0.000000	19.153958	699.351885
700.000000	0.000000	200.000000	0.000000	19.253227	699.384006
700.000000	0.000000	200.000000	0.000000	19.353489	699.384006
700.000000	0.000000	200.000000	0.000000	19.452782	699.191280
700.000000	0.000000	200.000000	0.000000	19.553061	699.705215
700.000000	0.000000	200.000000	0.000000	19.653320	699.094917
700.000000	0.000000	200.000000	0.000000	19.755560	698.998554
700.000000	0.000000	200.000000	0.000000	19.852818	699.480368
700.000000	0.000000	200.000000	0.000000	19.953084	698.966433
700.000000	0.000000	200.000000	0.000000	20.054353	699.930062
700.000000	0.000000	200.000000	0.000000	20.154622	699.191280
700.000000	0.000000	200.000000	0.000000	20.254889	700.026425
700.000000	0.000000	200.000000	0.000000	20.354151	698.934312
700.000000	0.000000	200.000000	0.000000	20.455421	700.187030
700.000000	0.000000	200.000000	0.000000	20.553683	699.865820
700.000000	0.000000	200.000000	0.000000	20.653949	699.416127

700.000000	0.000000	200.000000	0.000000	20.753234	699.384006
700.000000	0.000000	200.000000	0.000000	20.855525	699.351885
700.000000	0.000000	200.000000	0.000000	20.954751	700.026425
700.000000	0.000000	200.000000	0.000000	21.057022	700.283393
700.000000	0.000000	0.000000	200.000000	21.155282	702.467620
700.000000	0.000000	0.000000	200.000000	21.256563	714.769970
700.000000	0.000000	0.000000	200.000000	21.355817	723.442655
700.000000	0.000000	0.000000	200.000000	21.457090	726.108705
700.000000	0.000000	0.000000	200.000000	21.558354	730.766264
700.000000	0.000000	0.000000	200.000000	21.657758	734.106859
700.000000	0.000000	0.000000	200.000000	21.757889	744.289259
700.000000	0.000000	0.000000	200.000000	21.859155	756.559551
700.000000	0.000000	0.000000	200.000000	21.960424	773.519566
700.000000	0.000000	0.000000	200.000000	22.060778	789.162643
700.000000	0.000000	0.000000	200.000000	22.161990	802.075433
700.000000	0.000000	0.000000	200.000000	22.262233	805.223330
700.000000	0.000000	0.000000	200.000000	22.361493	806.765158
700.000000	0.000000	0.000000	200.000000	22.461758	814.024601
700.000000	0.000000	0.000000	200.000000	22.561021	831.081109
700.000000	0.000000	0.000000	200.000000	22.662291	852.988019
700.000000	0.000000	0.000000	200.000000	22.762561	865.001513
700.000000	0.000000	0.000000	200.000000	22.860820	866.928814
700.000000	0.000000	0.000000	200.000000	22.962098	866.928814
700.000000	0.000000	0.000000	200.000000	23.062357	867.057301
700.000000	0.000000	0.000000	200.000000	23.160617	866.607597
700.000000	0.000000	0.000000	200.000000	23.261889	867.378517
700.000000	0.000000	0.000000	200.000000	23.361150	866.318502
700.000000	0.000000	0.000000	200.000000	23.462505	866.671840
700.000000	0.000000	0.000000	200.000000	23.561684	866.029407
700.000000	0.000000	0.000000	200.000000	23.663960	866.414867
700.000000	0.000000	0.000000	200.000000	23.763221	866.125772
700.000000	0.000000	0.000000	200.000000	23.864504	866.318502
700.000000	0.000000	0.000000	200.000000	23.962761	866.768205
700.000000	0.000000	0.000000	200.000000	24.063017	866.768205
700.000000	0.000000	0.000000	200.000000	24.164290	866.736084
700.000000	0.000000	0.000000	200.000000	24.264555	866.639719
700.000000	0.000000	0.000000	200.000000	24.363818	866.382745
700.000000	0.000000	0.000000	200.000000	24.466090	866.382745
700.000000	0.000000	0.000000	200.000000	24.566361	866.543354
700.000000	0.000000	0.000000	200.000000	24.665624	866.607597
700.000000	0.000000	0.000000	200.000000	24.765932	866.607597

700.000000	0.000000	0.000000	200.000000	24.865152	866.736084
700.000000	0.000000	0.000000	200.000000	24.967428	866.671840
700.000000	0.000000	0.000000	200.000000	25.065773	866.511232
700.000000	0.000000	0.000000	200.000000	25.168965	866.671840
700.000000	0.000000	0.000000	200.000000	25.267234	866.511232
700.000000	0.000000	0.000000	200.000000	25.368492	866.511232
700.000000	0.000000	0.000000	200.000000	25.466753	866.511232
700.000000	0.000000	0.000000	200.000000	25.570167	866.479110
700.000000	0.000000	0.000000	200.000000	25.668313	866.575475
700.000000	0.000000	0.000000	200.000000	25.770562	866.607597
700.000000	0.000000	0.000000	200.000000	25.870828	866.446989
700.000000	0.000000	0.000000	200.000000	25.971124	866.511232
700.000000	0.000000	0.000000	200.000000	26.071389	866.607597
700.000000	0.000000	0.000000	200.000000	26.170640	866.543354

Table 6 - Element 3 - 700 Gram Data

Good set of sample raw data from text files

1809810

GRADEMARK REPORT

FINAL GRADE

76/100

GENERAL COMMENTS

Instructor

PAGE 1

PAGE 2

PAGE 3

PAGE 4

Text Comment. Good table of contents with good level of detail

PAGE 5

PAGE 6

PAGE 7

Text Comment. Table of figures is extensive and in good order

PAGE 8

Text Comment. Good use of tables

PAGE 9

Text Comment. Good use of tables

PAGE 10

Text Comment. Good summary

PAGE 11

PAGE 12

PAGE 13

Text Comment. A good explanation of the LabVIEW design with the DAQ interface blocks identified

PAGE 14

PAGE 15

Text Comment. Explained very well and shows a good understanding which is crucial to this element

PAGE 16

Text Comment. Coverage is good on this and the IP design method has been identified

PAGE 17

PAGE 18

Text Comment. Explanation is very good supported with good images

PAGE 19

Text Comment. Good work here which demonstrates your knowledge of the methods

PAGE 20

Text Comment. Explanation is good and all the research in this section is supported significantly with relevant sources

PAGE 21

PAGE 22

PAGE 23

Text Comment. Excellent work. The 4 bit adder hierarchy and inheritance has been identified and explained very well. All the components are explained.

PAGE 24

Text Comment. Good work and the code looks very neat and tidy

PAGE 25

Text Comment. IP integration is demonstrated and backed up with a good explanation.

PAGE 26

Text Comment. This is a 4 bit adder and 4 bit comparator

Text Comment. Good source design image showing no errors and IP design created

Text Comment. This is a 4 bit adder and 4 bit comp

Text Comment. Error here: should be 4 bit hierarchy

Text Comment. This cct should have a heading '8 bit Mag Comparator'

Text Comment. Good explanation here which offers a different method of SOC design for simpler circuits

PAGE 27

Text Comment. Good work and good use of the virtual bus to display results.

PAGE 28

Text Comment. Good example of test data

Text Comment. Good work here and good test data used to get all 3 results. You have also identified the static variable links from the Sim circuit.

PAGE 29

PAGE 30

Text Comment. Excellent work with the table of values indicating the settings on the FPGA board. Good test carried out

PAGE 31

Text Comment. Very good test result

PAGE 32

Text Comment. A full set of good test results

PAGE 33

Text Comment. Good circuit design

PAGE 34

PAGE 35

PAGE 36

Text Comment. Very good set of results

PAGE 37

Text Comment. Very good evaluation of the element

PAGE 38

Text Comment. Good introduction

PAGE 39

Text Comment. Good example which indicates a good understanding of op amps

PAGE 40

Text Comment. Good result and explanation

PAGE 41

Text Comment. Good work

Text Comment. The required gain is achieved and explained

PAGE 42

Text Comment. Good explanation

PAGE 43

Text Comment. Good explanation for 10 bit ADC

PAGE 44

Text Comment. Good example of front pane view for 10 bit ADC

Text Comment. Good explanation of 12 bit ADC

PAGE 45

Text Comment. Good front panel example of 12 bit ADC

PAGE 46

PAGE 47

Text Comment. Good design of 8 bit ADC

PAGE 48

Text Comment. The block achieves this by multiplying the 8 bit value by 256. The lower 8 spaces are then used to add the set point value

PAGE 49

Text Comment. Front panel view is good

Text Comment. Good explanation

Text Comment. PLD design is good

PAGE 50

Text Comment. FPGA ports are identified here

PAGE 51

PAGE 52

Text Comment. Good table of results

PAGE 53

Text Comment. Linear graph is correct

PAGE 54

Text Comment. 10 bit ADC tests are good

PAGE 55

Text Comment. 12 bit ADC tests are good

PAGE 56

Text Comment. DAQ board output result is good

PAGE 57

Text Comment. Good results

PAGE 58

Text Comment. Good clear image of equipment setup

PAGE 59

PAGE 60

PAGE 61

Text Comment. Very good set of results

PAGE 62

Text Comment. Evaluation i good

PAGE 63

Text Comment. Good introduction

PAGE 64

Text Comment. LabVIEW G-code is correct

PAGE 65

Text Comment. LabVIEW front panel view is a good design

PAGE 66

Text Comment. Good explanation

PAGE 67

Text Comment. Good test result

PAGE 68

Text Comment. Good graph of results

PAGE 69

Text Comment. Good result

PAGE 70

Text Comment. Good resultant graph

PAGE 71

Text Comment. Good result

PAGE 72

Text Comment. Good resultant graph

PAGE 73

Text Comment. Good evaluation

PAGE 74

PAGE 75

PAGE 76

Text Comment. An extensive reference list

PAGE 77

PAGE 78

PAGE 79

PAGE 80

PAGE 81

Text Comment. Good set of results for load cell and instrumentation amplifier

PAGE 82

PAGE 83

PAGE 84

Text Comment. Text file configuration

PAGE 85

PAGE 86

PAGE 87

Text Comment. Very good set of results

PAGE 88

PAGE 89

PAGE 90

PAGE 91

PAGE 92

PAGE 93

PAGE 94

PAGE 95

PAGE 96

PAGE 97

PAGE 98

PAGE 99

PAGE 100

PAGE 101

PAGE 102

PAGE 103

PAGE 104

PAGE 105

Text Comment. Good set of sample raw data from text files

GRADING FORM: CSG-RUBIC

DAVID THOMAS	**0**

RESEARCH-INFORMED LITERATURE

Research section has covered all requirements in good detail. Good relevant sources used. **8/10**

KNOWLEDGE AND UNDERSTANDING

E1-Design and use of magnitude comparator with digital inputs has been created with good explanations. There are some minor errors / confusions with headings. Test methods used are good and followed a logical sequence. 7.5/10 E2-The LabVIEW design for the analogue load cell input is explained and the design is a good effort. The 16 bit word operation for the fpga is partly explained. The shift right and add parts are missing and this is the key to how the data bits are organised for the fpga. The design is operational but needs to be explained further. 6.5/10 E3-Dat **22/30**

logging has ben fully explained and a good knowledge of this section is demonstrated. 8/10

ANALYSIS

E1-Test and results are very comprehensive . The evaluation covers the main issues. 3.5/5 E2-The results from LabVIEW are comprehensive and detailed. The evaluation is good. 7/10 E3-Results from the data logging section are very detailed and a good evaluation for this section. 8.5/10

19/25

PRACTICAL APPLICATION AND DEP.

E1-Prototypes for the comparator have been designed using logical methods. PLD design methods used were successfully implemented using the fpga dev board. 3.5/5 E2-Design and build of LabVIEW interface for fpga followed a good development sequence. The development sections were tested at designated stages to prove design. The data was shifted right and added successfully. 3.5/5 E3-Data logging using LabVIEW methods has ben designed and tested for operational requirements. 8/10

15/20

SKILLS FOR PROFESSIONAL PRAC.

A very good report with a good easy to follow structure

12/15