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University of Wales
Trinity Saint David

Complete, fold and seal
(see note 2 below)

SURNAME: PATEY

FORENAME(S): ROWAN

Examination Answer Books

12 Pages

Instructions to Candidates

1. Please give the information requested in the boxes below.
2. Enter your name in the space provided to the right, fold over and seal down (using the label provided) to hide your name.
3. The answers must be legibly written. The Examiners will not accept illegible script or have it typed and the expense of typing charged to the candidate.
4. Write your answers in ink.
5. Begin each answer on a fresh page. Do all rough work in the answer book and cross it through.
6. No part of this book is to be torn out; it must be handed in complete.
7. If more books than one are used, fasten them together using the tags available from the invigilator(s).
8. Every book must be handed in. In no circumstances may answer books, used or unused, be taken out of the examination venue.

1	Student Number	2317629
2	Title of Examination Paper	Mico, phrifodol a d. I. I. I.
3	Module Code	ACDA4004
4	Date and Time of Examination	08.01.24 At 09:00
5	Examination Venue	IA campus
6	Seat Number	022
7	Number of Answer Books handed in	

List the numbers of the questions you have attempted	Office Use
1	9
2	9
3	3
4	7
5	10
6	5
	43
	x 2
Total	86%

4
9
3
7
10
5

43

*1 Then saving the TOS to the PC.

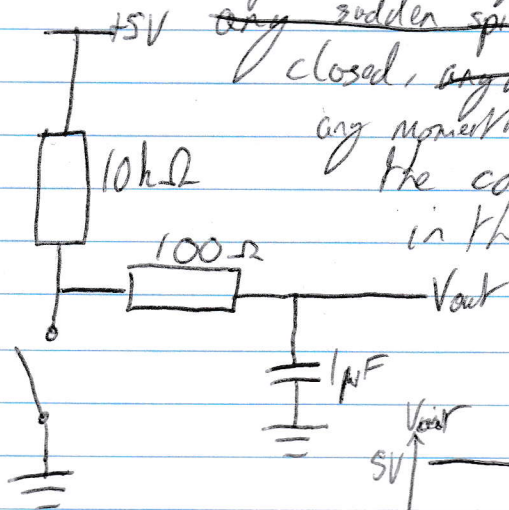
- 1a. RETURN = Return to subroutine
 = To return to the subroutine saved to the stack by POPing it. *1
 and taking the 11 bit address from the TOS. 2
- b. SLEEP = ~~Standby mode~~
 = ~~Save current program~~ Using PLATH high byte. 2
- SLEEP = Shutdown set, a standby low power mode. 2
- c. ADDLW = ~~Add W register contents with literal k~~ then save to 2
 = Add, literal W register *2 8 bit W register. 2
- d. BCF j, b = Bit clear
 = Clear bit 'b' in the j register 2
- e. DECF = Decrement j register
 = Decrement the contents of j register. If the 'b' bit is now 0, save the result to W register. If 'b' bit is now set (1) then save to the j register. 2

*2 Add W register contents with 8 bit literal 'k', then save to the W register.

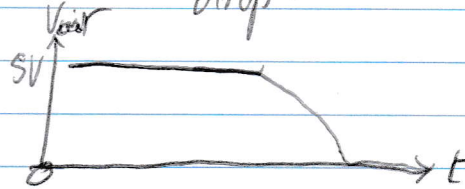
9

2. Method 1: RC implementation

Adding an RC component around a switch before the input will help to smooth out the output voltage. It acts as a rudimentary low pass filter where the noise will be reduced when the switch bounces against the internal contact, causing fluctuations in the output voltage. The smoothing occurs due to the slow discharge of the capacitor, meaning when the switch is dropped,

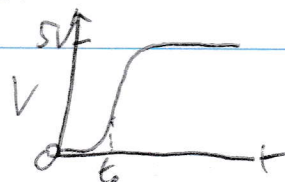
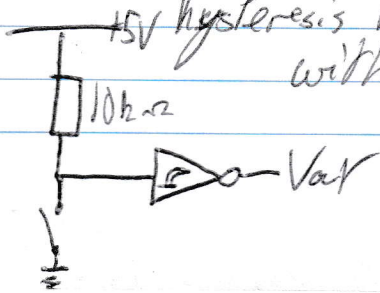


any sudden spike of voltage output and closed, any sudden drop of voltage output (causing a momentary change of the switch hitting the contact will not be clear in the V_{out} amplitude, where the capacitor will slowly discharge causing a smooth voltage drop.



Schmitt Inverter

Common to many logic gates and ICs are schmitt inverters, special buffers that change the threshold voltage values in such a manner that when the voltage is set high, the input voltage must drop significantly lower than prior, to cause the logic state to switch. As such it 'holds the line high' through smaller fluctuations like switched fence. The same holds true for the opposite, where the threshold to raise the line high from low is much increased, holding the line low. This is a hysteresis trigger. This produces a clean singular signal with all bounce noise removed.



3



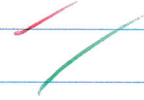
A	B	Q
0	0	0
0	1	0
1	0	0
1	1	1

3

3

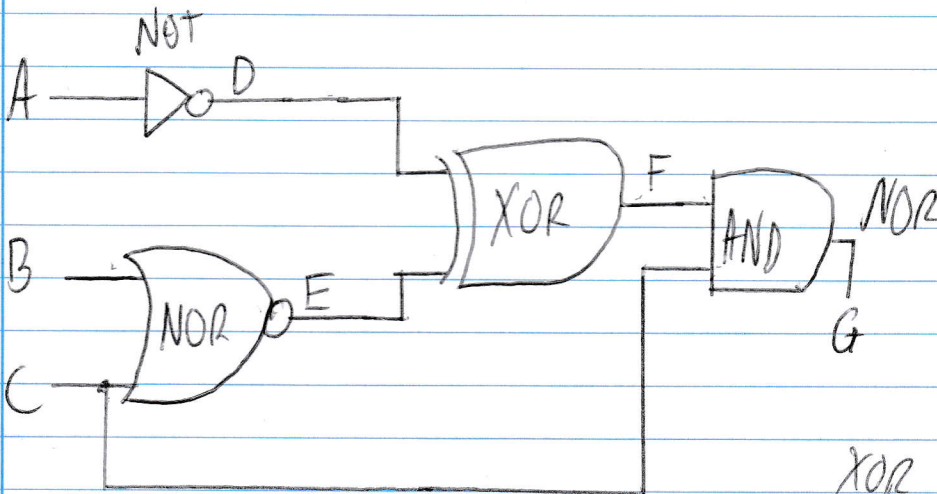
1/4

A	B	C	D	E	F	G
0	0	0	1	1	0	0
0	0	1	1	0	1	1
0	1	0	1	0	1	0
0	1	1	1	0	1	1
1	0	0	0	1	1	0
1	0	1	0	0	0	0
1	1	0	0	0	0	0
1	1	1	0	0	0	0



7

7



OR

B	C	Q
0	0	0
0	1	1
1	0	1
1	1	1

NOR

B	C	Q
0	0	1
0	1	0
1	0	0
1	1	0

XOR

B	C	Q
0	0	0
0	1	1
1	0	1
1	1	0

B	C	A	E	D	F	G
0	0	0	1	1	0	0
0	0	1	1	0	1	0
0	1	0	0	1	1	1
0	1	1	0	0	0	0
1	0	0	0	1	1	0
1	0	1	0	0	0	0
1	1	0	0	1	1	1
1	1	1	0	0	0	0

b

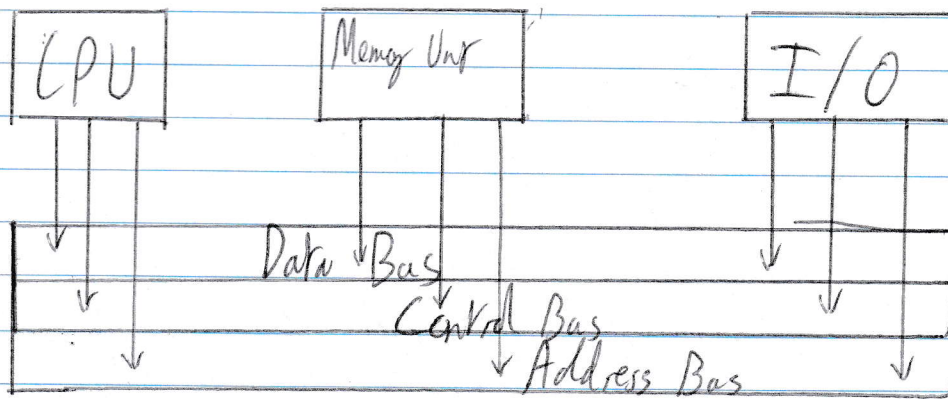
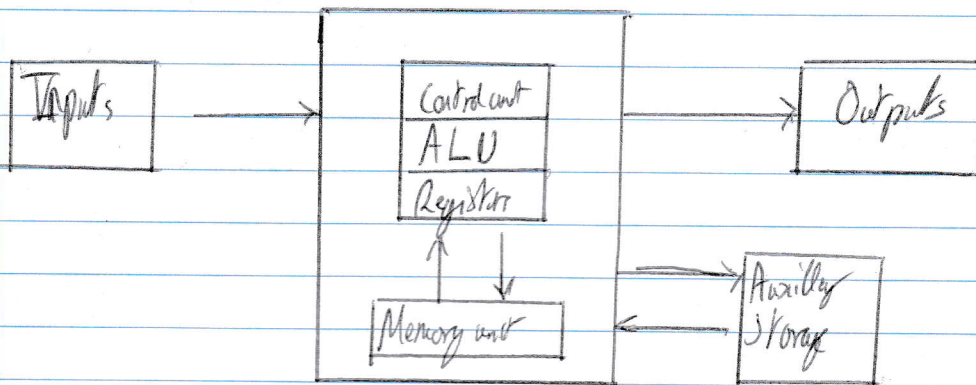
~~the~~	A	B	C	G
	0	0	0	0
	0	0	1	1
	0	1	0	0
	0	1	1	1
	1	0	0	0
	1	0	1	0
	1	1	0	0
	1	1	1	0

A $\rightarrow$ ~~DO~~

B	C	NOR	XOR	OR	AND
0	0	1	0	0	0
0	1	0	1	1	0
1	0	0	1	1	0
1	1	0	0	1	1
0	0	1	0	0	0
0	1	0	1	1	0
1	0	0	1	1	0
1	1	0	0	1	1

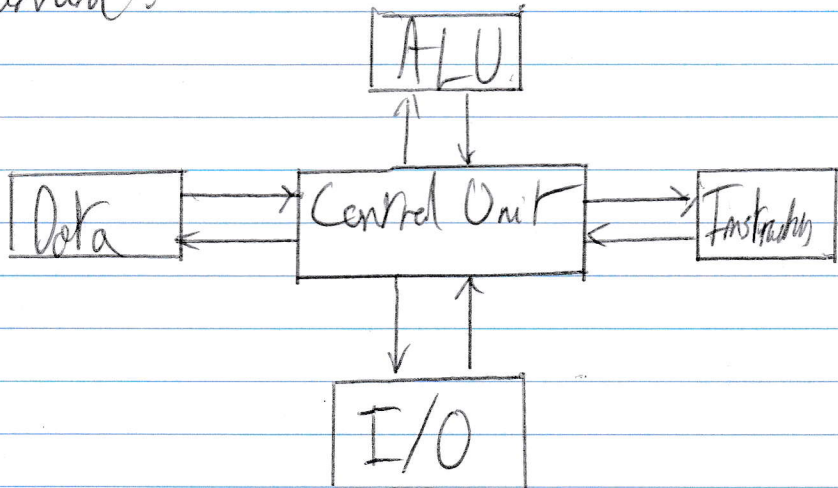
$\overline{A} \times C$

5 Von Neumann



Von Neuman architecture allows for more efficient use of memory, where the memory unit can be overwritten with other data or instructions, compared to Harvard architecture where data and instructions do not share the same physical memory address. The single bus shared throughout these systems also lowers complexity and design costs compared to Harvard systems.

Harvard:



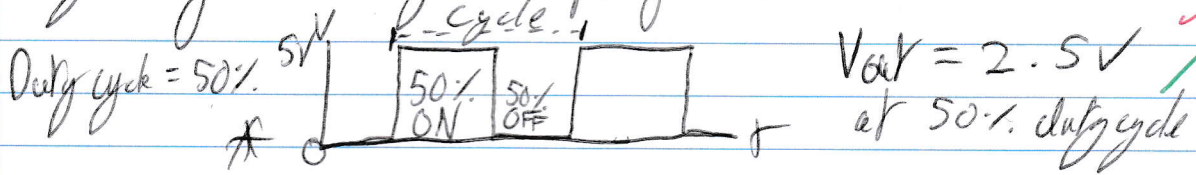
Harvard architecture systems are able to leverage their two separate Data and instruction buses to simultaneously process both in a single processing cycle. This allows Harvard systems to parallel processes compared to VN systems that must sequentially run through the fetch-execute cycle every clock cycle. Harvard systems are also less likely to suffer data corruptions given their two crucial data and instructions memory stores are separated, making the likelihood of accidental overwrites on crucial memory locations much more difficult.

10

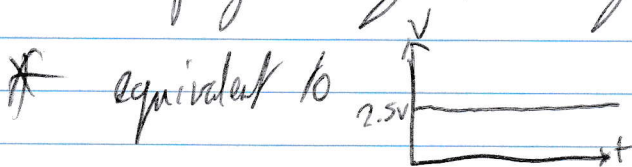
10

6. The DAC requires a

A PWM signal is a method of producing a faux analogue signal from a digital output pin.



By modulating the width of each pulse, changing the ratio of high to low each signal cycle undergoes, the average voltage amplitude output can be modified with a range of granularity. Therefore despite being a digital signal that can only be on or off, high or low (1 or 0), the width modulated signal can be modified by changing the duty cycle to output a range of voltages from 0V to 5V. To then achieve a DAC, the resolution must be determined. The resolution of a DAC is determined by its bit depth, 2^n where n = the number of input bits. Therefore the resolution of the output pin is defined by the N -bit counter that determines the number of pulse widths possible. For example, a 16-bit counter would have 2^{16} possible states for the duty cycle and as such 2^{16} steps for creating an analogue signal. The number



Smoothing?