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by Jordan Rees

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1. Executive summary

This assignment covered the manufacturing process and testing of ICs. The research covered the fabrication faults that can occur on ICs and how stuck at fault modelling can be used to test the functionality of ICs. It then covered the methods used to manufacture a sustainable product such as machine vision, frequency signature analysis and in circuit testing. Also, the effects of electrostatic discharge on ICs was covered and how it can damage ICs and also how to prevent ESD from occurring.

Tasks were then carried out by designing an IC by using Karnaugh maps and truth tables to produce the inputs and outputs of the logic gates. A stuck at fault modelling technique was used to then test the IC which was simulated on multisim and tested practically using a NI Elvis board. These results were then compared and analysed to prove that the circuit was working correctly and prove that the theory is correct. Due to the results being successful a PCB was designed using a CAM software which was converted into Gerber files to be sent away and built into a PCB. This was then further tested to prove functionality.

There were many things learnt in this assignment such as how ICs work how they are built, designed and tested. The issues ICs have while being manufactured and the effects of ESD on ICs and the prevention methods. Also, methods to produce a sustainable product.

Summary indicates an understanding of the requirements

2. Research

2.1 Integrated circuit fabrication faults

When integrated circuits are manufactured there can be small defects in the integrated circuits (IC) when they are being produced. These manufacturing defects get more severe the bigger and denser the chip is. This can cause built in faults in the chips. (Koren, 1998)

"Figure 1" shows the failure rate of IC faults.

Good significant point made here

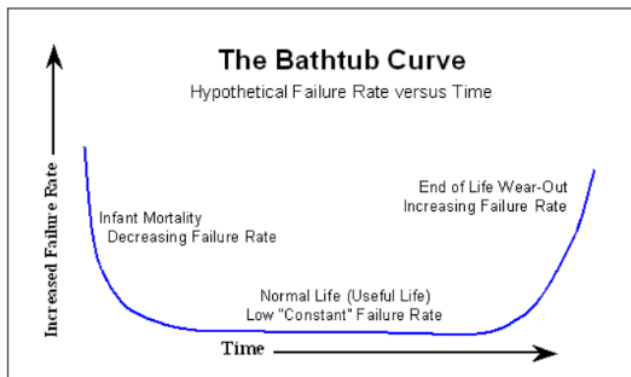


Figure 1: IC faults graph

(Wilkins, 2022)

"Figure 1" shows the failure rate of ICs. This follows a bathtub curve where the failure rate is large at the early stages of the ICs this is due to the manufacturing defects where the ICs will fail usually within 1 to 20 weeks. After this the failure rate will drop and the ICs will have a low consistent failure rate this will usually last 10 to 20 years. The failure rate then increases this is due to the ICs starting to wear due to there long lifespan. To prevent ICs being released with defects fault detection tests are done so that the ICs can surpass that 1 to 20 week failure. (Wilkins, 2022)

An interesting fact supported by an image and ref source

Below are the IC fabricated fault categories that occur.

Gate level stuck at fault: This occurs when an input of a logic gate is stuck at either 0 or 1. This will have an effect on the output of the device.

Transistor level stuck at fault: This fault is when the transistor switch is either stuck open or closed.

Delay fault: This fault is when there is a resistive short/open circuit. This causes the signal to propagate slowly. This can cause the signal to not meet the specified time limit. This can occur when there is manufacturing defects in the circuit.

Bridging fault: This is when there's a short between the connections or components in the circuit. Open circuit fault can act like a line-stuck at faults.

There are three issues that can cause a single stuck at fault these are; One line or wire is faulty, the line with a fault is set to zero or one permanently, and the fault can be either in the input or output.

Good explanation of fault types

(Mohammadat, 2015) (fall, 2002)

Below is an example of a stuck and 0 and stuck at 1 fault and compared against a working AND gate. "Figure 2 shows a working AND gate".

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1



Figure 2: Working AND gate and truth table

"Figure 3" shows stuck at 1 fault where the input "A" are stuck at logic 1 this causes the AND gate to produce 2 outputs instead of 1 as shown in the truth table.

A	B	Y
1	0	0
1	1	1
1	0	0
1	1	1



Figure 3: SA1 and gate and truth table

"Figure 4" shows the stuck at 0 fault where the input "A" is stuck at logic 0 this causes the AND gate to always produce an output 0. This is shown in the truth table.

A	B	Y
0	1	0
0	0	0
0	1	0
0	0	0



Figure 4: Stuck and 0 AND gate and truth table

"Figure 5" shows the stuck at 1 fault with an OR gate where the input "A" is stuck at logic 1. This will produce 4 outputs at logic 1 instead of 3 if the OR gate was working correctly.

A	B	Y
1	0	1
1	0	1
1	1	1
1	1	1



Figure 5: Stuck at 0 OR gate and truth table

Appropriate application examples

Single stuck at faults is a fault modelling technique to create physical faults in a circuit. The amount of stuck at faults is double the amount of inputs and outputs in the circuit for example if there is a total of three inputs/outputs (two inputs and one output) there will be a total of 6 possible stuck at faults.

Test vectors are test patterns used in a circuit which can detect faults in the circuit. The test pattern must be able to give a different output then that of a good circuit if a fault is present. For example if a good circuit has a output of logic 0 then the test pattern must be logic 1 if there is a fault.

There are 4 different stuck at faults that can occur. These are:

Stuck at 1 - input or output is at 1.

Stuck at 0 - input or output is at 0.

Bridging fault - two gate outputs shorted together.

Feedback bridging fault - input and output of a gate is shorted.

This is also shown in "figure 6".

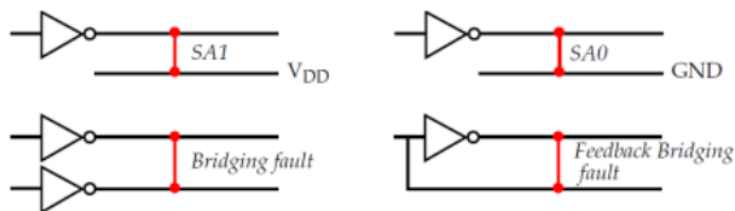


Figure 6: Type of stuck at faults

SSF fault types are identified and explained

(PLusquellic, 2004)

"Figure 7" shows how the test vector operates for a stuck at fault. By applying "11" to the NAND gate, an input "a" SA0 fault is found. The output of the NAND gate will change from 0 to 1 if "a" stuck at 0 fault is found.

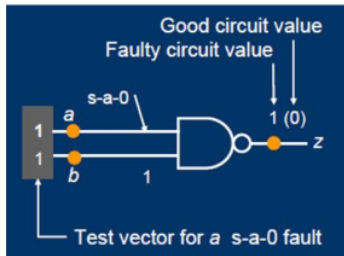


Figure 7: SA0 NAND gate

(Kastensmidt, 2008)

There is a technique used that reduces the amount of single stuck at faults this is called fault equivalence. This technique works by finding two or more faults and grouping them into subsets. These faults in the subsets can then be reduced into one fault and therefore one test pattern or vector. Using this fault collapse technique many of the tests can be removed and still produce the same outcome. (Ubar & Raik, 2017) (Mazumder, 2002)

"Figure 8" below shows the fault equivalence technique used on a 2 input AND gate and a 2 input OR gate. The AND gate produces a stuck at 0 fault this will give a logic 0 output and 2 out of 3 faults are taken away. Shown by the orange line. This is also applied to the OR gate and the total number of faults are taken down from six to four.

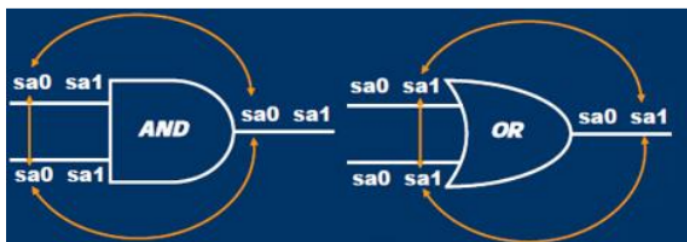


Figure 8: Fault equivalence technique

(Kastensmidt, 2008)

Extensive research carried out on this topic.

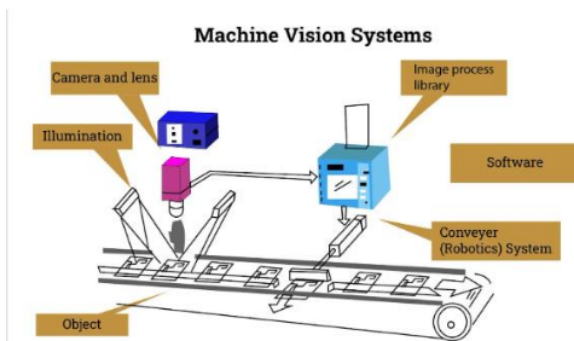
2.2 methods and techniques required to manufacture a sustainable product that meets the wider engineering requirements.

2.2.1 Machine vision

Machine vision is a field of artificial intelligence that deals with the development of computer systems that can accurately identify objects, interpret their environment, and take decisions based on the data received. It is an interdisciplinary area that combines computer science, optics, mechanical engineering, electronic engineering, and various other sciences. Machine vision systems generally involve the use of cameras and image processing software to capture images of the environment, analyse the data, and then use the information to make decisions or take action.

The most common application of machine vision is in the industrial setting. Machine vision is used to help automate the manufacturing process, allowing companies to produce products more quickly and accurately. This technology is also used in robotics, where it is used to guide robots in their movements and to identify objects in their environment.

In the future, machine vision will likely be used in a variety of other areas, such as autonomous vehicles, facial recognition systems, and home security systems. It will continue to evolve as the technology improves and new applications are developed. "Figure 9" shows the machine vision system.



This should have a ref source to support the research findings

Figure 9: Machine vision system

2.2.2 Frequency signature analysis

Frequency signature analysis is a technique used to identify the characteristics of a signal or waveform. It involves measuring the frequency components of a signal and then analysing the relative amplitudes of the components to gain information about the signal. Frequency signature analysis is used in several different fields, including engineering, biology, and music.

In engineering, frequency signature analysis can be used to detect and identify problems in electronic equipment and systems. By analysing the frequency components of a signal, engineers can detect any irregularities or anomalies in the signal which may indicate a problem or fault. This technique can also be used to improve the performance of a system by identifying areas where the system is not operating optimally. An example of this is the use of a spectrum analyser to identify the frequency components of a vibration signal. This technique is used to identify defects in machinery as well as to diagnose problems with engines, pumps, and other mechanical components. (artesis, 2022) (Fossum, 2022)

There are some good points made in this section

2.2.3 in circuit test

In circuit testing (ICT) is a type of electrical testing used to determine the functionality of an electronic circuit. ICT is performed by inserting probes into the device under test (DUT) and measuring the voltage, current and other characteristics of the device. This type of testing allows for a more comprehensive assessment of the device than traditional tests such as functional tests.

The goal of ICT is to ensure that the circuit is functioning properly and that all components are operating within their specified parameters. This is achieved by testing each component of the circuit individually and then testing the complete system. The testing process begins with identifying the type of device and its components. This includes identifying the power source, the output circuit, the input devices and the type of signal being sent. Once all components have been identified, the ICT process begins by measuring the voltage, current and other parameters of each component.

The next step in ICT is testing the circuit as a whole. This is done by connecting the components of the circuit together and then measuring the voltage, current and other signals. The tester will then compare the measurements to the expected values. This type of testing is often used to identify any problems with the circuit, such as shorts, opens or other anomalies (ELECTRONICS, 2022) (Technologies, 2022)

Good research carried out here. An image example would have supported the content

2.3 Electrostatic discharge (ESD)

Electrostatic discharge is when static electricity gets transferred into electronic devices. This occurs when insulated surfaces rub together or pull apart. This causes one of the surfaces to gain electrons and the other surface losing electrons. This creates a big potential difference which can cause damage. Due to ICs and the components on the ICs being vulnerable to the discharging it can cause a lot of damage to the ICs. "Figure 10" shows the ESD voltages that can occur from everyday occurrences.

Source ESD	Typical ESD voltages in KV at 20% humidity
Walk across vinyl floor	12KV
Walk across synthetic carpet	35KV
Opening plastic bag	20KV
Rising from foam cushion	18KV
Removing plastic tape from PCB	12KV
Removing shrink film from PCB	12KV
Triggering vacuum solder remover	8KV
Spraying freezer spray	15KV

There should be a ref source for this

Figure 10: ESD voltages

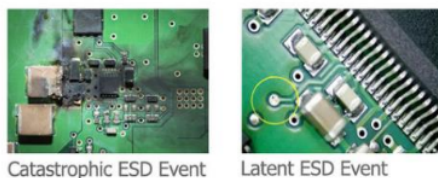
"Figure 11" shows the range of voltages that the components in the ICs are susceptible to with respect to ESD. This shows that some components can withstand higher voltages than others which is taken into consideration with ESD prevention methods.

Components	ESD susceptibility
BJT Transistor	380 – 7000 V
CMOS logic	250 – 3000 V
EPROM	100 V
Film resistor	300 – 3000 V
TTL logic	1000 – 25000 V
Micro chips	10 V

This should have a ref source

Figure 11: ESD susceptibility

With the large amount of voltages placed on the components there is a large amount of heat produced. The amount of heat produced can cause the components to melt and fail. If the damage put on the components is not an instant failure then the damage can cause a delayed failure which can reduce the lifespan of the component. This is called the latent effect. (Rouse, 2011) "Figure 12" shows the damage caused by ESD.



A good example

Figure 12: Damage caused by ESD

(barcodefactory, 2022)

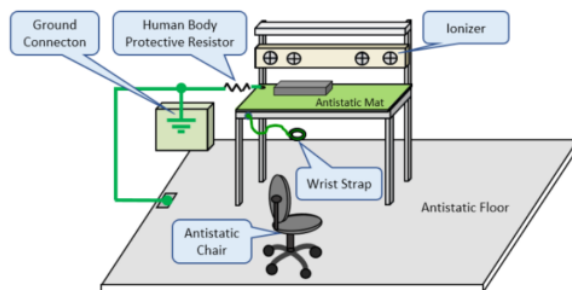
2.3.1 Prevention methods

ESD is a significant issue in many sectors because it can harm delicate electrical systems and components. There are several strategies that may be used to avoid ESD.

The adoption of appropriate grounding techniques is the first preventative measure. It's crucial to check that the equipment and surroundings are correctly grounded while dealing with delicate electrical components. This implies that all non-conductive materials, including carpets, furniture, and other objects, should be well insulated and connected to a good earth ground. Shoes, wrist straps, and antistatic carpets can all be used to lessen the build-up of static electricity.

ESD protection packaging is a further effective means of preventing ESD. This kind of packaging works by creating an electrostatic shield around the components to stop ESD. It is often comprised of conductive materials, such polyethylene or aluminium foil, and it is intended to absorb any possible static charge. The packing should also be stored in a dry, temperature-controlled location that is not vulnerable to ESD.

Finally, while handling or storing sensitive components, it's crucial to use ESD-safe materials. This implies that ESD-safe materials should be used wherever possible because they will help to lower the risk of ESD. In order to prevent the build-up of static electricity, it is also crucial to keep all surfaces clean and free of dust and dirt. "Figure 13" shows ESD prevention methods. (semicon.sanken, 2022) (DAS, 2022) (Analysis, 2022)



Good preventive examples have been explained

Figure 13: ESD prevention method

3 Design of assignment requirements

"Figure 14" is the circuit design used as the CUT for the test and analysis.

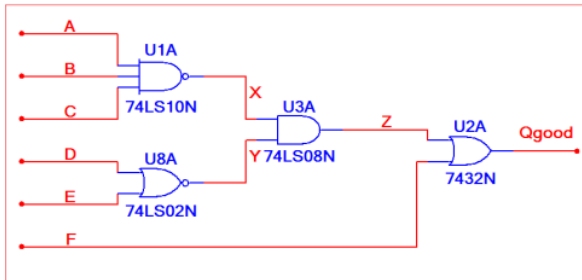


Figure 14: Circuit under test model

3.1 stuck and fault modelling

The SA fault model technique is used to detect SA0 and SA1 faults. A formula $m+1$ (where m is the amount of inputs) is used to reduce the amount of test vectors required for the gates shown in "Figure 14".

"Figure 15" shows the 3 input NAND gate and the truth table, there will be 4 tests needed.

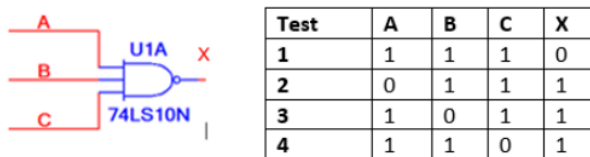


Figure 15: 3 input NAND gate and truth table

"Figure 16" shows the 2 input NOR gate with reduced tests and the truth table.

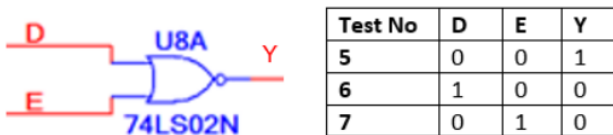


Figure 16: 2 Input NOR gate and truth table

“Figure 17” shows the 2 input AND gate with reduced tests and the truth table.

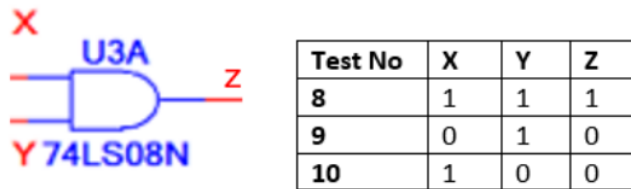
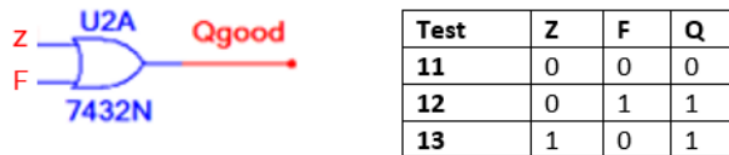


Figure 17: 2 input AND gate with truth table

“Figure 18” shows the 2 input OR gate with reduced tests and the truth table.



Good work. test vectors for gates have been identified

Figure 18: 2 input OR gate with reduced tests and the truth table

3.2 Test vectors and test patterns – Tables and reduction process

“Figure 19” shows the table for all the stuck at fault tests and each scenario of possible faults that are needed to test each stage.

Test	A	B	C	D	E	F	Qgood	HEX	X	Y	Z	Fault
1	1	1	1	0	0	0	0	70	0	1	0	A+B+C SA0
2	0	1	1	0	0	0	1	31	1	1	1	A SA1
3	1	0	1	0	0	0	1	51	1	1	1	B SA1
4	1	1	0	0	0	0	1	61	1	1	1	C SA1
5	0*	0*	0*	0	0	0	1	01	1	1	1	D+E SA1
6	0*	0*	0*	1	0	0	0	08	1	0	0	D SA0
7	0*	0*	0*	0	1	0	0	04	1	0	0	E SA0
8	0*	0*	0*	0	0	0	1	01	1	1	1	X+Y SA0
9	1	1	1	0	0	0	0	70	0	1	0	X SA1
10	0*	0*	0*	1**	1**	0	0	0C	1	0	0	Y SA1
11	1	1	1	1**	1**	0	0	7C	0*	0*	0	F+Z SA1
12	1	1	1	1**	1**	1	1	7F	0*	0*	0	F SA0
13	0*	0*	0*	0	0	0	1	01	1	1	1	Z SA0

*At least one condition is at logic 0.
**At least one condition is at logic 1.

Application of redundancy rules are identified

Figure 19: Stuck at fault table

The circled tests in “figure 19” show the duplicated tests. These tests can be reduced to just 1 test per duplicate. Test 1 and 9 are duplicates and tests 5, 8, 13 are duplicates this means these can be reduced to just one test.

"Figure 20" shows the updated table after the duplicated tests have been removed. The removed tests are test 9,8 and 13.

Test	A	B	C	D	E	F	<u>Qgood</u>	hex	X	Y	Z	Fault
1	1	1	1	0	0	0	0	70	0	1	0	A+B+C SA0, X SA1
2	0	1	1	0	0	0	1	31	1	1	1	A SA1
3	1	0	1	0	0	0	1	51	1	1	1	B SA1
4	1	1	0	0	0	0	1	61	1	1	1	C SA1
5	0*	0*	0*	0	0	0	1	01	1	1	1	D+E SA1, X+Y SA0, Z SA0
6	0*	0*	0*	1	0	0	0	08	1	0	0	D SA0
7	0*	0*	0*	0	1	0	0	04	1	0	0	E SA0
10	0*	0*	0*	1**	1**	0	0	0C	1	0	0	Y SA1
11	1	1	1	1**	1**	0	0	7C	0*	0*	0	F+Z SA1
12	1	1	1	1**	1**	1	1	7F	0*	0*	0	F SA0

*At least one condition is at logic 0.

**At least one condition is at logic 1.

Reduced table is correct with redundancies eliminated

Figure 20: Reduced table

With the (*) on test 5 it can be altered to match test 4. This will then create a redundant test vector and due to the equivalence rule the test vector can be removed. This is also applied to test 6 and 10. The table is then further reduced and the faults from the redundant test vector are applied to the existing test vector. This is shown in "Figure 21" below.

Test No	A	B	C	D	E	F	<u>Qgood</u>	HEX	X	Y	Z	Fault
1	1	1	1	0	0	0	0	70	0	1	0	A+B+C SA0, X SA1
2	0	1	1	0	0	0	1	31	1	1	1	A SA1
3	1	0	1	0	0	0	1	51	1	1	1	B SA1
4	1	1	0	0	0	0	1	61	1	1	1	C SA1, D+E SA1, X+Y SA0, Z SA0
6	0*	0*	0*	1	0	0	0	08	1	0	0	D SA0, Y SA1
7	0*	0*	0*	0	1	0	0	04	1	0	0	E SA0
11	1	1	1	1*	1*	0	0	7C	0*	0*	0	F+Z SA1
12	1	1	1	1*	1*	1	1	7F	0*	0*	0	F SA0

*At least one condition is at logic 0.

**At least one condition is at logic 1.

Figure 21: Final reduced table

Good application of the wildcard rule to further eliminate redundancies

3.3 Design test using word generator

"Figure 22" shows the circuit for the Automatic test equipment (ATE). This will be used for the circuit under test by using a word generator which will create a test sequence for the inputs.

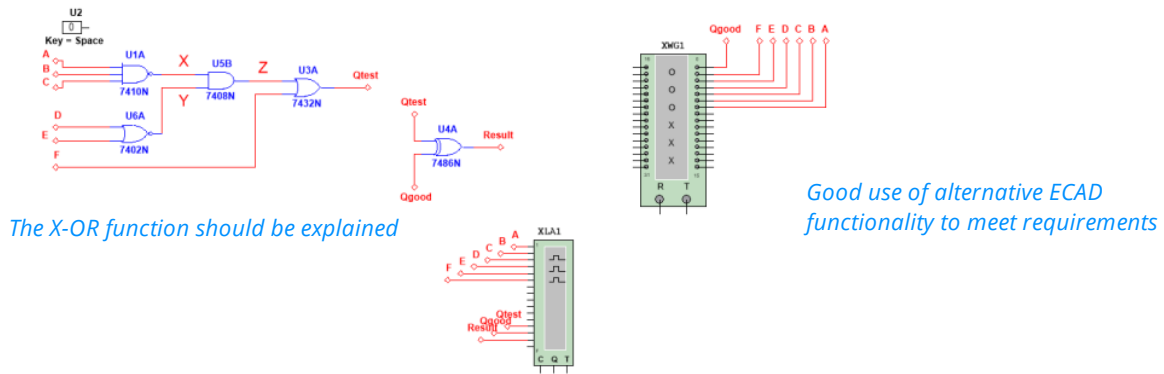
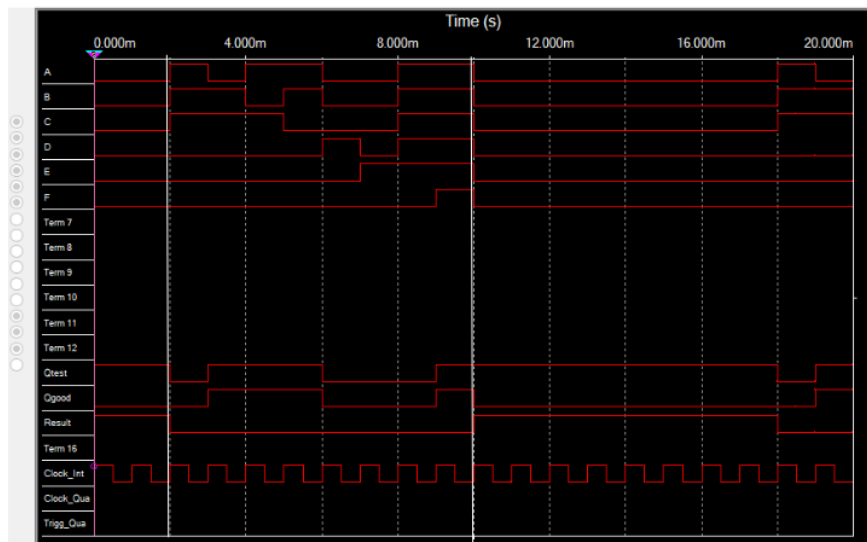


Figure 22: ATE circuit

This should be described as a pulse waveform

The logic analyser (XLA1) shown in "figure 22" will produce a square wave from the results shown in "figure 23". "Figure 23" shows that there is no fault, this is shown from the "result" line as there is no pulse and the result line stays flat between the 2 white cursors. This shows that the circuit is working as intended due to there being no 'stuck at' faults put on the circuit.



NFF condition is achieved. This is crucial before the test stages

Figure 23: No fault found ATE

4 Analysis of NI MultiSim results

The circuit shown in “figure 22” was used to test the stuck at faults from “figure 21”. 3 Faults from “figure 21” was put on the circuit to prove that the faults would show the correct results from the logic analyser. This is shown below. ‘U2’ on the circuit in “figure 24” is used to set the inputs to either stuck at logic 0 or stuck at logic 1.

4.1 A stuck at 0

“Figure 24 shows the test circuit with A stuck at logic 0.

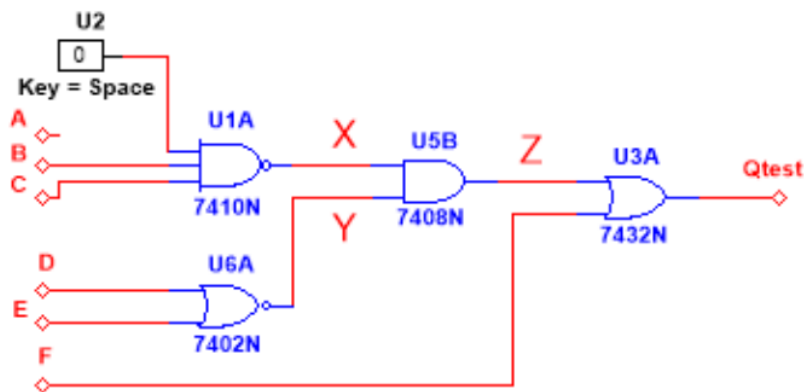
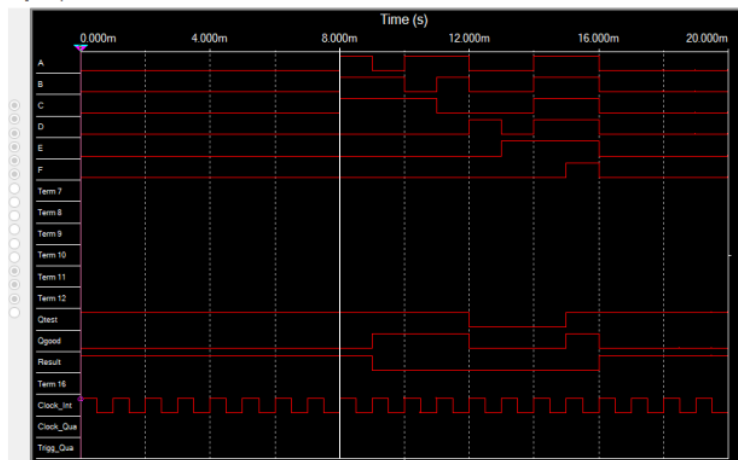


Figure 24: A stuck at 0

“Figure 25” shows the fault from the logic analyser. This is shown under the “result” waveform where the waveform is on logic 1 as shown by the cursor where it should be on logic 0.



Fault condition is set and identified in the output

Figure 25: A stuck at 0 logic analyser

4.2 D stuck at 0

"Figure 26" shows the test circuit with D stuck at logic 0.

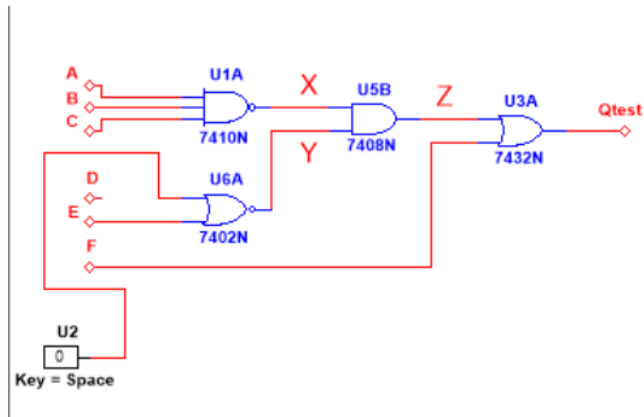


Figure 26: D stuck at 0

"Figure 27" shows the result of the logic analyser with D stuck at logic 0. The "result" waveform pulses to logic 1 indicating a fault due to D being stuck at 0.

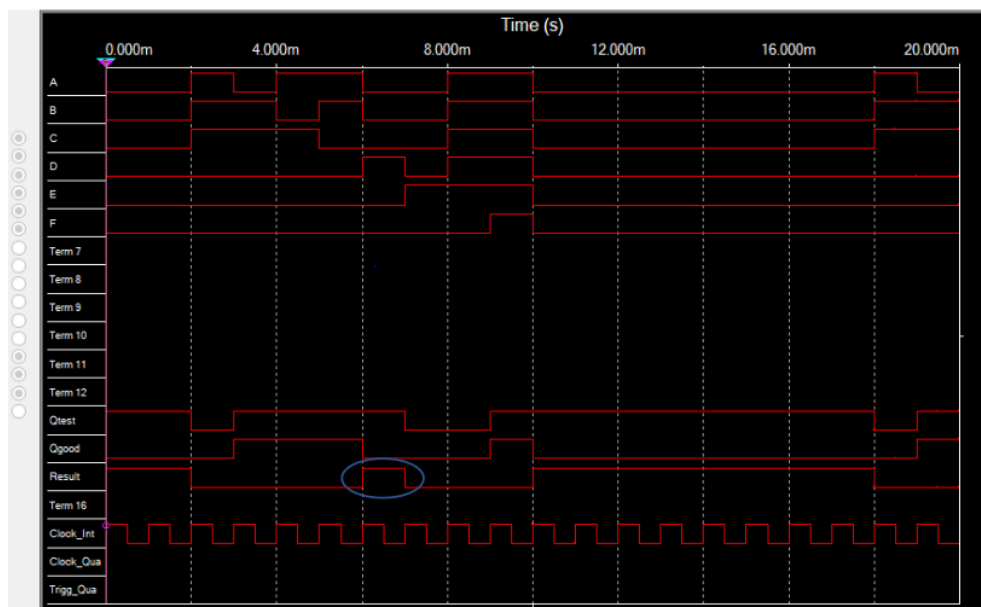


Figure 27: D stuck at 0 logic analyser

Fault condition set and identified in the output

4.3 B stuck at 1

"Figure 27" shows the test circuit with B stuck at logic 1.

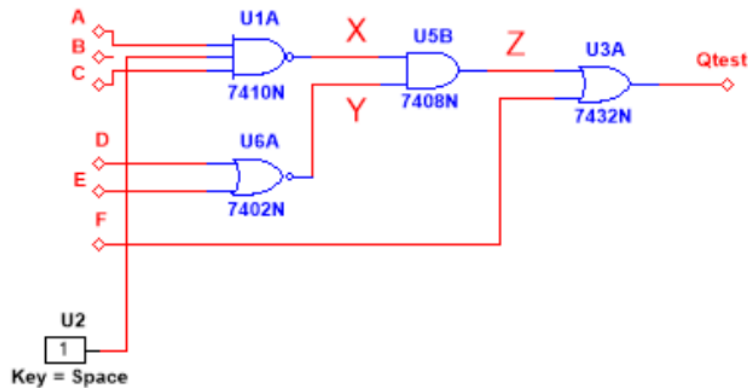


Figure 28: B stuck at 1

"Figure 29" shows the result of the logic analyser with B stuck at logic 1. The "result" waveform pulses to logic 1 indicating a fault with B stuck at logic 1. This is shown in the circle on "Figure 29".

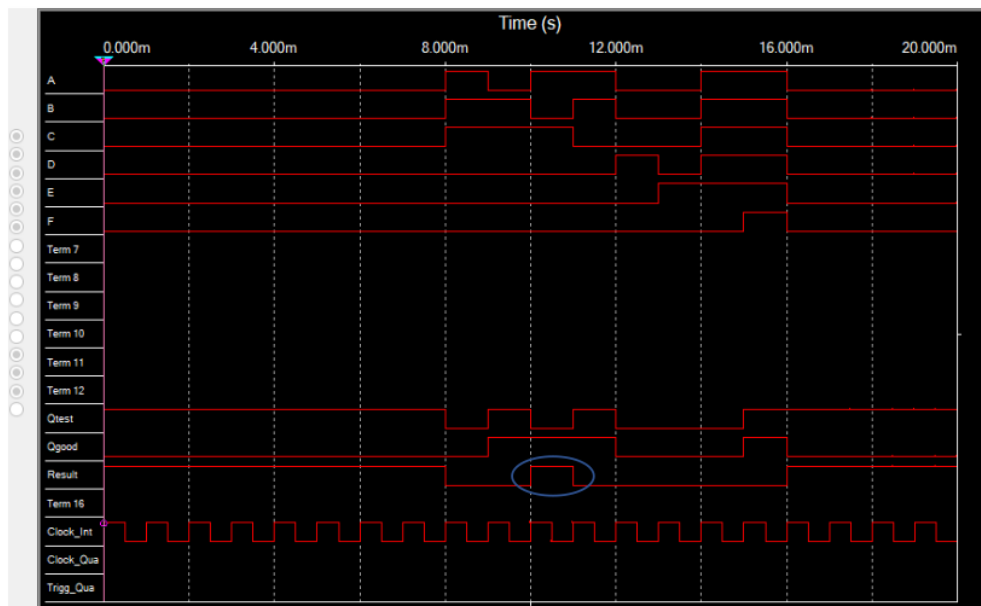


Figure 29: B stuck at 1 logic analyser

Third fault is set and identified in the output

5 Practical build and test using Labview

This is not the LabVIEW section

5.1 6-bit register design and test.

To test the CUT, a 6-bit register was built as a part of ATE design method. The faults will be created using the same stuck at method and the results will be analysed.

"Figure 30" shows the truth table with the current and next state that was designed. This produced the test vectors for inputs from A-F.

Current state						Next state					
A	B	C	D	E	F	A+	B+	C+	D+	E+	F+
1	1	1	0	0	0	0	1	1	0	0	0
0	1	1	0	0	0	1	0	1	0	0	0
1	0	1	0	0	0	1	1	0	0	0	0
1	1	0	0	0	0	0	0	0	1	0	0
0	0	0	1	0	0	0	0	0	0	1	0
0	0	0	0	1	0	1	1	1	1	1	0
1	1	1	1	1	0	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	0	0	0

Next states have been identified

Figure 30: 6-bit generator next state truth table

Karnaugh maps were used which creates the logic states needed for the feedback combinational logic for the input sequence. The Karnaugh maps can be seen in the appendix "9.1 Karnaugh maps".

From the Karnaugh maps the Boolean expressions were derived shown below for QA-QF.

$$QA = A \cdot B \cdot C \cdot D \cdot E + A \cdot NB \cdot C \cdot ND \cdot NE \cdot NF + NA \cdot B \cdot C \cdot ND \cdot NE \cdot NF +$$

$$NA \cdot NB \cdot NC \cdot ND \cdot E \cdot NF$$

$$QB = A \cdot C \cdot ND \cdot NE \cdot NF + A \cdot B \cdot C \cdot D \cdot E + NA \cdot NB \cdot NC \cdot ND \cdot E \cdot NF$$

$$QC = NA \cdot NB \cdot NC \cdot ND \cdot E \cdot NF + NA \cdot B \cdot C \cdot ND \cdot NE \cdot NF + A \cdot B \cdot C \cdot ND \cdot NE \cdot NF + A \cdot B \cdot C \cdot D \cdot E$$

19 *This does not belong here!*

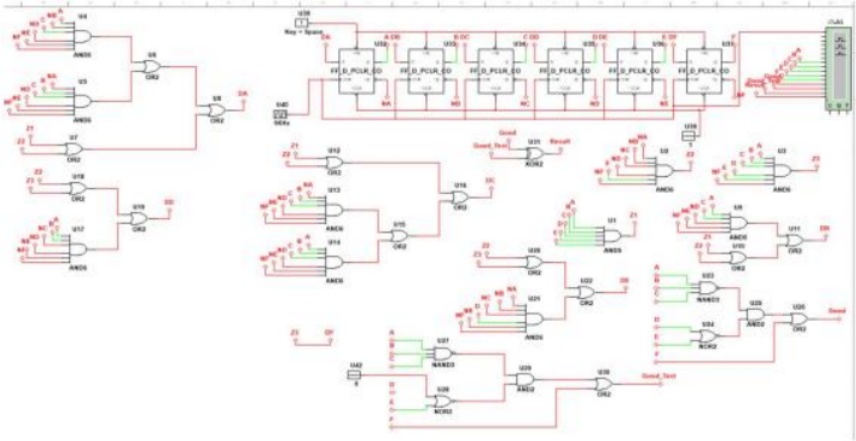
$$QD = NA \cdot NB \cdot NC \cdot ND \cdot E \cdot NF + A \cdot B \cdot NC \cdot ND \cdot NE \cdot NF + A \cdot B \cdot C \cdot D \cdot E \cdot NF$$

$$QE = NA \cdot NB \cdot NC \cdot ND \cdot E \cdot NF + NA \cdot NB \cdot NC \cdot D \cdot NE \cdot NF + A \cdot B \cdot C \cdot D \cdot E \cdot NF$$

$$QF = A \cdot B \cdot C \cdot D \cdot E \cdot NF$$

From the next state design process, the 6-bit register was designed on multisim shown in “figure 31”. The Boolean expressions from the Karnaugh maps are implemented into the feedback circuits which minimizes the combinational circuit.

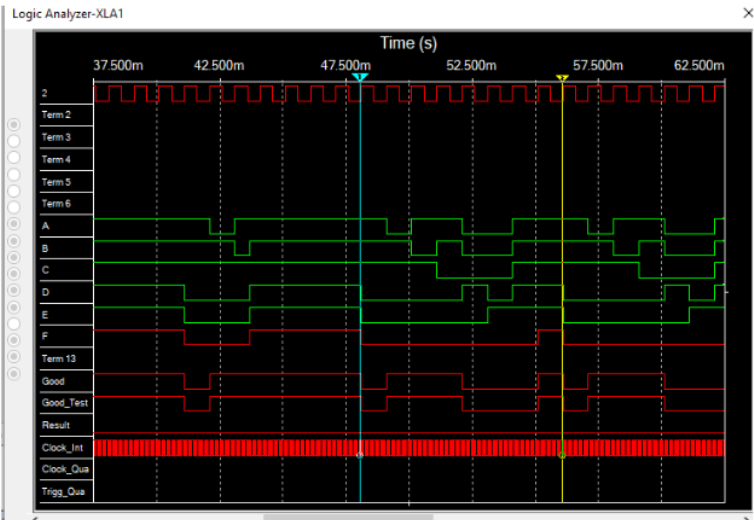
The output of the CUT shown in “figure 31” is compared with a working identical circuit. The outputs of these 2 circuits is inputted into a XOR gate which differentiates the 2 circuits.



Comparison of outputs is explained

Figure 31: Multisim 6-bit register

The circuit is tested first with no faults this will prove that the circuit is working as intended. “Figure 32” shows the waveform from the test results. The ‘result’ waveform (which is the output from the XOR gate) has zero pulses to logic 1 and stays at logic 0 which proves the circuit is working as intended.



Critical NFF state is achieved

Figure 32: ATE no fault found.

Stuck at faults were then placed on the CUT ATE. To prove that the circuit is working correctly.

“Figure 33” shows the fault condition A stuck at zero placed on the NAND gate.

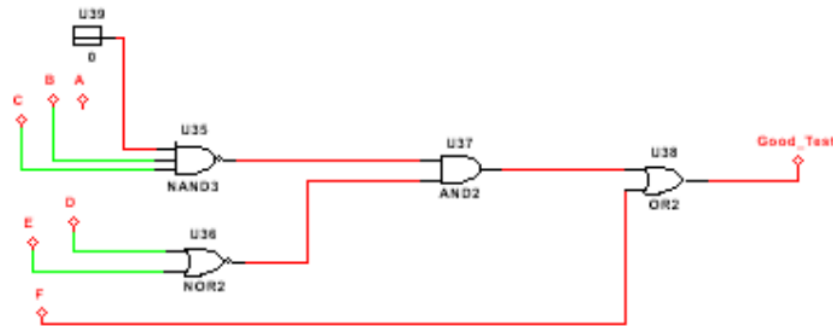


Figure 33: ATE A stuck at 0

“Figure 34” shows the ATE waveform results with A stuck at 0. The ‘result’ waveform pulses to logic 1 highlighted by the circle on the waveform. This indicates that there is an error due to A being stuck at 0. This shows that the ATE is working correctly.

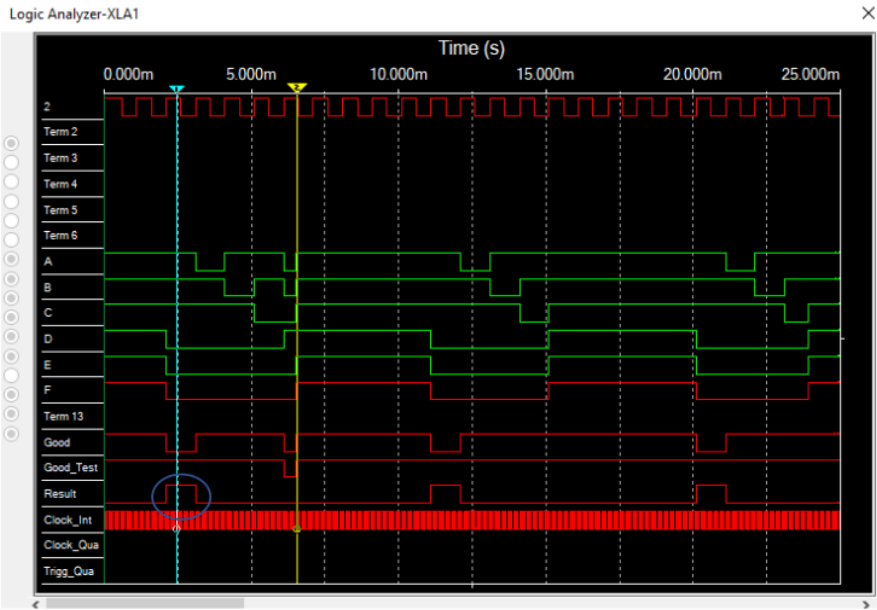


Figure 34: ATE stuck at 0 waveform

Fault condition is set and fault identified at the output

This test was then repeated with D stuck at 0 shown in “Figure 35”.

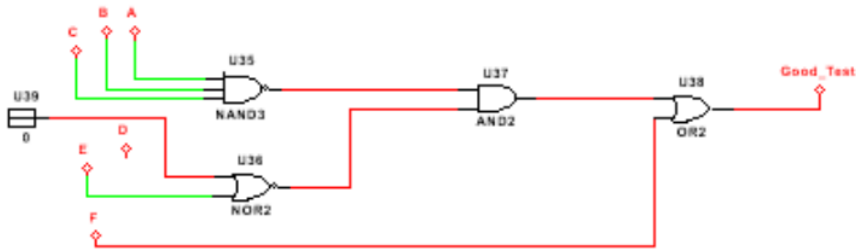


Figure 35: ATE D stuck at 0

The ATE waveform result with D stuck at logic 0 is shown “figure 36”. The ‘result’ waveform pulses to logic 1 indicated by the circle which proves there is an error when D is stuck at logic 0.

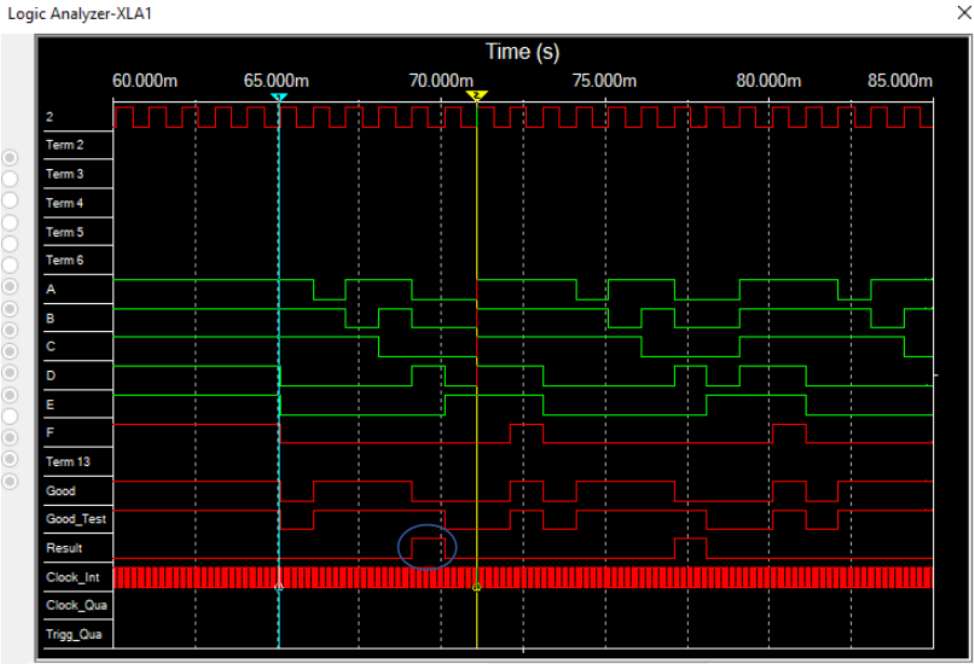


Figure 36: ATE D stuck at 0 waveform

Second fault set and identified

This test was also done with B stuck at 1 shown in “Figure 37”.

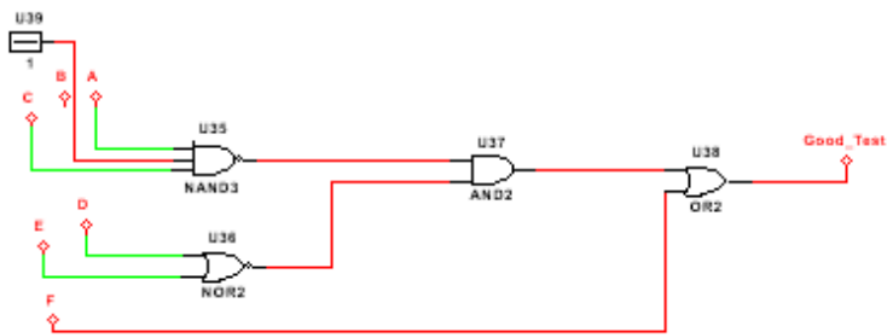


Figure 37: ATE B stuck at 1

The waveform shown in “figure 38” shows the result from B stuck at logic 1. The circled result shows the error where B is stuck at logic 1 which pulses the ‘result’ waveform indicating an error.

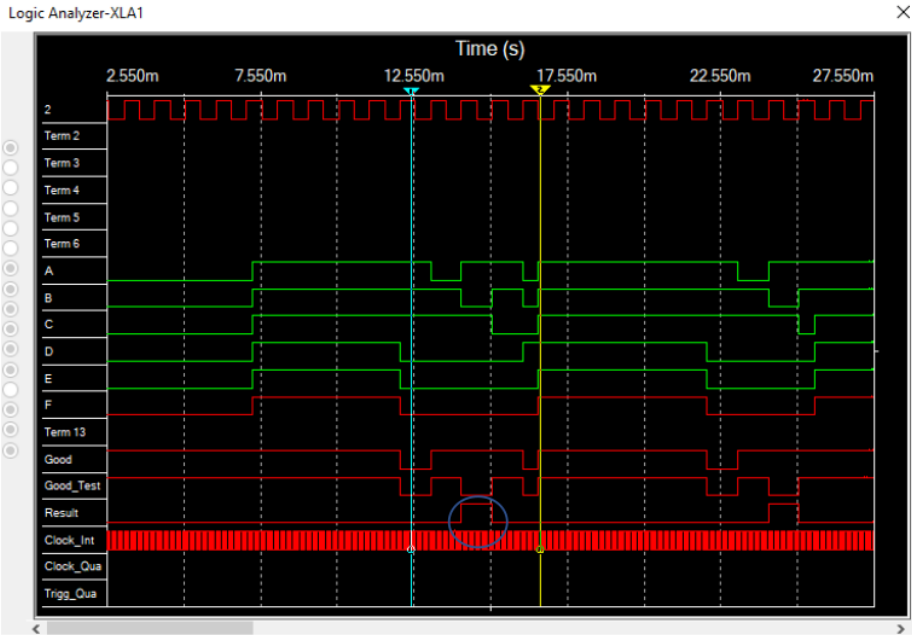
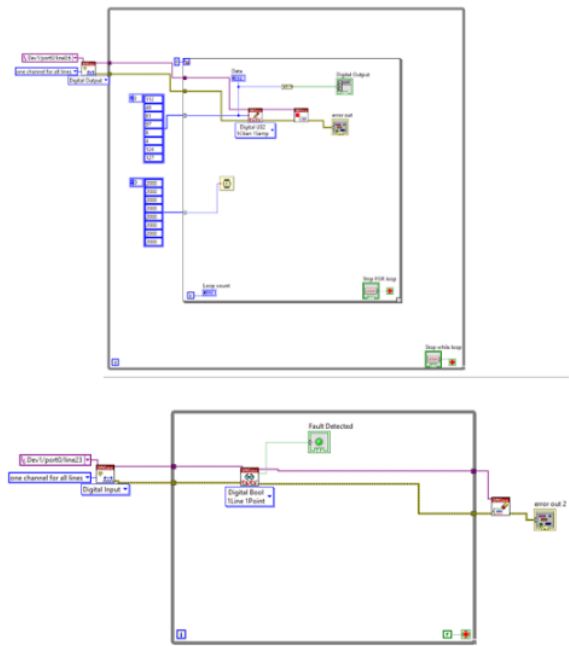


Figure 38: ATE B stuck at 1 waveform

Third fault set and identified

This should have a new heading here. This section applies to the practical part of the tasks and should be separate from the ECAD simulations.

Another method of testing the CUT was done to prove that the circuit was working correctly and to compare results. This method was designed by using Labview and implemented on the National Instruments ELVIS prototyping board. "Figure 39" shows the circuit design on labview.



The program functions should be explained

Figure 39: Labview circuit design

The results from the Labview and NI ELVIS prototyping board are shown in the appendix under "9.2 Labview and NI elvis board". A table of results was then made shows in "Figure 40" shown below.

	multisim ATE 6-Bit Register				LabView and ELVIS Board			
	No fault	A SA0	D SA0	B SA1	No fault	A SA0	D SA0	B SA1
Fault found	NO	YES	YES	YES	NO	YES	YES	YES

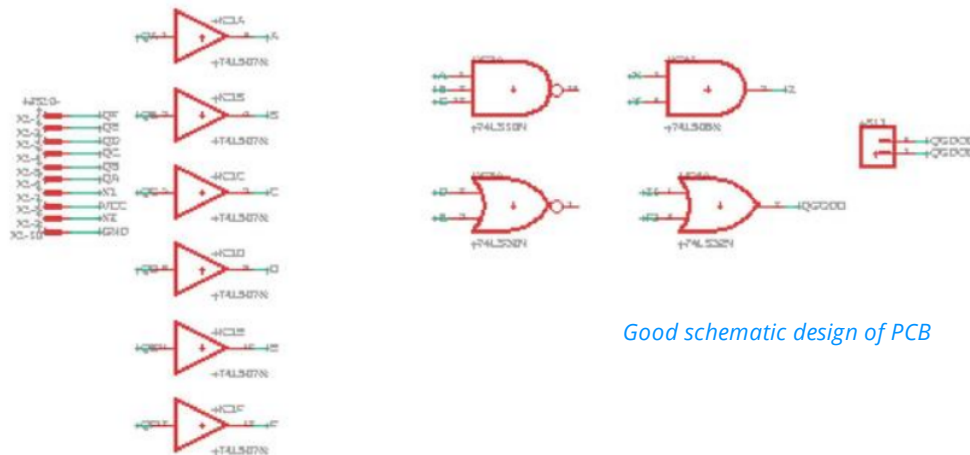
Good use of table

Figure 40: ATE 6 bit register comparison table

The table shows that both the Multisim and Labview/Elvis board results match. This proves that the results obtained are accurate and both methods work as intended.

6 CAM design and build of prototype

A CAM software (Computer Aided Manufacture) was used to design prototype PCB that is sustainable. The software used was Eagle Autodesk. This software was used to design the schematic for the PCB. The design was then turned into Gerber files which will convert the design into a schematic. The design for the PCB is shown in “figure 41”.



Good schematic design of PCB

Figure 41: PCB CAM design

The Gerber files were then sent away to PCBway where the PCB board can be made and sent back. The customer needs were met due to the PCB boards meeting the spec from the Gerber files. The PCB board was then tested on the NI Elvis board with stuck at faults shown in figures “56-58” under section 9.3 in the appendix.

These tests proved that the PCB boards are working as intended by producing the expected results from the test and also matching the results from the 6 bit register.

The PCB boards were manufactured in a sustainable, reliable manner. This was done by using components that are recycled and produced legally and ethically.

The PCB CAM design is missing.

The Gerber files are missing

7 Conclusions and Recommendations

The research done on this task gave a good understanding on fault modelling on ICs, the use of vision systems as a modern way of manufacturing in a sustainable manner and how ESD can affect ICs in a negative way and the methods to reduce the effect of ESD.

The knowledge gained from the research task was used during the assignment to complete the tasks such as the stuck at fault modelling during the design of the CUT and the creation of the truth tables. This was then carried over, using the same CUT for the 6-bit register. The CUT design was then simulated on Multisim and then implemented practically on the NI Elvis board. The results were then compared to prove that the design and testing was successful which proved that the theory is correct. A CAM software was then used to design a PCB and the Gerber files were sent away to be built. The PCB was then tested practically on the NI Elvis board to prove that the PCB was working correctly.

With knowledge of the damage ESD can cause from the research great care was taken into the manufacturing process that all precautions were taken such as proper grounding.

When comparing the results from the simulated practical and theory it showed that the theory is correct. This is due to the tests undertaken all matched which is a clear sign that the theory learnt from the research is correct. The testing done on this assignment was cost effective such as the use of Labview and Multisim simulation and practically with the NI Elvis board. If further testing was needed a ICT test can be carried out which is a more in-depth method of testing but the equipment needed is expensive.

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A good number of ref sources used in research

9. Appendix

9.1 Karnaugh maps

ABC DEF	000	001	011	010	100	101	111	110
000	0	0	1	0	0	1	0	0
001	0	0	0	0	0	0	0	0
011	0	0	0	0	0	0	0	0
010	1	0	0	0	0	0	0	0
100	0	0	0	0	0	0	0	0
101	0	0	0	0	0	0	0	0
111	0	0	0	0	0	0	1	0
110	0	0	0	0	0	0	1	0

Figure 42: QA Karnaugh maps

ABC DEF	000	001	011	010	100	101	111	110
000	0	0	0	0	0	1	1	0
001	0	0	0	0	0	0	0	0
011	0	0	0	0	0	0	0	0
010	1	0	0	0	0	0	0	0
100	0	0	0	0	0	0	0	0
101	0	0	0	0	0	0	0	0
111	0	0	0	0	0	0	1	0
110	0	0	0	0	0	0	1	0

Figure 43: QB Karnaugh maps

ABC DEF	000	001	011	010	100	101	111	110
000	0	0	1	0	0	0	1	0
001	0	0	0	0	0	0	0	0
011	0	0	0	0	0	0	0	0
010	1	0	0	0	0	0	0	0
100	0	0	0	0	0	0	0	0
101	0	0	0	0	0	0	0	0
111	0	0	0	0	0	0	1	0
110	0	0	0	0	0	0	1	0

Figure 44: QC Karnaugh maps

ABC DEF	000	001	011	010	100	101	111	110
000	0	0	0	0	0	0	0	1
001	0	0	0	0	0	0	0	0
011	0	0	0	0	0	0	0	0
010	1	0	0	0	0	0	0	0
100	0	0	0	0	0	0	0	0
101	0	0	0	0	0	0	0	0
111	0	0	0	0	0	0	0	0
110	0	0	0	0	0	0	1	0

Figure 45: QD Karnaugh maps

ABC DEF	000	001	011	010	100	101	111	110
000	0	0	0	0	0	0	0	0
001	0	0	0	0	0	0	0	0
011	0	0	0	0	0	0	0	0
010	1	0	0	0	0	0	0	0
100	1	0	0	0	0	0	0	0
101	0	0	0	0	0	0	0	0
111	0	0	0	0	0	0	0	0
110	0	0	0	0	0	0	1	0

Figure 46: QE Karnaugh maps

ABC DEF	000	001	011	010	100	101	111	110
000	0	0	0	0	0	0	0	0
001	0	0	0	0	0	0	0	0
011	0	0	0	0	0	0	0	0
010	0	0	0	0	0	0	0	0
100	0	0	0	0	0	0	0	0
101	0	0	0	0	0	0	0	0
111	0	0	0	0	0	0	0	0
110	0	0	0	0	0	0	1	0

Figure 47: QF Karnaugh maps

9.2 Labview and NI elvis board



NFF state is achieved

Figure 48: Labview no fault found

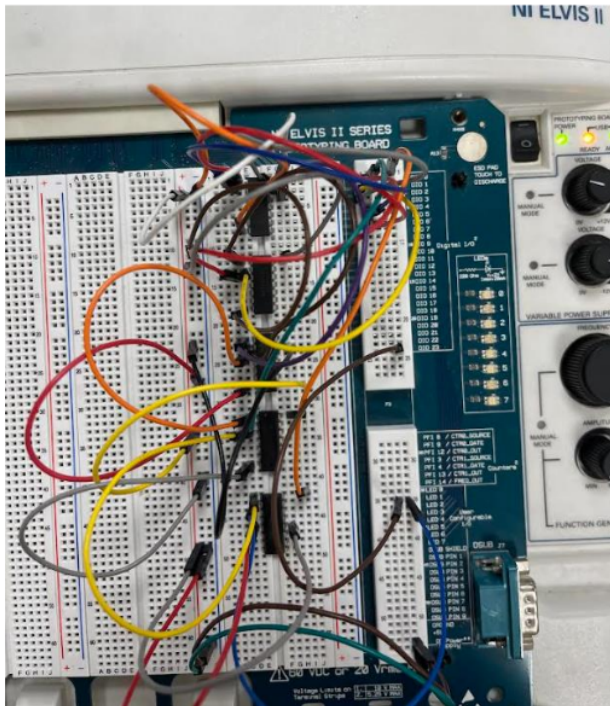


Figure 49: NI elvis no fault found

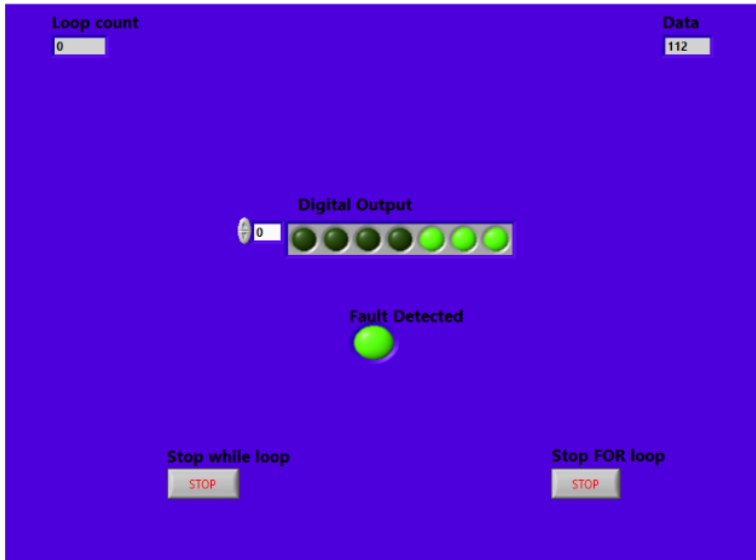


Figure 50: Labview A stuck at 0

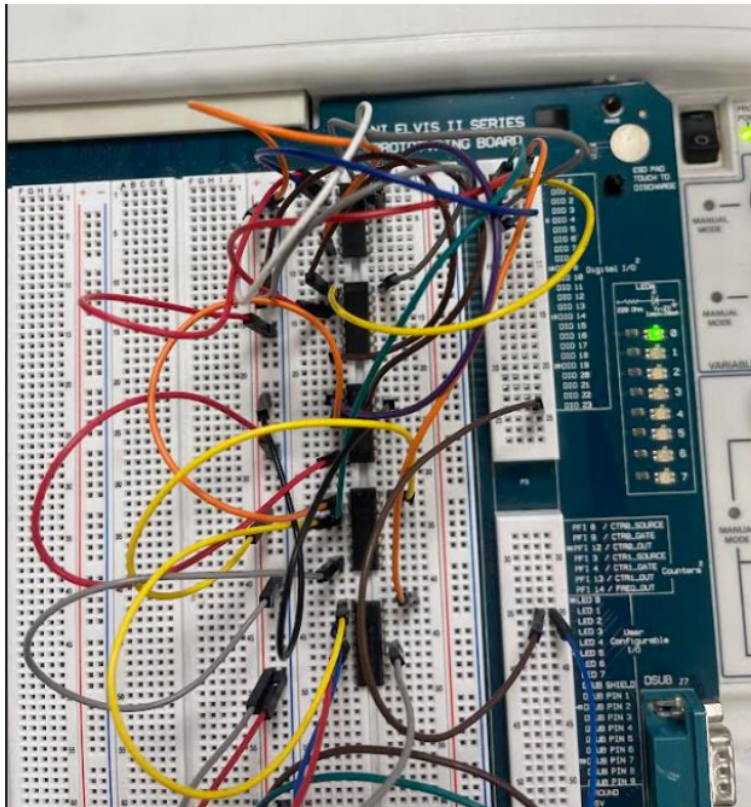


Figure 51: NI elvis A stuck at 0



Figure 52: Labview D stuck at 0

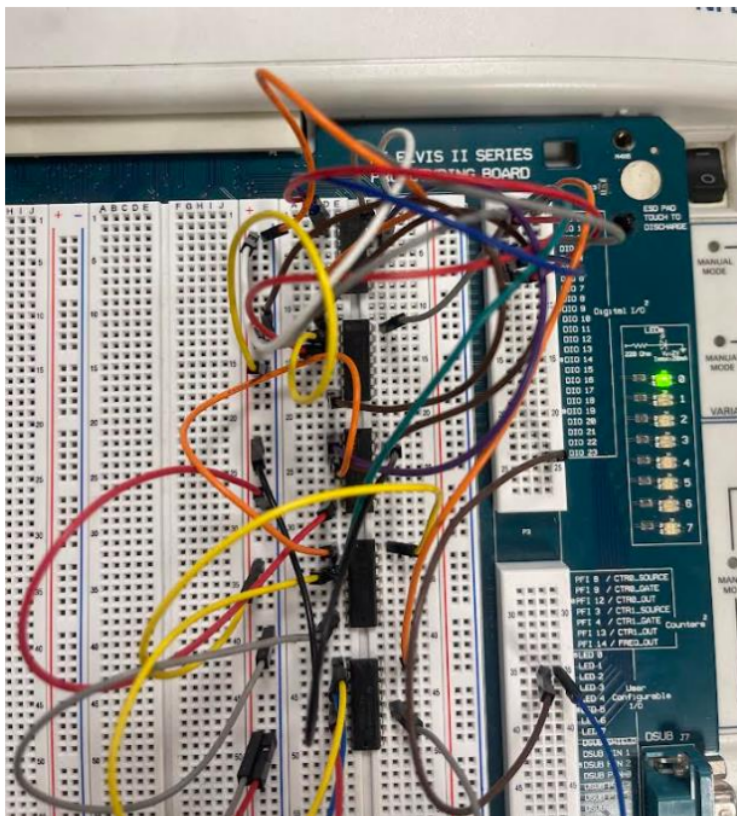


Figure 53: NI elvis D stuck at 0

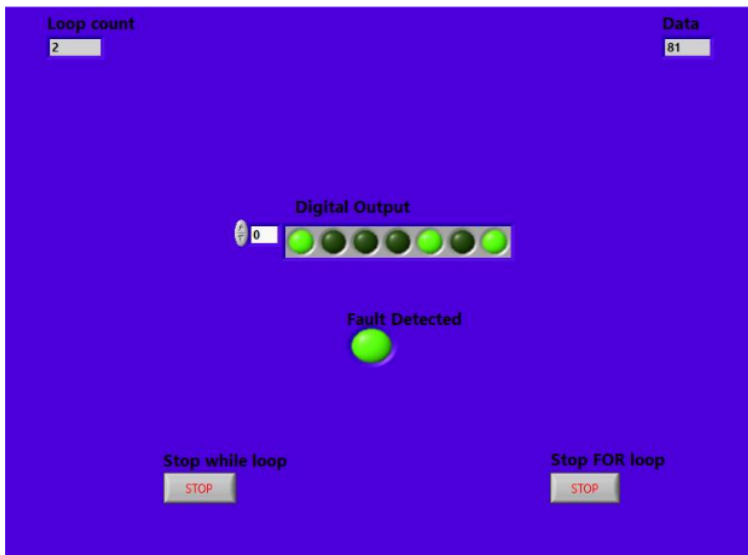


Figure 54: Labview B stuck at 1

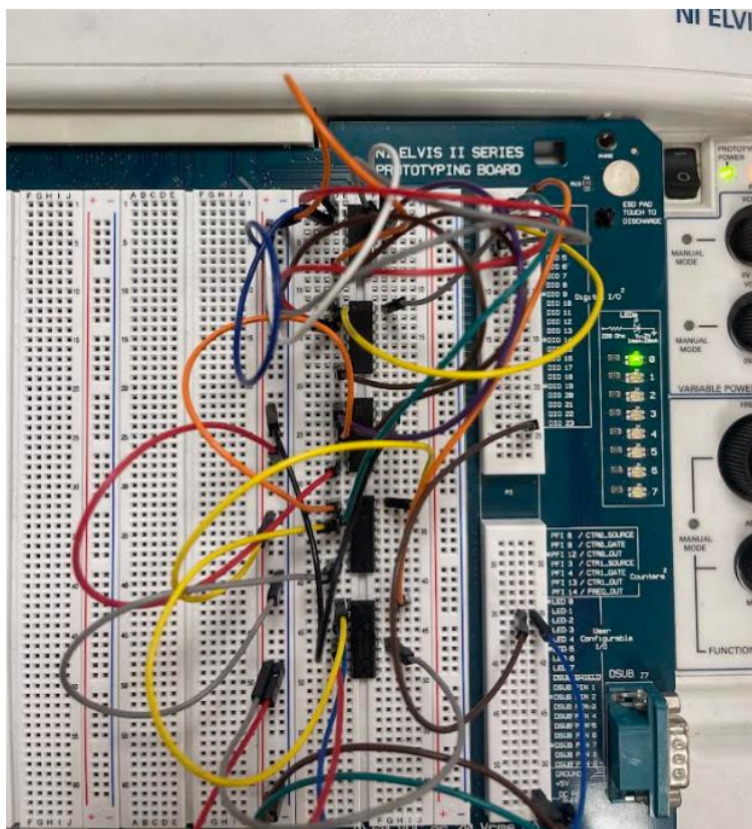


Figure 55: NI Elvis B stuck at 1

Three faults have been tested and faults detected

9.3 CAM PCB boards test

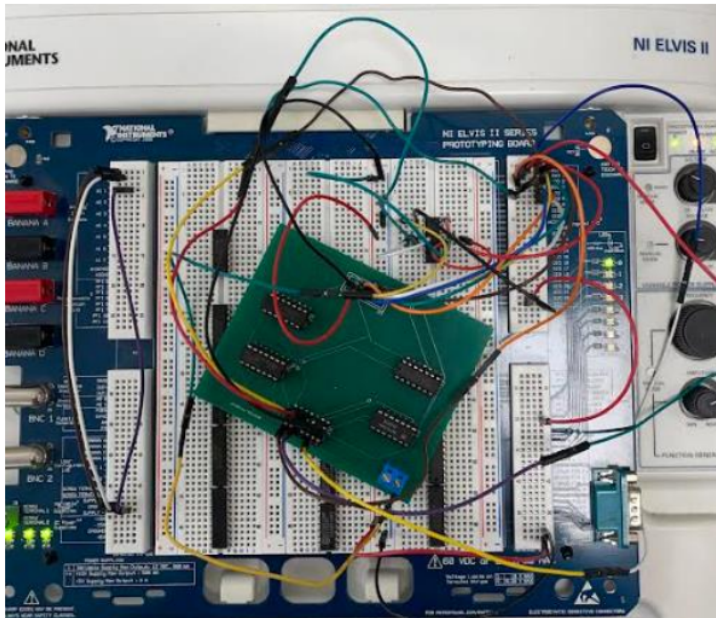


Figure 56: A stuck at 0 PCB

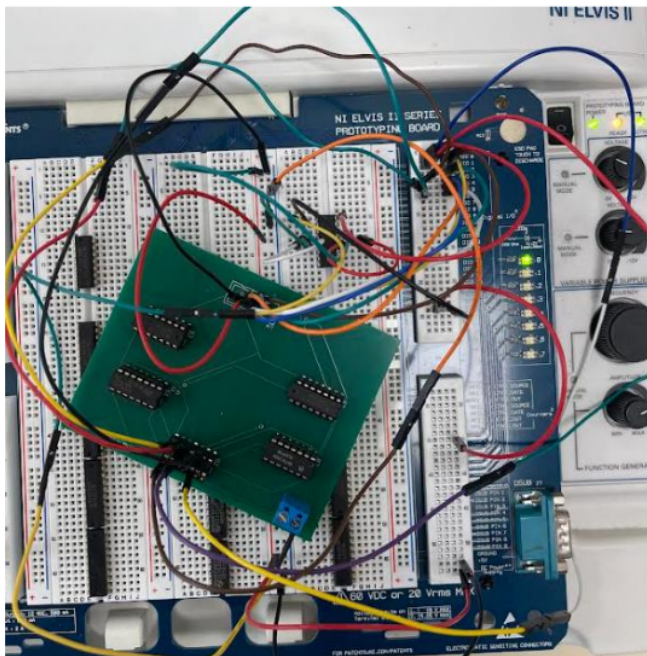


Figure 57: D stuck at 0 PCB

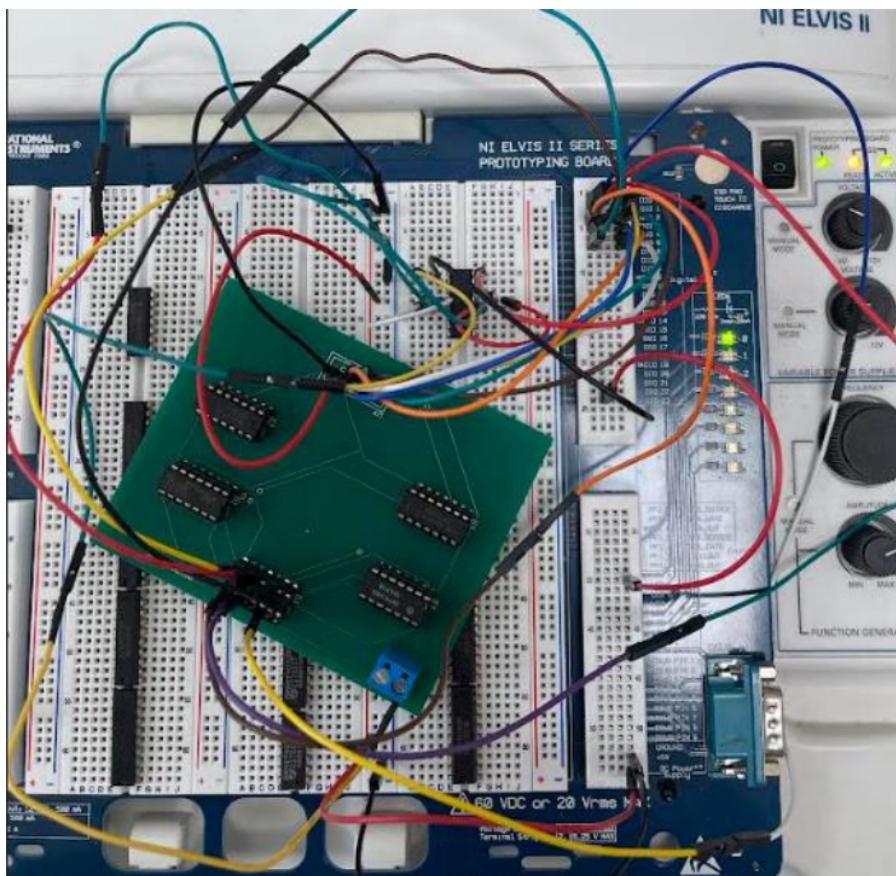


Figure 58: B stuck at 1 PCB

PCB faults have been tested and faults detected

1909752

GRADEMARK REPORT

FINAL GRADE

GENERAL COMMENTS

Instructor

66/100

PAGE 1

PAGE 2

Text Comment. Good detailed table of contents

PAGE 3

PAGE 4

Text Comment. Extensive list of figures

PAGE 5

Text Comment. Summary indicates an understanding of the requirements

PAGE 6

Text Comment. Good significant point made here

Text Comment. An interesting fact supported by an image and ref source

PAGE 7

Text Comment. Good explanation of fault types

PAGE 8

Text Comment. Appropriate application examples

Text Comment. SSF fault types are identified and explained

PAGE 9

Text Comment. Extensive research carried out on this topic.

PAGE 10

Text Comment. This should have a ref source to support the research findings

PAGE 11

Text Comment. There are some good points made in this section

Text Comment. Good research carried out here. An image example would have supported the content

PAGE 12

Text Comment. There should be a ref source for this

Text Comment. This should have a ref source

Text Comment. A good example

PAGE 13

Text Comment. Good preventive examples have been explained

PAGE 14

PAGE 15

Text Comment. Good work. test vectors for gates have been identified

Text Comment. Application of redundancy rules are identified

PAGE 16

Text Comment. Reduced table is correct with redundancies eliminated

Text Comment. Good application of the wildcard rule to further eliminate redundancies

PAGE 17

Text Comment. Good use of alternative ECAD functionality to meet requirements

Text Comment. The X-OR function should be explained

Text Comment. This should be described as a pulse waveform

Text Comment. NFF condition is achieved. This is crucial before the test stages

PAGE 18

Text Comment. Fault condition is set and identified in the output

PAGE 19

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PAGE 20

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PAGE 21

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PAGE 22

Text Comment. Comparison of outputs is explained

Text Comment. Critical NFF state is achieved

PAGE 23

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PAGE 24

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Text Comment. The program functions should be explained

Text Comment. Good use of table

Text Comment. Good schematic design of PCB

Text Comment. The PCB CAM design is missing.

Text Comment. The Gerber files are missing

Text Comment. A good number of ref sources used in research

Text Comment. NFF state is achieved

Text Comment. Three faults have been tested and faults detected

Text Comment. PCB faults have been tested and faults detected

GRADING FORM: CSG-RUBIC

JORDAN REES

0

RESEARCH-INFORMED LITERATURE



Good research carried out with many significant relevant points made. The ref sources demonstrate an extensive researchh carried out.

16/20

KNOWLEDGE AND UNDERSTANDING



A good understanding in all areas has been demonstrated and test vectors have been obtained using SSF methods. 3.5/5 LabVIEW design is correct and includes all test vectors required, however, the program should have been explained, even minimally. 3/5 ECAD alternative methods have been successfully implemented and explained. 3.5/5 CAM development has many parts missing i.e. PCB CAM design and Gerber files with layers. 2/5

12/20

ANALYSIS



ECAD analysis is covered in good detail and explained. The test results are explained enough to demonstrate a good understanding. 7.5/10 Test results confirm the theory. Three faults have been set to check consistency. 3.5/5 Conclusion includes good valid arguments in relection, and a good recommendation. 3/5

14/20

PRACTICAL APPLICATION AND DEP.



Only part of the prototype PCB is covered in the report. 4.5/10 The final prototype test has been carried out with three fault conditions. 6.5/10

11/20

SKILLS FOR PROFESSIONAL PRAC.



Extensive use of softwrae has been demonstrated and is evident in the report. 6.5/10 Report layout is good and in the correct sequence of tasks. There are parts missing and in the wrong section. 3/5 Word count is within limits and good use of appendicies. 3.5/5

13/20