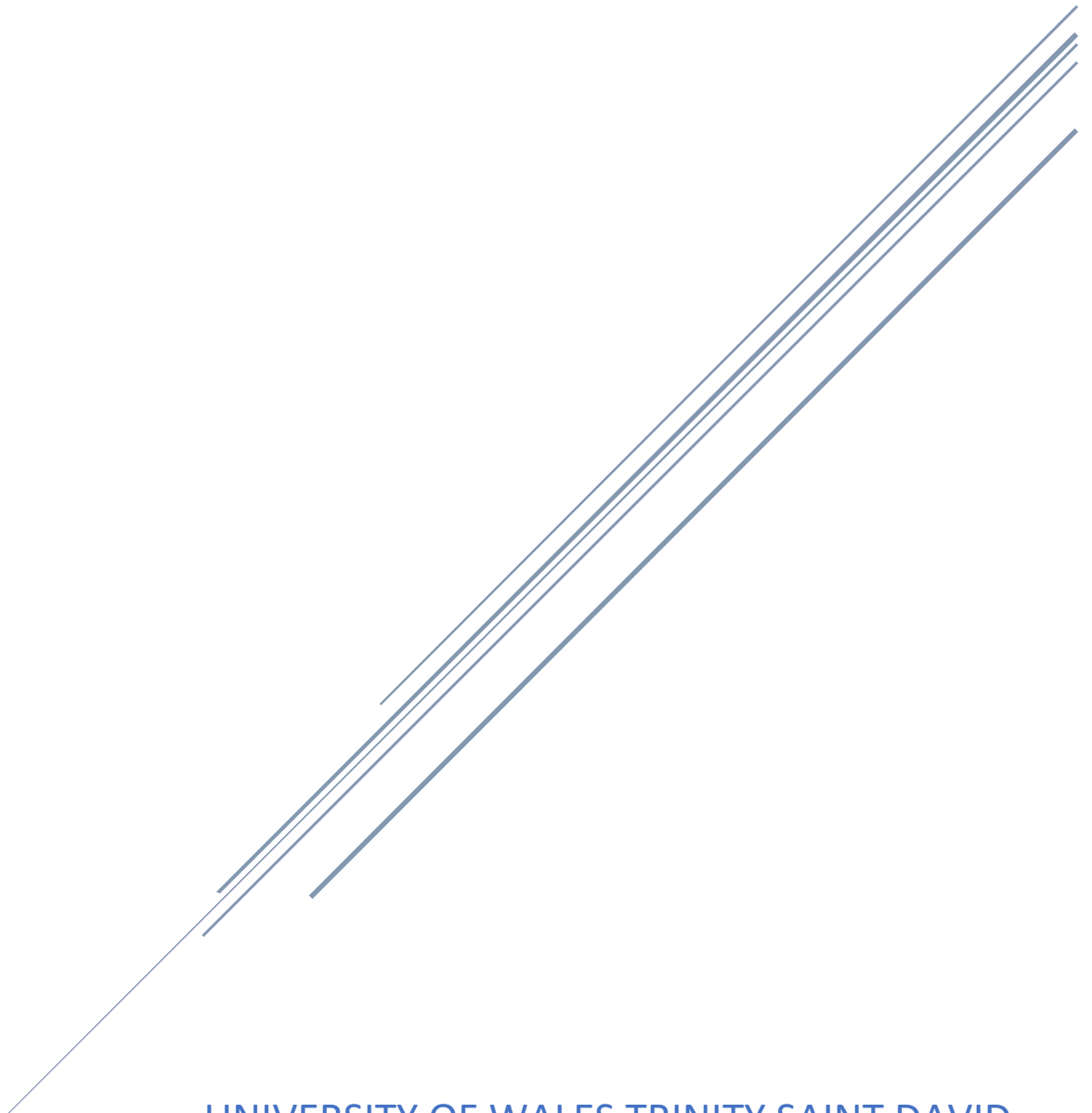


WORK BASED PROJECT

WRITEUP

BY MICHAEL HOWELLS



UNIVERSITY OF WALES TRINITY SAINT DAVID
WORK BASED PROJECT – ACDA5016

CONTENTS

1	ABSTRACT.....	3
2	OVERVIEW.....	4
3	BRIEF	6
4	AUTOPOD OVERVIEW.....	6
5	PINBASE OVERVIEW.....	7
5.1	EXISTING MICROCONTROLLER TEST JIG.....	10
6	AIM.....	12
7	LEGAL AND ETHICAL CONSIDERATION	12
8	PLAN.....	13
9	DESIGN	15
9.1	DESIGN CONCEPTS	15
9.1.1	SINGLE BOARD.....	15
9.1.2	MODULAR CARDS.....	16
9.2	PCB DESIGN	17
TESTING.....		19
9.3	MAIN BOARD DEBUG	19
9.3.1	POWER SUPPLY CIRCUIT	20
9.3.2	SOLID STATE RELAY CIRCUIT	24
9.3.3	MODULE ID CHECK.....	26
9.4	TEST MODULE DEBUG.....	28
9.4.1	POWERING THE MODULE	28
9.4.2	ETHERNET INTERFACE.....	30
9.4.3	EMMC PROGRAMMING CHECK	32
9.5	TESTING THE MICROCONTROLLER PRODUCT.....	34
9.6	MECHANICAL CHECK.....	34
RESULTS		36
REVIEW.....		36
10	APPENDIX.....	38
10.1	TRIPLE TEST JUSTIFICATION CALCULATIONS.....	38
10.2	SCHEMATICS	39
10.2.1	MAIN BOARD(PAGE 1)	39
10.2.2	MAIN BOARD (PAGE 2).....	40

10.2.3	MAIN BOARD (PAGE 3).....	41
10.2.4	MAIN BOARD (PAGE 4).....	42
10.2.5	TEST MODULE (PAGE 1)	43
10.2.6	TEST MODULE (PAGE 2)	44
10.2.7	TEST MODULE (PAGE 3)	45
10.2.8	TEST MODULE (PAGE 4)	46
10.2.9	TEST MODULE (PAGE 5)	47
11	REFERENCES	49

1 ABSTRACT

This document is a writeup that shows the process taken to develop the hardware/software required to create a triple test jig for a microcontroller product manufactured at Sony UK Technology Centre. The test jig design is based off existing hardware that is used in current production test equipment of the product. The outcome of the project was a success as a prototype was created, however some improvements have been noted.

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2 OVERVIEW

Sony UK Technology Centre is a manufacturing facility in South Wales. All products manufactured at Sony go through the same general production process. Firstly, blank PCBs are put through an SMT line where the surface mount components are soldered and checked for placement.

Next, the boards are sent to the main production area where they will go through a test process that will check the functionality of the completed product. Any faulty product detected during testing is sent to a technician who will repair it if possible. Good product is sent to a packing station where it is boxed off ready for shipping to the customer.

The main focus of this project will be around the testing phase of the process for a specific microcontroller. The product name will not be specified in this document.

The test facility for the microcontroller product has gone through two designs currently. The generation 1 test equipment was designed by an external company. However, it had reliability issues affecting the first time yield of the jigs and also the hardware was not to the standard of our current test equipment and so it was redesigned.

Figure 1 shows the original test jig for the microcontroller.

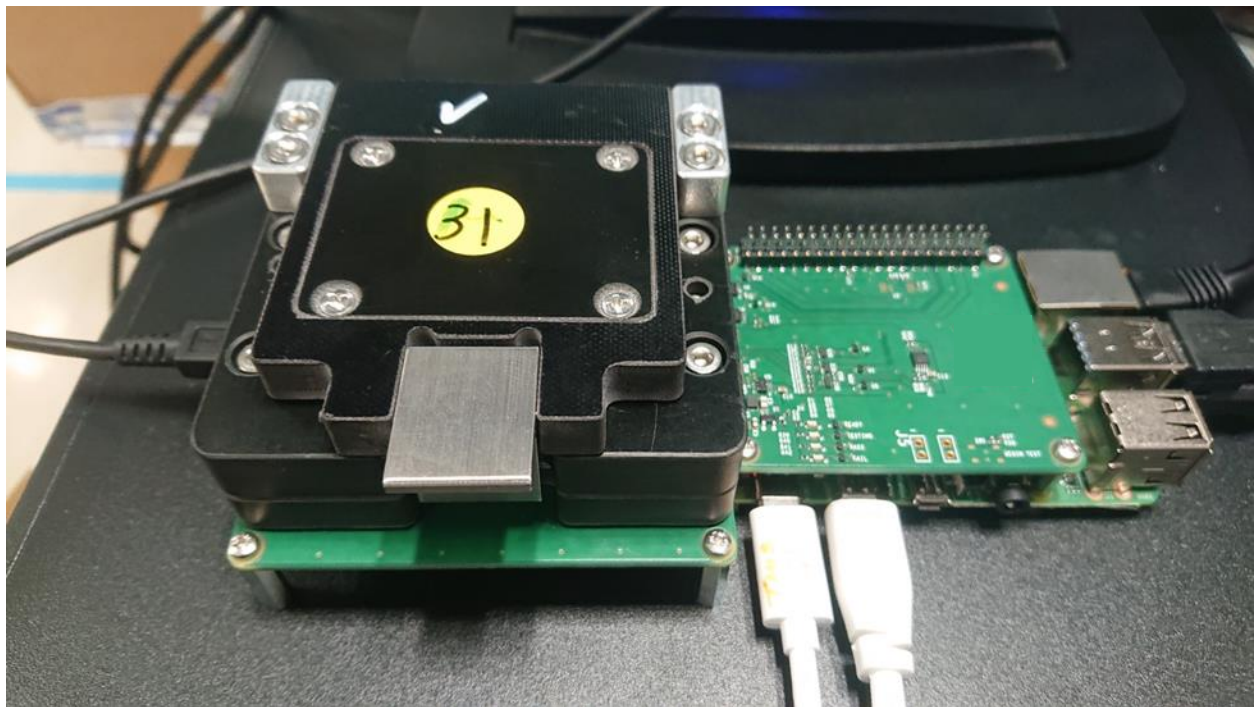


Figure 1 - Generation 1 microcontroller jig (lid down)

Then the lid was raised, a microcontroller could be placed in the testing area where it would interface with the electronics through the pins shown in figure 2.

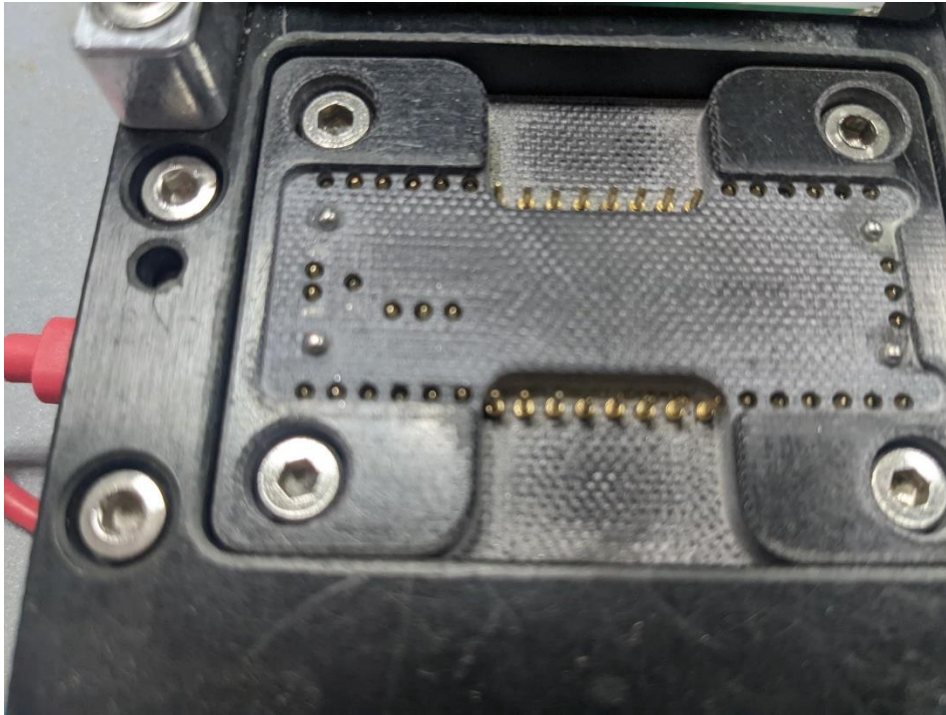


Figure 2 - Generation 1 microcontroller jig (lid up to show pins)

The second generation jig was more in line with the other manual test jigs and the reliability increased greatly. This is shown in detail in section 5.1.

3 BRIEF

The project brief can be defined as:

“Design a test facility for a specific microcontroller product that can be incorporated into existing automation equipment “

4 AUTOPOD OVERVIEW

The existing automation equipment the brief refers to is called an “autopod”, and its function is to load, test and unload product automatically. There are 4 testing areas inside the autopod, and product is continuously fed to each head. An autopod can be seen in figure 3.



Figure 3 – Image of autopod

Each test area has a modular “pin base” containing the test electronic that can be easily removed and changed for different models.

Some sensors and peripheral equipment are installed in the area above the pinbase. This is called a “top hat” and is a modular component that can be swapped out for different models. The top hat also contains plastic pushers that will press the device under test (DUT) into the pinbase to ensure a good connection.

This project will require collaboration with the mechanical engineering team to ensure that the PCBs fit within the form factor of the pinbase and to ensure that everything lines up correctly.

5 PINBASE OVERVIEW

The pinbase is a bed of pins that interfaces to a DUT through its B side, either through the underside of through hole components or through dedicated test points on the board.

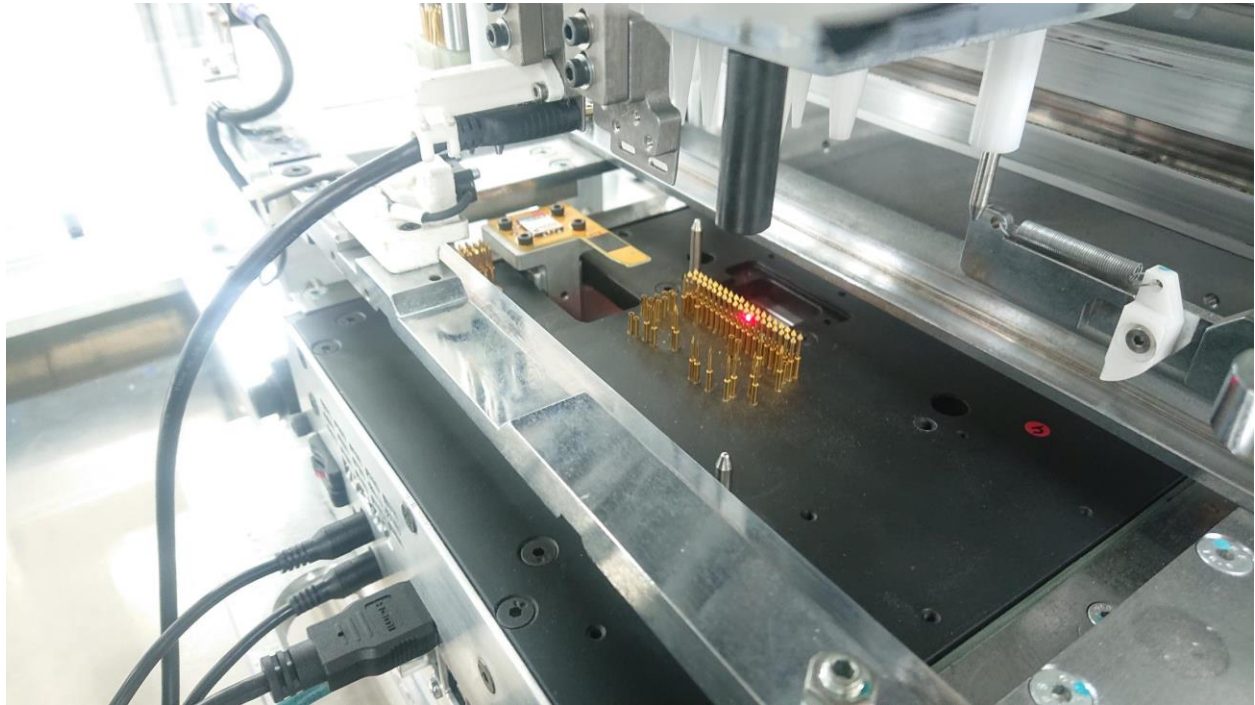


Figure 4 - Image of Sony pinbase bed of pins

There are many different types of pins and each have specific uses. The type of pins that are used in a pinbase are dictated by the product and what it is connected to.

Each pin fits into a receptacle that is mounted into a drilled piece of material that houses all receptacles (black material shown in figure 4). There are different types of pin receptacle.

Some require wires to be soldered to one of their ends (figure 5), however the most common type used on jigs within Sony are spring ended ones. The reason that spring ended pins are used is that they can interface with bespoke PCBs that have exposed pads the springs can connect to. This setup can be seen in figure 6.



Figure 5 - Image of test jig with soldered wire connections to pin receptacles [5]

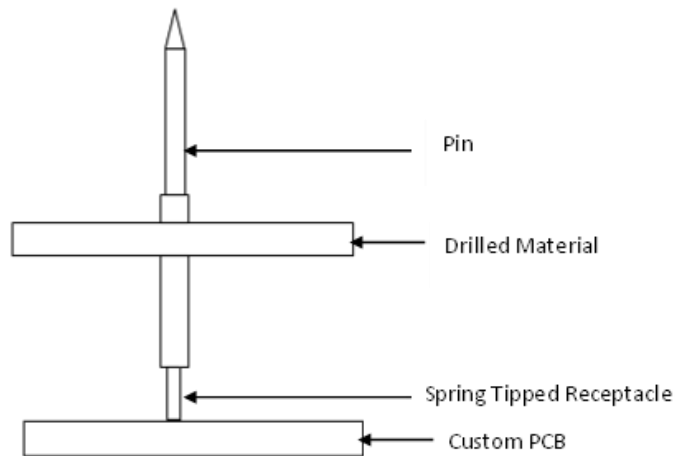


Figure 6 - Example of pinbase pin/receptacle/PCB setup

This setup enables the jig construction to be much simpler as no wires are soldered to the pin receptacles and can speed up jig assembly time. The assembly will also be smaller due to no wires.

The electronics within the pinbase varies between jigs and is dependent on the test requirements for the specific product. Some common features will include:

- Analog to digital converters for voltage measurements
- Controller hardware, often a microcontroller or raspberry pi embedded within the pinbase
- Remote input/output lines.

This document will give an overview for the hardware inside the current pinbase for the single test microcontroller (second generation) product as it will give context in understanding the reasons for certain design choices.

5.1 EXISTING MICROCONTROLLER TEST JIG

The current microcontroller test jig is a single unit tester (figure 7).

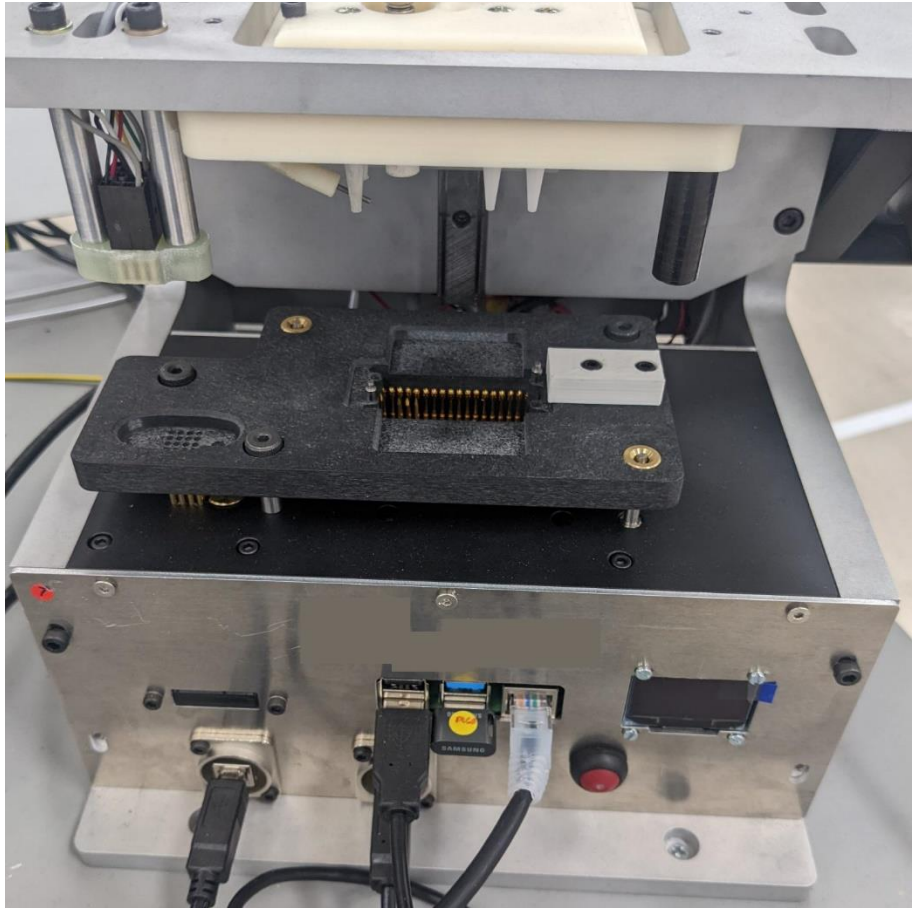


Figure 7 -Generation 2 microcontroller test jig.

The internals of the pinbase contains a raspberry pi and electronics required for testing on a PCB. This includes, ADC ICs, power supply circuits and high side switches. The internals of the generation 2 pinbase can be seen in figure 8.



Figure 8 - Generation 2 test jig internals

6 AIM

The main aim for this project is to develop a working prototype of the test system. This is to confirm the feasibility of the automated test setup. This will require the design and debug of PCBs to be used inside the test equipment and the software that will be run on the jig.

The designed test equipment will be required to meet the following criteria:

- Electronics must fit within a pinbase with a form factor suitable for the autopod.
- Must be able to interface with the product correctly
- The new jig must be able to test the product at an equal level as existing test equipment.
- Must interface with any peripherals on the top of the jig.
- Will be required to trigger PLC controlled features
- Jig needs to meet production quantities on a single shift

7 LEGAL AND ETHICAL CONSIDERATION

No legal or ethical issues were identified during the planning of this project.

8 PLAN

The Gantt chart in figures 9 and 10 shown the schedule for the project.

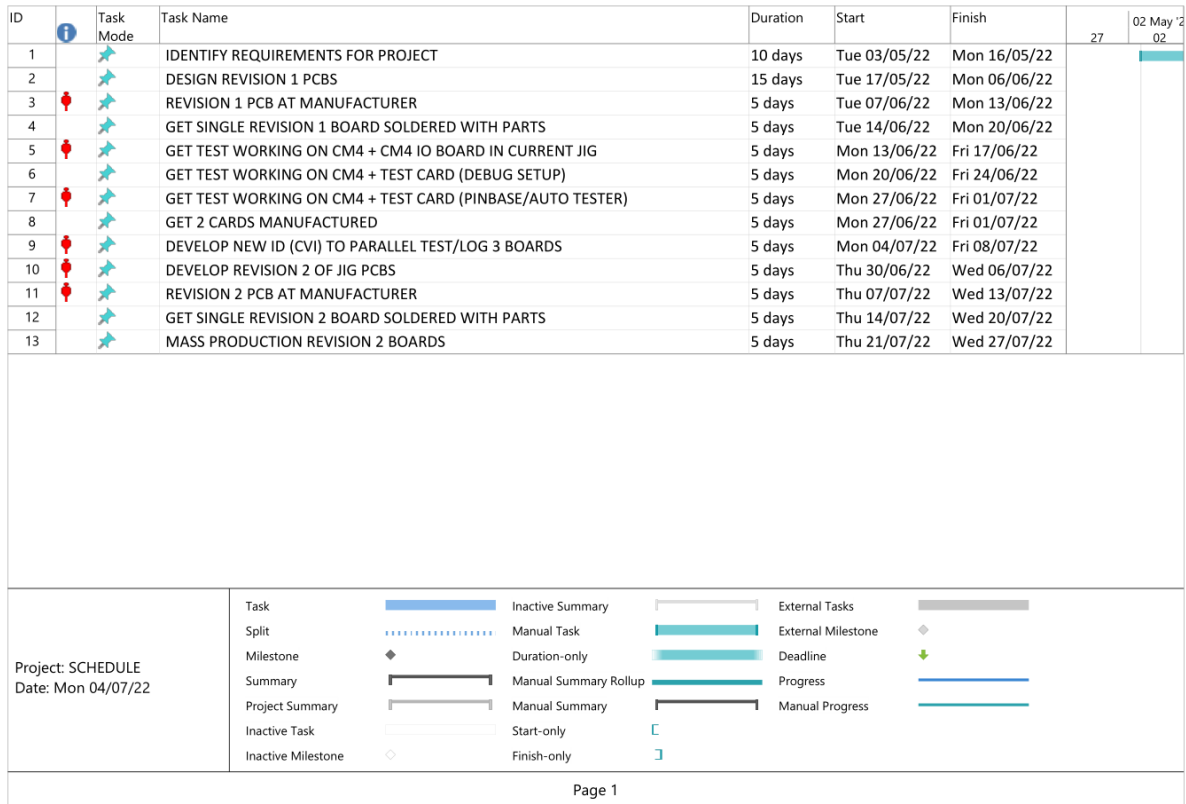


Figure 9 – Project Schedule on part 1

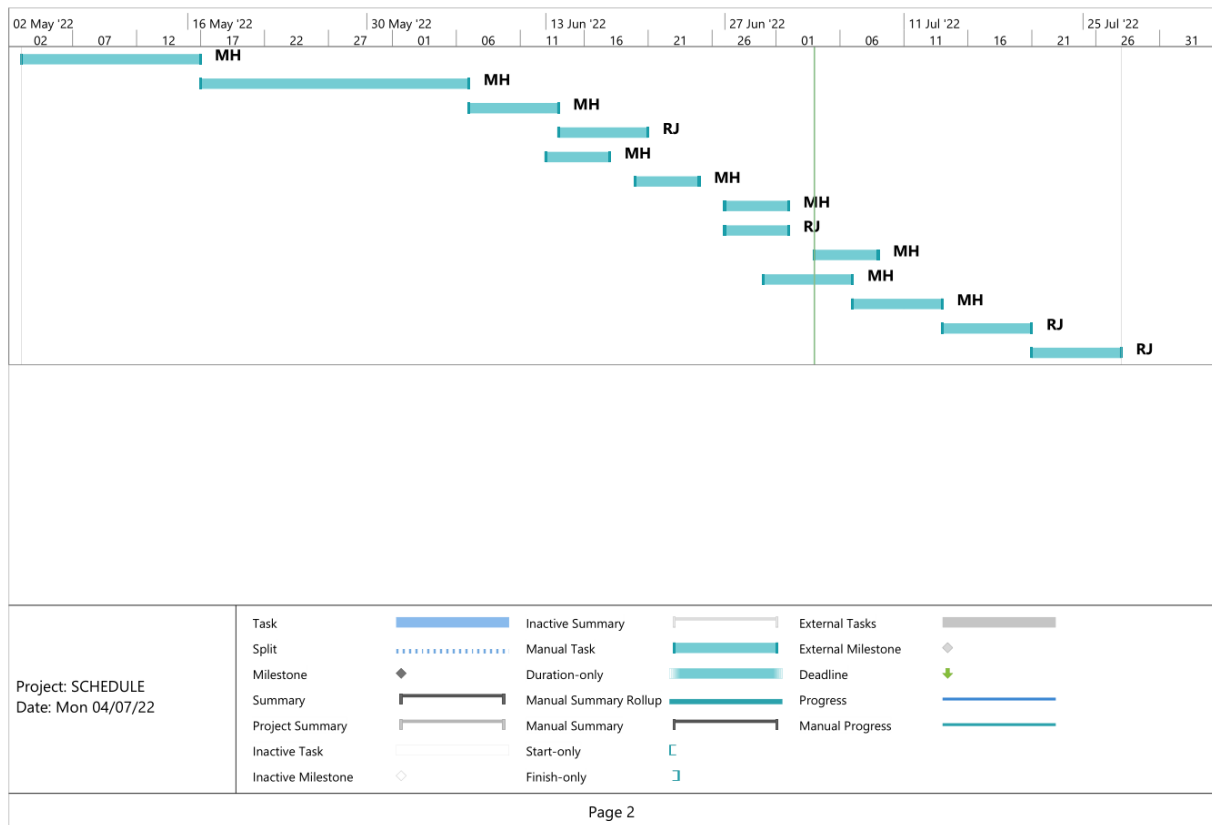


Figure 10 - Project Schedule on part 2

9 DESIGN

The production schedule for the microcontroller was used as a basis for the output requirements of the automation jig. It was decided that a parallel test pinbase would be required to meet production quantities. Calculations in appendix (11.1).

9.1 DESIGN CONCEPTS

Two design concepts were explored in this project. One design philosophy that is constant however is the idea to keep the test electronics as close as possible to the original design. This is to reduce variation and time taken to debug the project because the design is known to be working.

9.1.1 SINGLE BOARD

The first design idea is a single PCB with exactly the same electronics and components as in the original microcontroller test jig. The rough idea can be seen in figure 11.

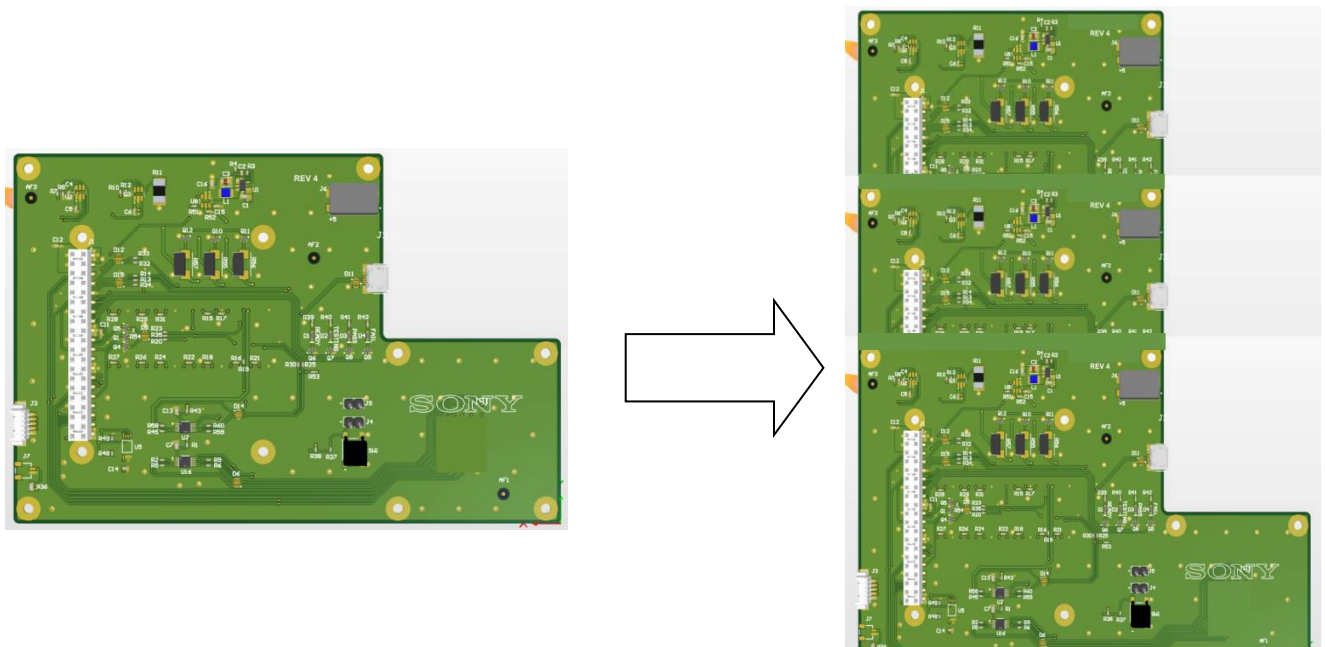


Figure 11 - Single board concept

The main problem with this design is the size that would be required. Each test head would require a raspberry pi which would force the size to be larger than that of the pinbase the jig is required to fit inside of.

Another problem with this design is that if there is a problem with the board while in production, the whole unit will need to be replaced. This could be quite time consuming and could amount to a large amount of jig downtime and loss of production.

9.1.2 MODULAR CARDS

The second design idea was to develop a modular test card that mounts to a main board that has all test points that connect to the pins and interfaces to the product. The main board has 3 connectors that can each house a single test module.

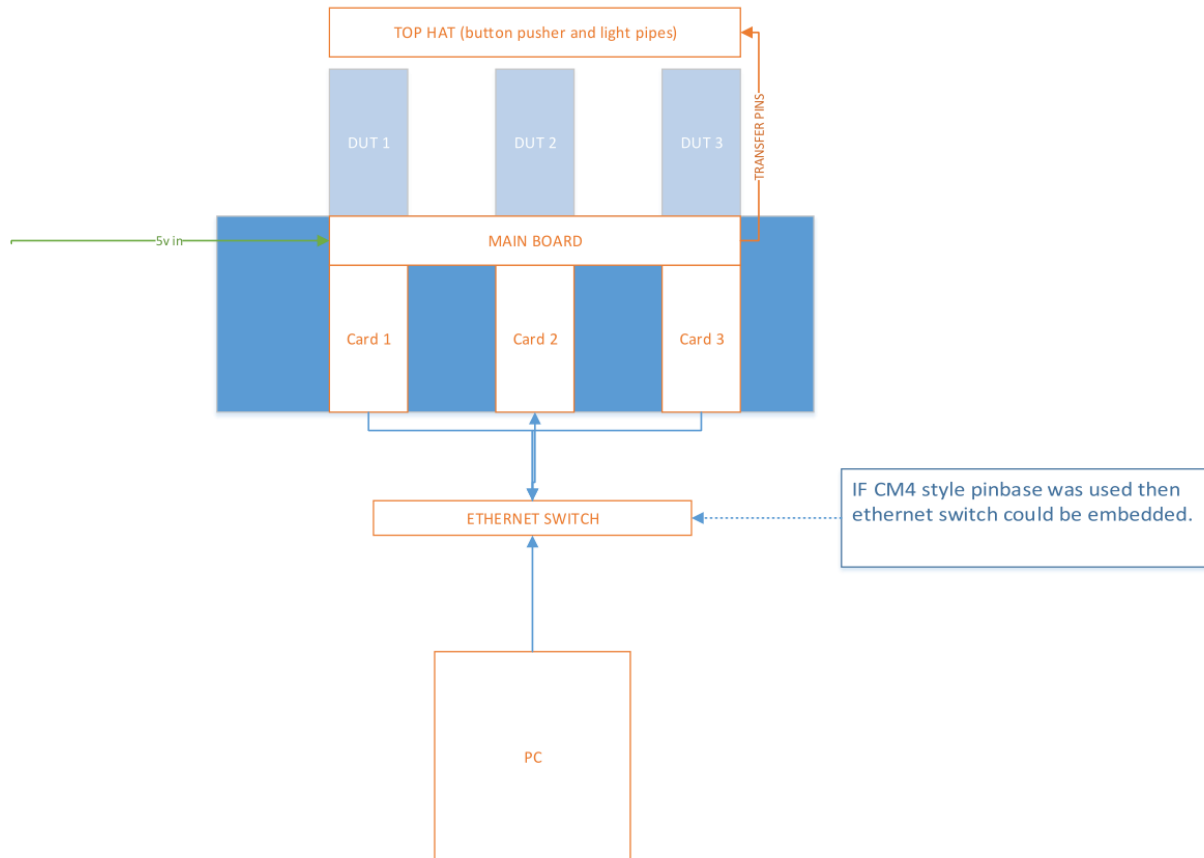


Figure 12 - Modular Triple Test Concept Block Diagram

Figure 12 shows this concept in a block diagram.

Each test module could replace the pi4 with a compute module 4 (CM4). A CM4 is a computer that can be easily embedded into electronics projects. It utilizes the same processor as the pi4 and so the software on the original test jig would be compatible. The CM4 has a much smaller form factor than the pi4 so the hardware can be smaller which is key for this project.

Another benefit of the modular design is that parts are much easier to replace if there is a problem. Both the modular test card and the CM4 could be easily replaced if there is an issue. It also keeps the majority of components off the main board which is the most time-consuming part to replace if there is a problem, so it minimizes the risk.

The modular card design was chosen as the most suitable route for a multi test jig due to the numerous benefits.

9.2 PCB DESIGN

All PCBs designed for this project were completed in Altium Designer which is a PCB design software package. The design for the main board can be seen in figure 14.

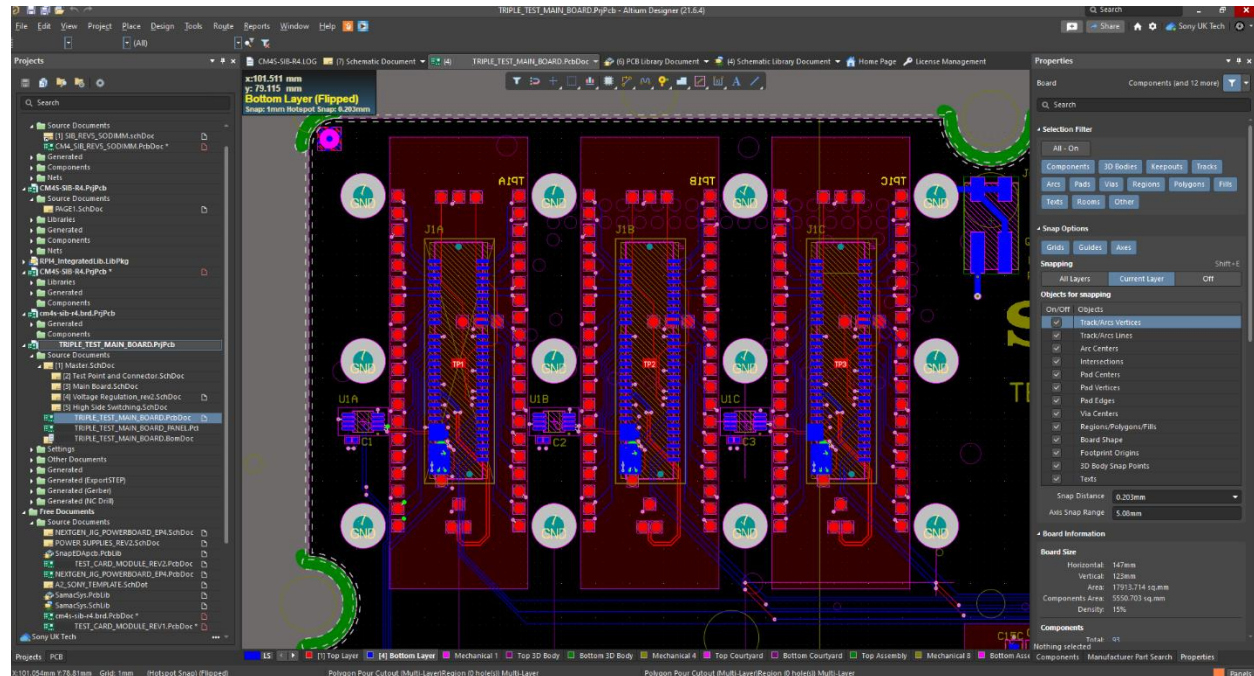


Figure 13 – Main board design in Altium Designer

The first task to complete in any board design is the schematic. A hierarchical schematic design was chosen for the main board. This type of schematic has a master document that allows schematic sheets to be referenced and duplicated. This is useful for the test point to connector connections because they will be required to be duplicated 3 times. The power supply circuit was also duplicated 3 times.

The board layout is the next phase of the PCB design. This stage is where all of the PCB tracks are placed on the design. A PCB board design consists of many 2D layers that specify different aspects of the PCB. For example, both the module and main board will have, top and bottom layers that define the wiring on the board. They are also both 4-layer boards so have a ground plane and power planes. This allows for easier connections to power lines and grounds while reducing the routing on the top and bottom layers. It also improves the current return path as there is a direct path to the power source. There are layers that also define the text displayed on either side of the boards among other things such as the location of solder paste.

The shape of the boards was defined by the mechanical designer using a 2D DXF file. This can be imported into the design and used as the outline of the board. It can also define the location of mounting holes and other key features. This is one instance of collaboration between different departments within Sony.

A large portion of the circuit is a duplication of the original test circuit. The main challenge was to fit it in the small form factor of a card and with the addition of the CM4 parts.

After the design for both boards were completed, they were panelized. This means the single board was put into a panelized design that included multiple copies of the board, waste material, and holes for mounting onto a pasting jig. A panelized board can be seen in figure 15.

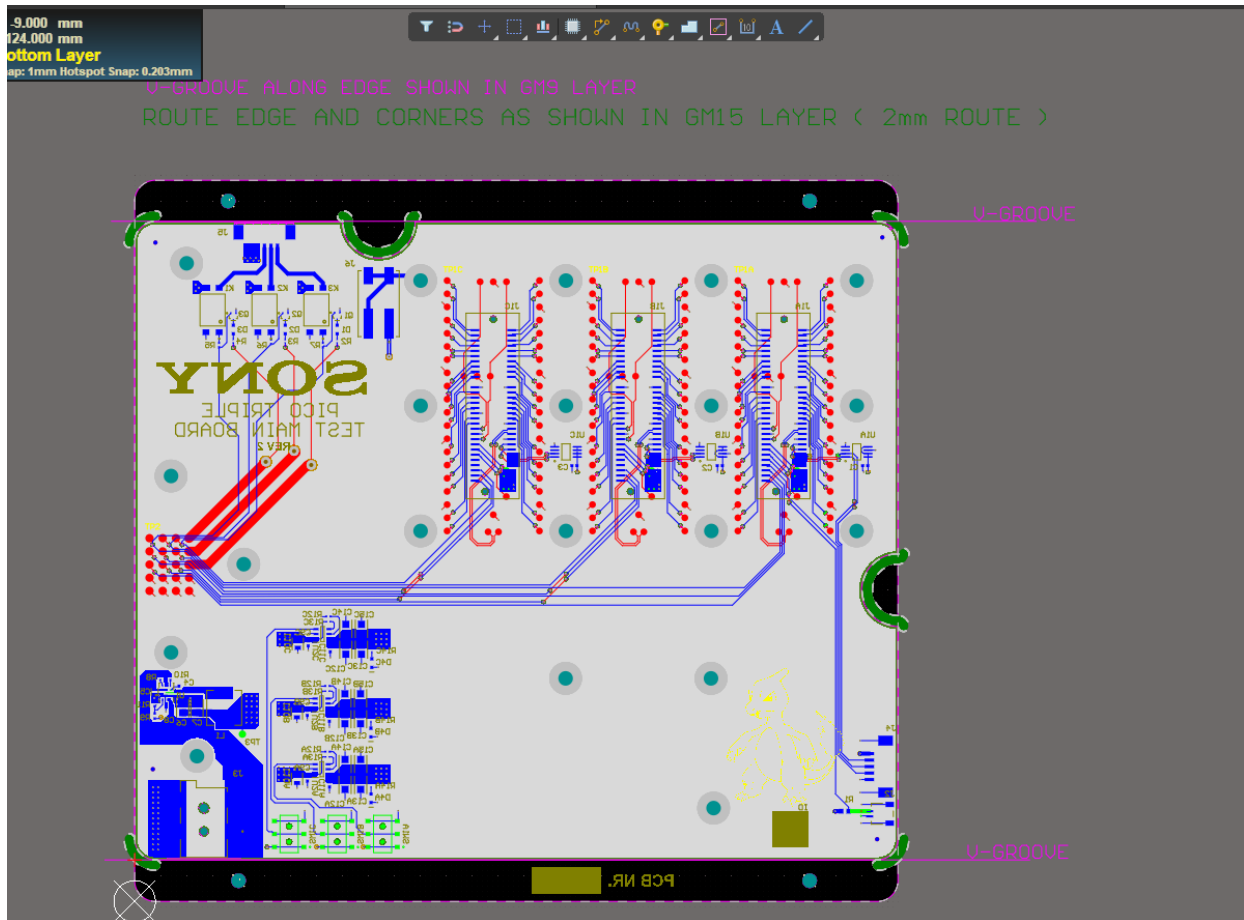


Figure 14 - Panelized main board in Altium Designer

After panelization, the design is exported into formats that the board manufacturer can use. This includes drill files and gerber files. The boards were then sent to the manufacturer.

TESTING

9.3 MAIN BOARD DEBUG

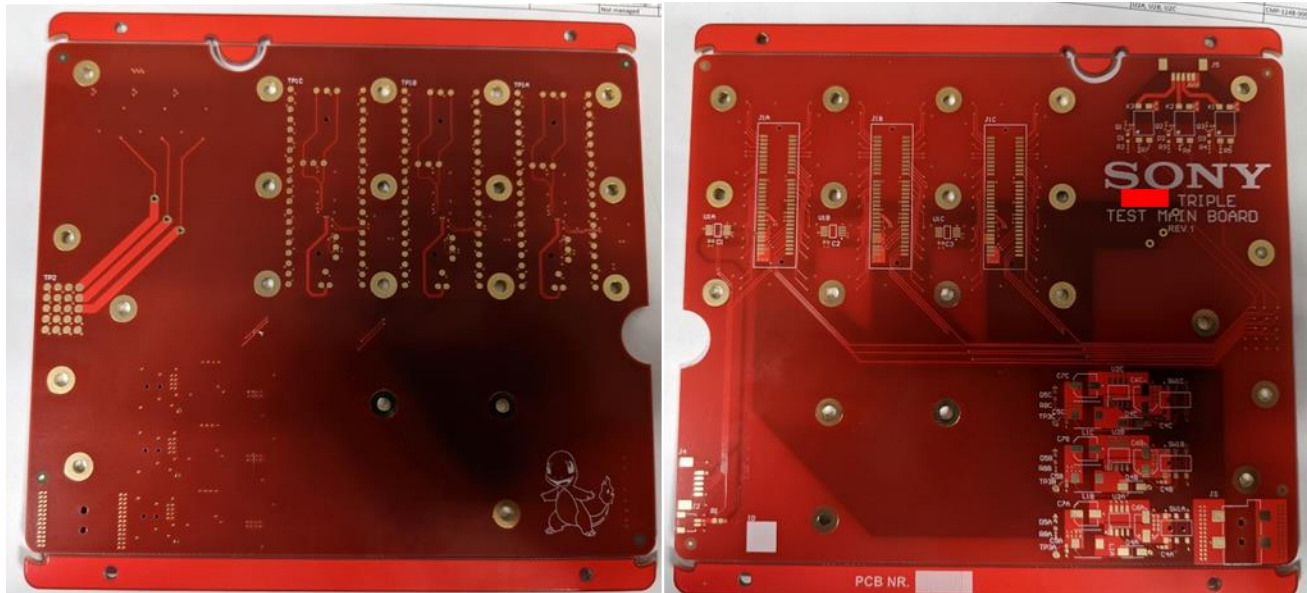


Figure 15 -- Unpopulated Main Board, B side (left) and A side (right)

The first PCB to be debugged is the main board, shown in figure 22. There are 5 main features of this board that must be checked:

- Power supply circuit
- Solid State Relay Circuit
- Test point to edge connector wiring
- Module ID
- OLED / Switch

Only the power supply circuit can be tested easily without a CM4 being present, so this was tested first.

9.3.1 POWER SUPPLY CIRCUIT

The main board contains 3 power supply circuits, one for each module. Only one has been fitted to the board so that the circuit can be tested and if there is a problem with the design then there are no wasted parts.

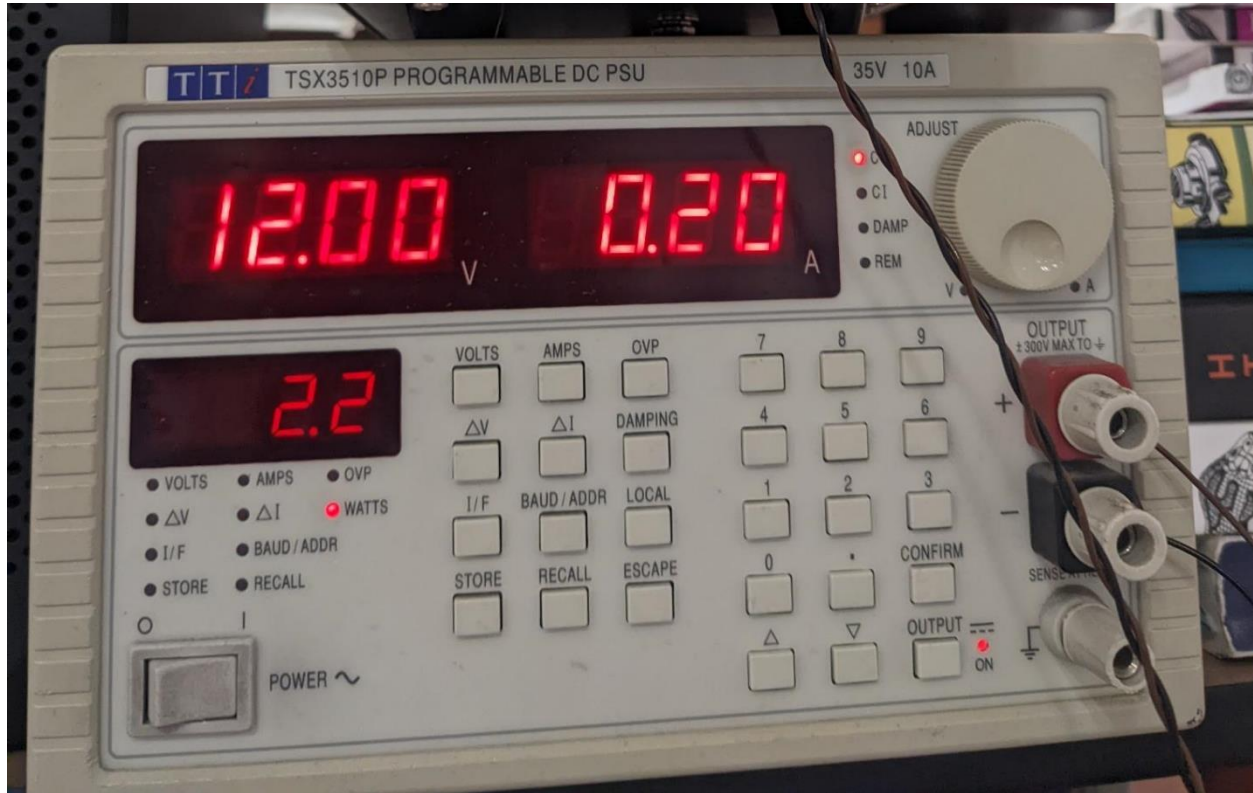


Figure 16 - TSX3510 Programmable DC PSU

The DCDC buck power supply circuit should be able to produce a smooth 5V out using a 12V input. The 12V supply was taken from a TSX3510P Programmable DC PSU shown in figure 23. The current can also be measured using the power supply which could be used to indicate an issue. The circuit was also under load from the CM4 and test hardware module. The current usage was measured at around 500mA, mostly being used by the CM4. To measure the output voltage of the power supply a multimeter was connected to it. 5V was read and which is correct. An oscilloscope was connected to ensure that the output waveform looked correct.

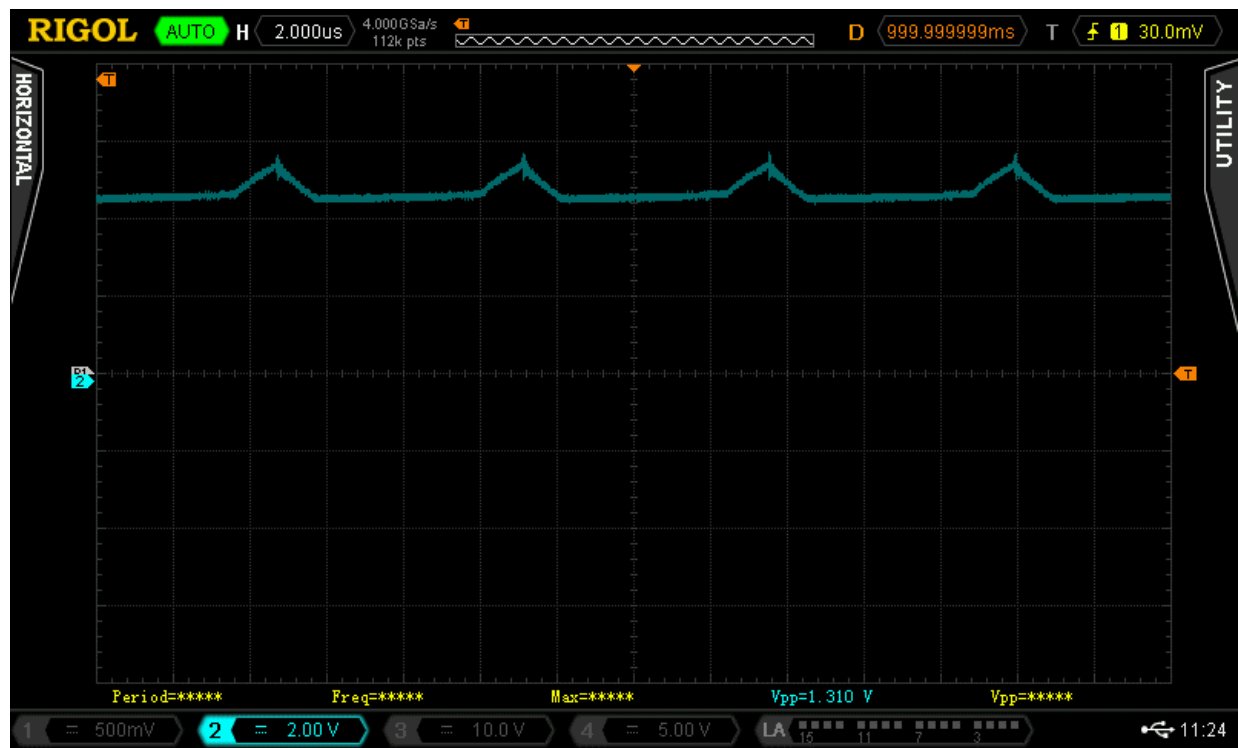


Figure 17 - Main Board Power Supply Voltage Output Measure by Oscilloscope

Figure 24 shows the output voltage of the power supply circuit. The output is a positive voltage with an average of about 5V, however there are lumps in the waveform, which is not desirable. The DCDC buck converter circuit was analysed for any errors in its design within the PCB.

It was identified that C6 was not rated for 12V. This was changed for a capacitor that was rated for above 12V however the lumpy DC was still present.

The smoothing capacitors were also identified to be too small. A C7 was replaced by a larger 470uF capacitor. The output voltage was measured however it was still deemed to be too lumpy (figure 25).

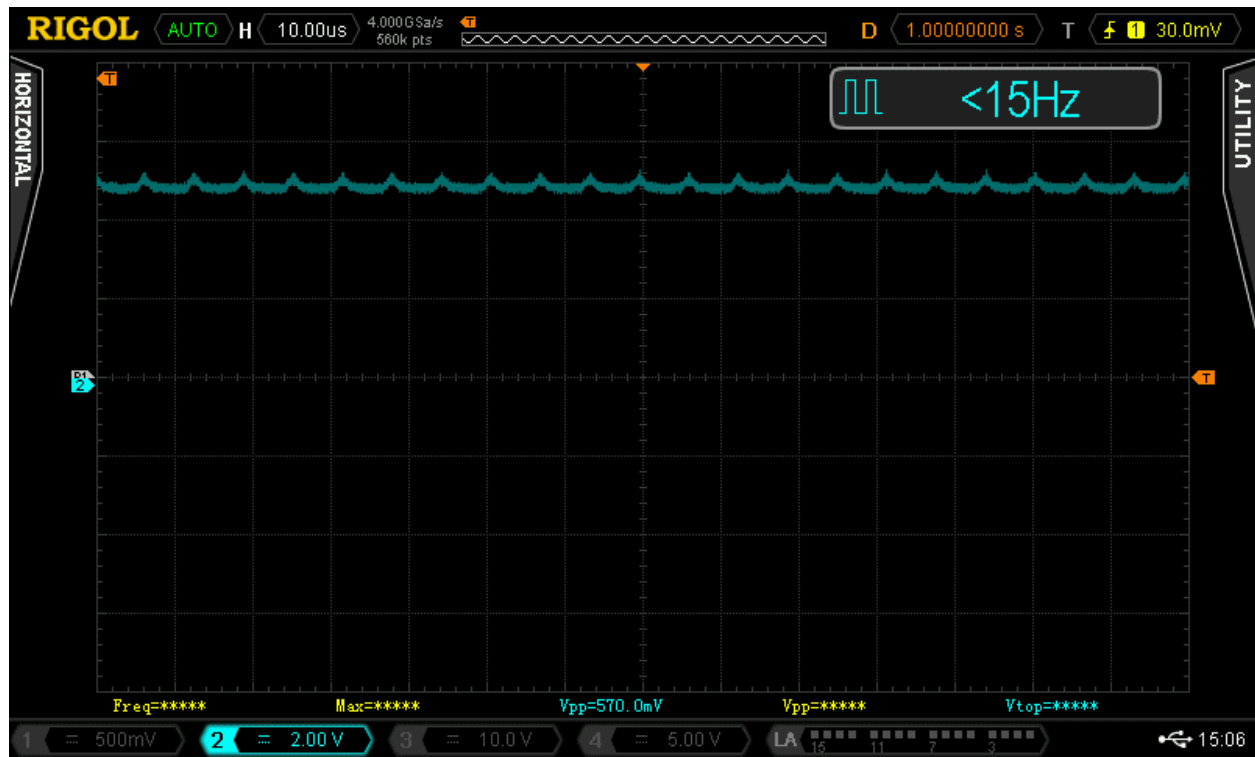


Figure 18 - Main Board Power Supply Voltage with C7 as 470uF

To get a good reference of a power supply output, the voltage of a CM4 IO powered by 12V was measured. The circuit was also under load with a CM4 being connected and using about 500mA. The DC output was very smooth (shown in figure 26).

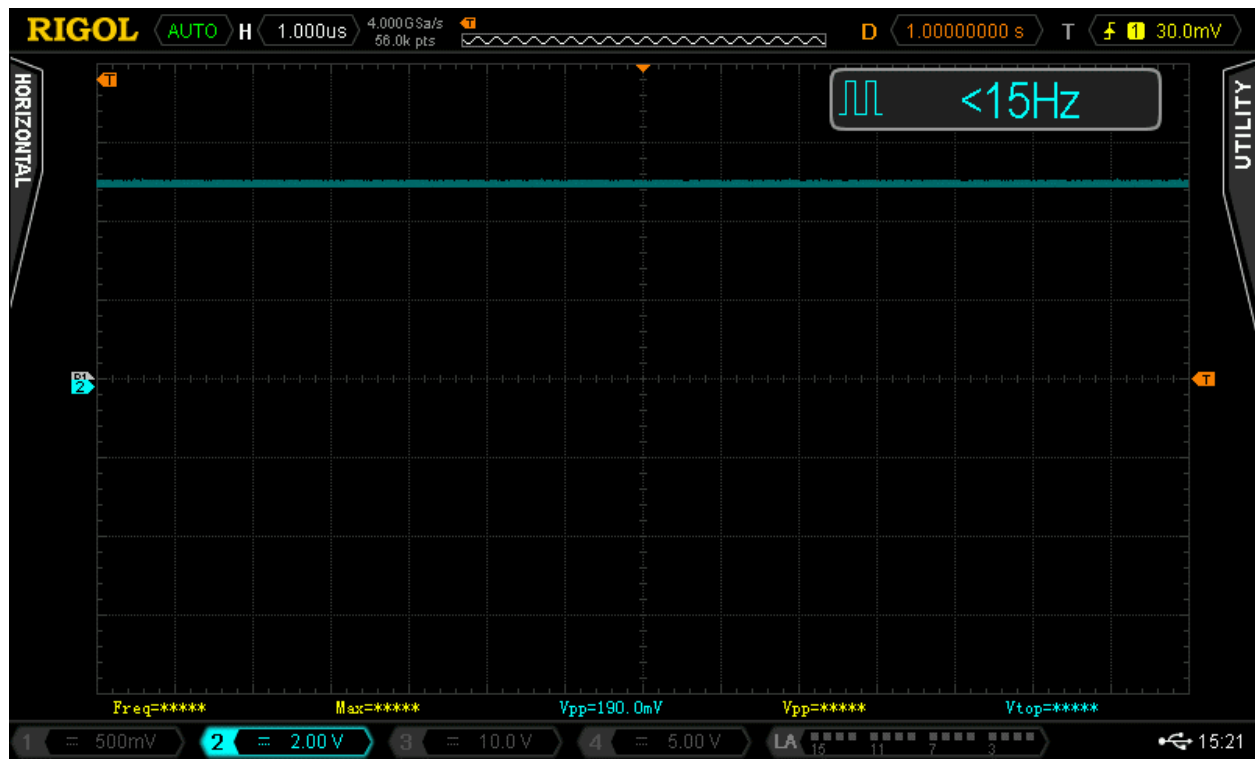


Figure 19 - CM4 IO PSU Circuit Output

The inductor in the buck converter circuit was also identified as being too small. The correct size inductor was calculated; however, its size was much larger than the current one. This was due to the switching frequency of the buck converter IC. If a buck converter IC that switches at a higher frequency was used, then a smaller inductor could be used and more space on the board could be saved. As space is very limited in this part of the circuit it was decided that this circuit was not suitable. An alternate circuit will be designed in revision 2. As the lumpy 5V is capable of powering the circuit, it will be used for the continued debug of the project.

9.3.2 SOLID STATE RELAY CIRCUIT

The solid state transistor circuit was tested after the test module. This was because the CM4 was required to toggle the IO line high and low.

The desired functionality of this circuit was for the switched side of the relay to go high as low as the GPIO changes state. To test this, a small python script was written to toggle the GPIO line high and low, and the switched line of the relay was measured using an oscilloscope. 24V from a separate power supply was connected to the common line of the relay.

Figure 27 shows how the oscilloscope was connected to the switched line of the relay.

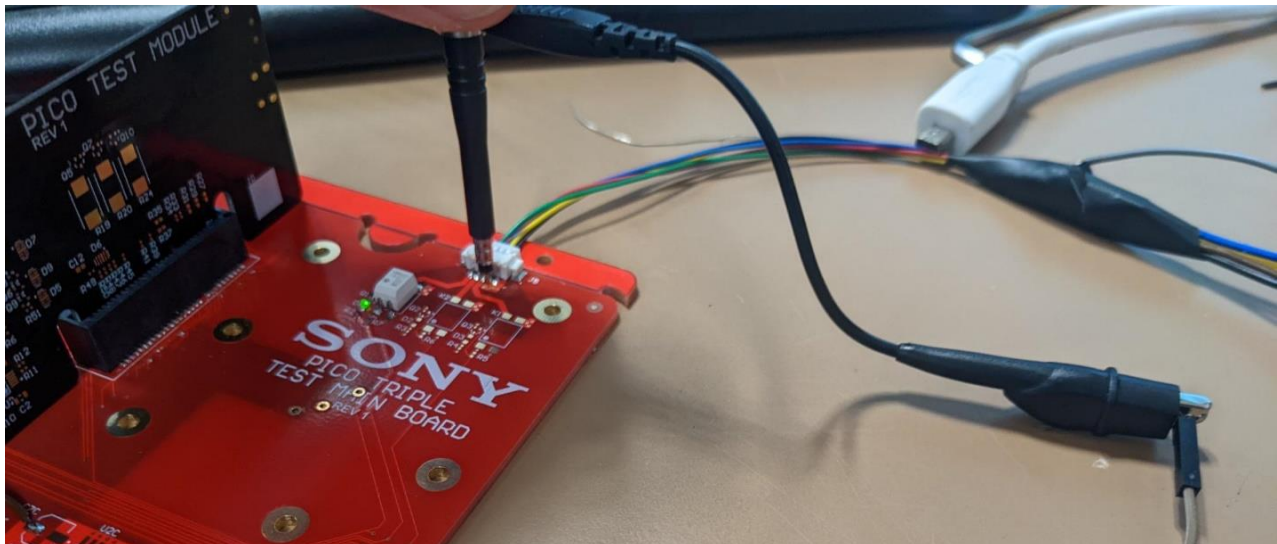


Figure 20 - Solid State Relay Test Setup

Figure 28 shows the square wave measured on the oscilloscope as the line was switched high and low. There were no problems with this part of the circuit, and it worked as expected.

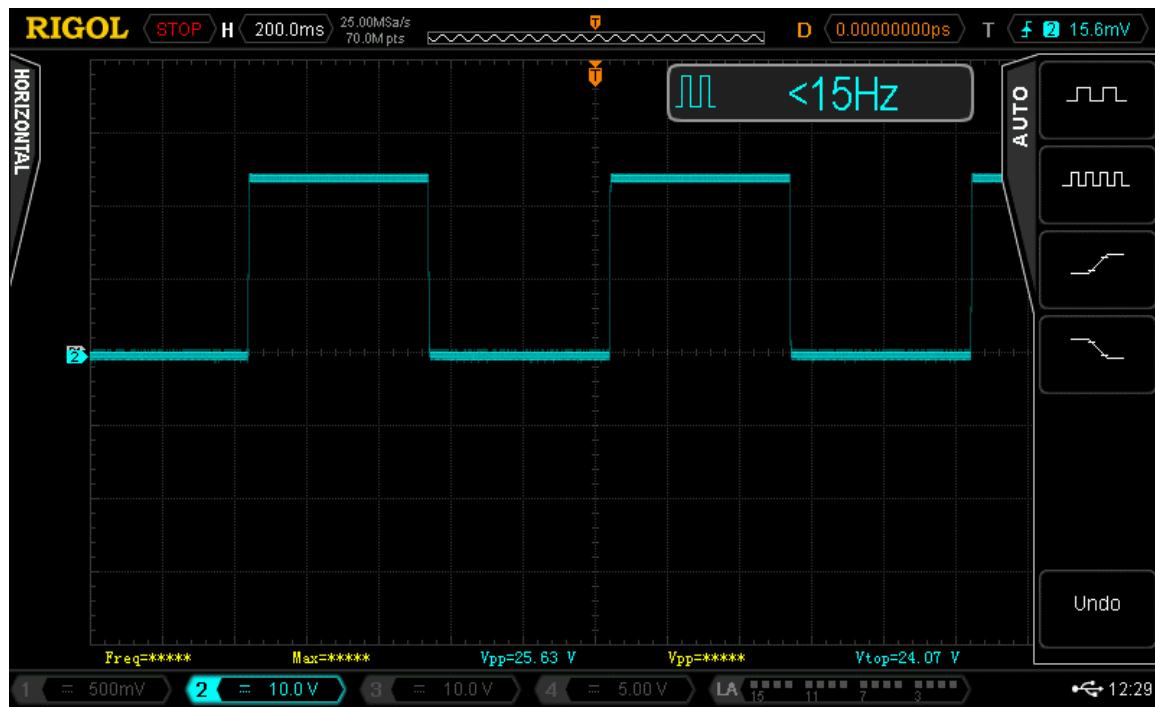


Figure 21 - Solid State Relay Oscilloscope Reading

9.3.3 MODULE ID CHECK

The module ID check is to ensure that the CM4 in the test module can read the uniquely addressed I2C device at each position (U1A, U1B and U1C shown in figure 28).

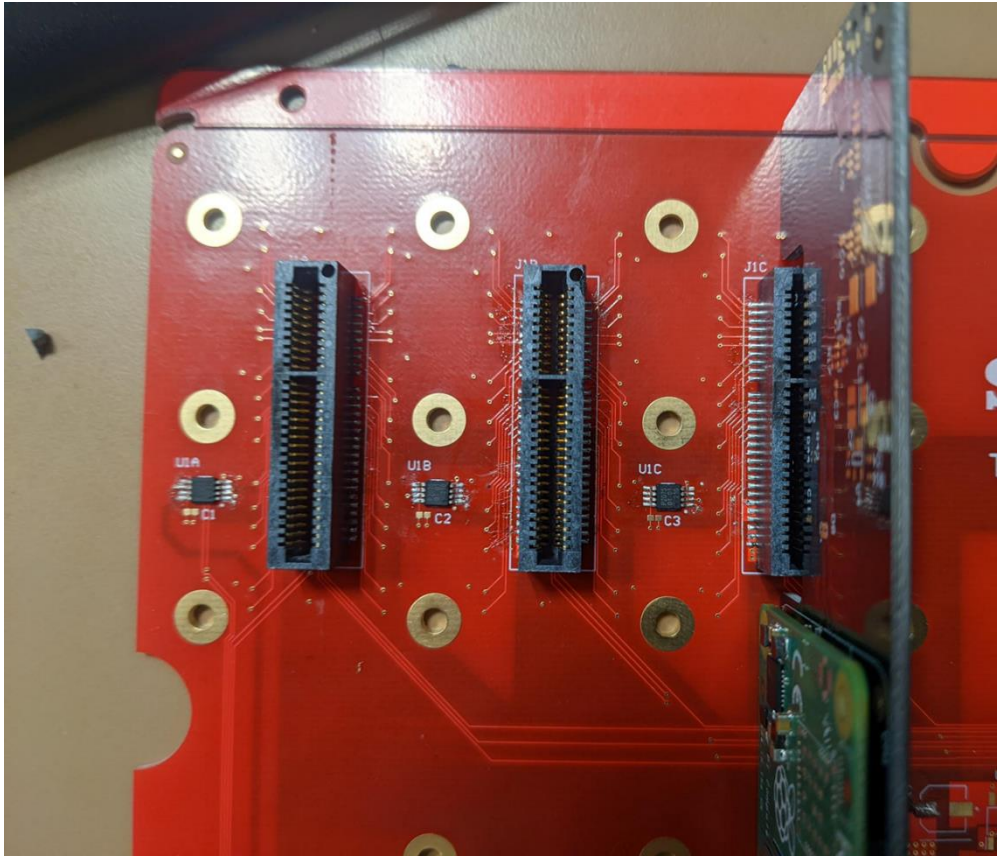


Figure 22 - I2C IC on main board

To check this functionality, the test module was placed into each position and the I2C bus was read to confirm the expected device detected. The command “i2cdetect -y 1” was used on the CM4 module to check the I2C bus. The results can be seen in figures 29, 30 and 31.

```
pi@raspberrypi: ~  
File Edit Tabs Help  
pi@raspberrypi:~$ i2cdetect -y 1  
 0  1  2  3  4  5  6  7  8  9  a  b  c  d  e  f  
00:  --  --  --  --  --  --  --  --  --  --  --  --  --  --  --  
10:  --  --  --  --  --  --  --  --  --  --  --  --  --  --  --  
20:  --  --  --  --  --  --  --  --  --  --  --  --  --  --  --  
30:  --  --  --  --  --  --  --  --  --  --  --  --  3d  --  --  
40:  --  --  --  --  --  --  --  --  --  --  --  --  4d  --  --  
50:  --  --  --  --  --  --  --  --  --  --  --  --  --  --  --  
60:  --  --  --  --  --  --  --  --  --  --  --  --  --  --  --  
70:  --  --  --  --  --  --  --  --  --  --  --  --  --  --  --
```

Figure 25 - The device in position 1 (4d) was detected successfully

```
pi@raspberrypi: ~  
File Edit Tabs Help  
pi@raspberrypi:~$ i2cdetect -y 1  
 0  1  2  3  4  5  6  7  8  9  a  b  c  d  e  f  
00:  --  --  --  --  --  --  --  --  --  --  --  --  --  --  --  
10:  --  --  --  --  --  --  --  --  --  --  --  --  --  --  --  
20:  --  --  --  --  --  --  --  --  --  --  --  --  --  --  --  
30:  --  --  --  --  --  --  --  --  --  --  --  --  --  --  --  
40:  --  --  --  --  --  --  --  --  --  --  --  --  4e  --  --  
50:  --  --  --  --  --  --  --  --  --  --  --  --  --  --  --  
60:  --  --  --  --  --  --  --  --  --  --  --  --  --  --  --  
70:  --  --  --  --  --  --  --  --  --  --  --  --  --  --  --
```

Figure 24 - The device in position 2 (4e) was detected successfully

```
pi@raspberrypi: ~  
File Edit Tabs Help  
pi@raspberrypi:~$ i2cdetect -y 1  
 0  1  2  3  4  5  6  7  8  9  a  b  c  d  e  f  
00:  --  --  --  --  --  --  --  --  --  --  --  --  --  --  --  
10:  --  --  --  --  --  --  --  --  --  --  --  --  --  --  --  
20:  --  --  --  --  --  --  --  --  --  --  --  --  --  --  --  
30:  --  --  --  --  --  --  --  --  --  --  --  --  --  --  --  
40:  --  --  --  --  --  --  --  --  --  --  --  --  4f  --  --  
50:  --  --  --  --  --  --  --  --  --  --  --  --  --  --  --  
60:  --  --  --  --  --  --  --  --  --  --  --  --  --  --  --  
70:  --  --  --  --  --  --  --  --  --  --  --  --  --  --  --
```

Figure 23 - The device in position 3 (4f) was detected successfully.

Each module worked exactly as intended and will be used to automatically configure the IP address of the CM4 module at boot based on its position on the main board.

9.4 TEST MODULE DEBUG

The test module is the most complicated part of this project and contains circuit required for testing the microcontroller product and also for the CM4 embedded computer. The main features that will be tested in to confirm its operation is:

- Powering the module
- Ethernet interface
- Microcontroller Test Hardware
- EMMC disable switch
-

9.4.1 POWERING THE MODULE

The first problem identified with the test module was found when trying to power it up. When the module was connected and power was applied, the voltage would suddenly drop. This was discovered to be a connection between the 5V and ground nets. The voltage drop was caused by the low resistance at the short causing a high current, more than the power supply was rated for and so the voltage is decreased to prevent damage.

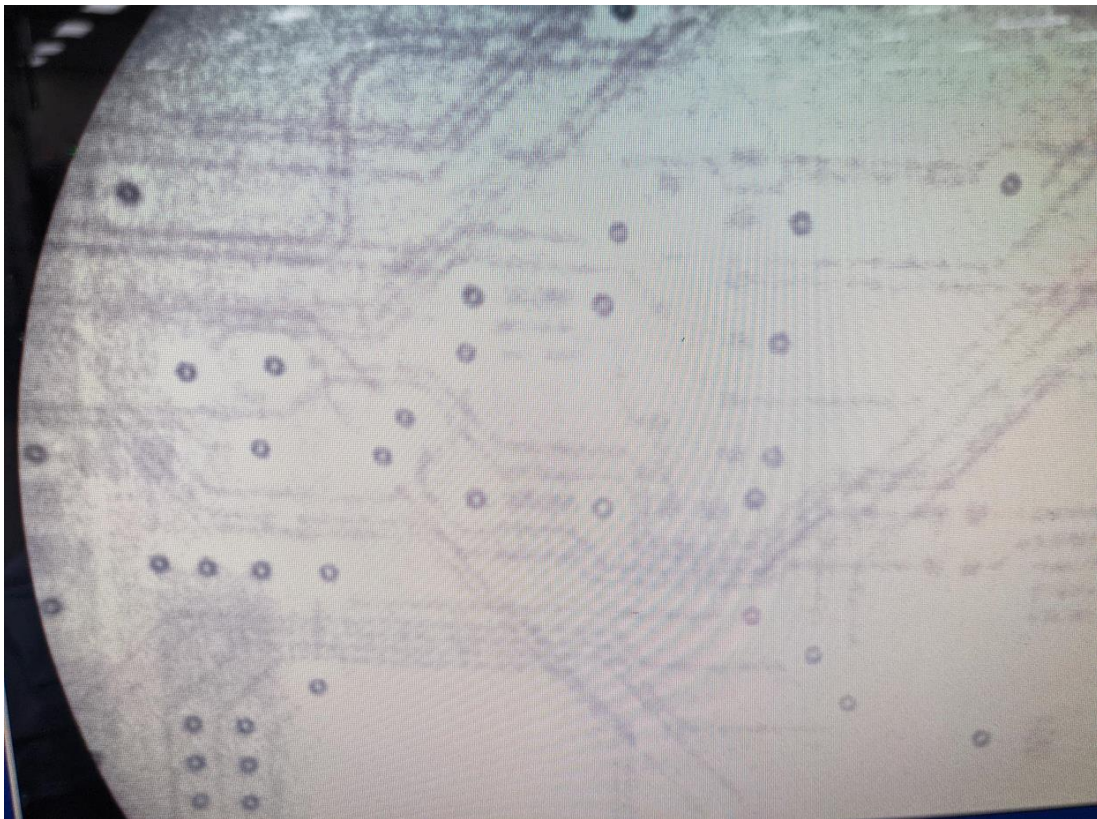


Figure 26 - X ray of test module PCB

After a visual inspection of the board, the short could not be identified. The board was x-rayed., however the image was unclear..

After reviewing the design files and running the rule checking. The short was identified. A 5V via was intersecting a ground trace. In order for this error to be overcome, the PCB was modified by cutting tracks and adding mod wire.

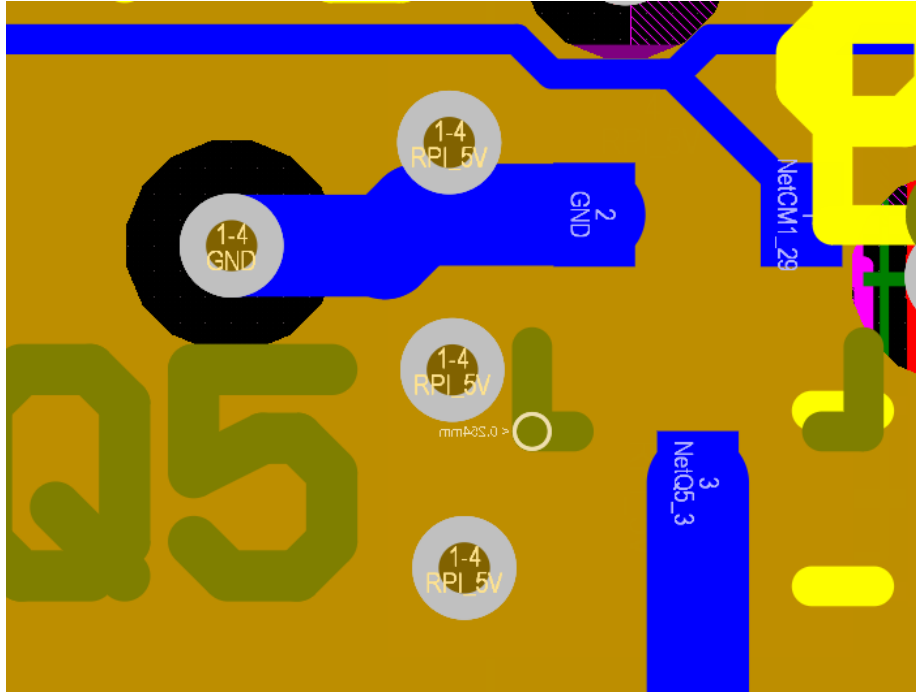


Figure 27 - Identified short on test module PCB

The design was modified in Altium so the next revision of the board would not have this issue.

After the board was modified, the module was able to be powered and the voltage would not drop below 5V.

9.4.2 ETHERNET INTERFACE

To test the ethernet interface a CM4 was loaded onto the two 100 pin connectors and power was applied. The CM4 booted but the PC was unable to connect to the CM4 on the test module.

The CM4 was powered up on a CM4 IO board and the ethernet interface was confirmed to be working as the PC could access the CM4 through VNC [1]. This confirmed that the problem was with the hardware on the test module.



Figure 28 - Image of CM4 on CM4 IO board with ethernet connected

After reviewing the datasheet for the ethernet connector used on the test module card and comparing it to the design, it was identified that the footprint used for the part was incorrect and the pinout was backwards.

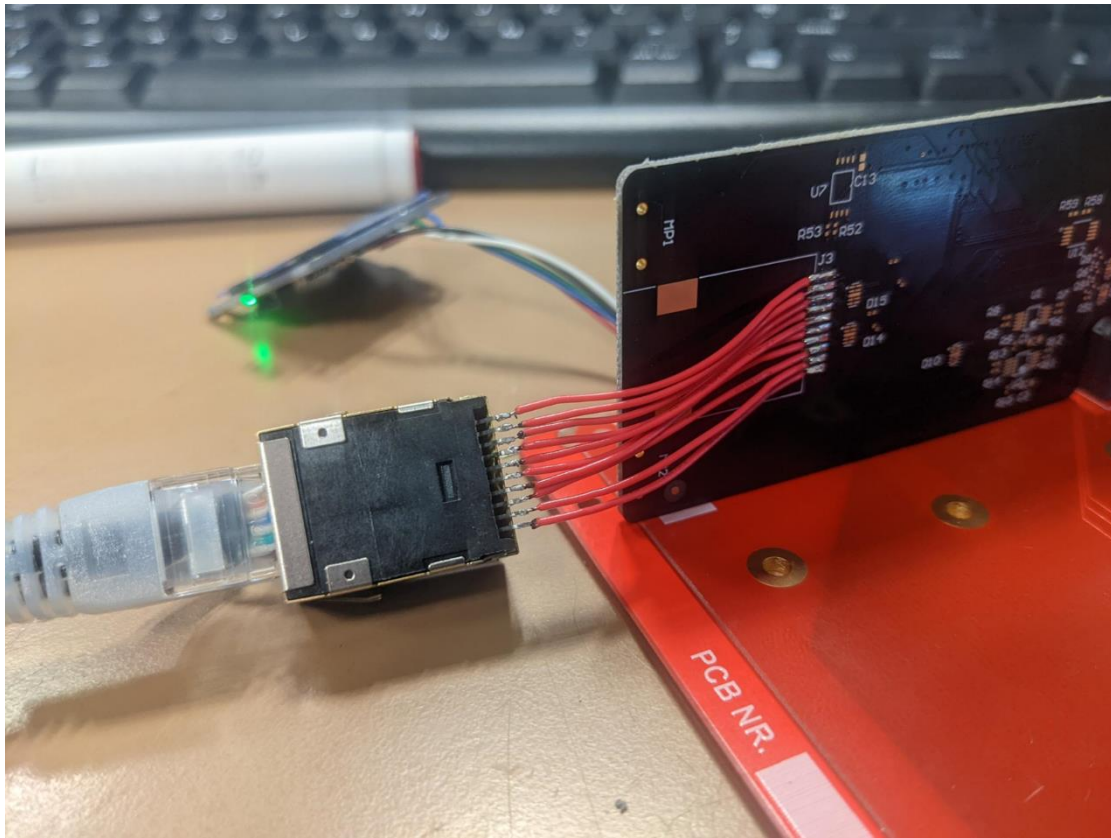


Figure 29 - Image of modification to connect ethernet correctly

The board was modified to reverse the pinout with mod wires and the ethernet interface then worked.

9.4.3 EMMC PROGRAMMING CHECK

On the test module, there is a switch that can be toggled to disable the EMMC boot. This is to be used so that the EMMC on the CM4 can be programmed when inside the pinbase, using the micro-USB connector on the module.

The same steps for programming the CM4 EMMC shown previously can be repeated. However, when it was attempted, the EMMC was not visible to the computer and windows displayed an error, shown in figure 36.



Figure 30 - USB device error

Firstly, the VCC line was checked and 3V3 was measured. Then the USB select line was checked, which should be 2.5V when then slave was connected (micro-USB used for programming program). This voltage was measured and was correct. Next, the circuit was reviewed for errors.

Figure 37 shows the circuit used around U12, which is a multiplexer for USB data lines. In this design, it is used to switch between the USB of the microcontroller under test and the slave USB data lines used for programming, when 5V is present on the slave USB bus. Pin 8 and 9 have been wired backwards and the positive and negative lines of the differential pair have been reversed.

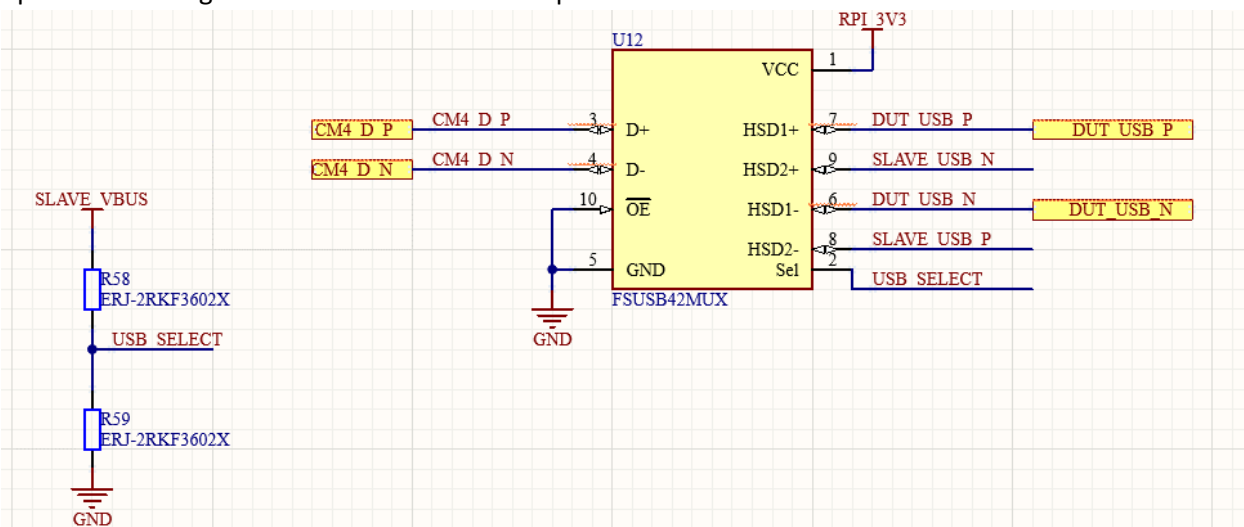


Figure 31 – USB multiplexer wiring, used to switch in USB line for programming

To test if this was the cause of the USB malfunction detected by the PC, the USB data lines on a USB cable were reversed and the programming was attempted again.

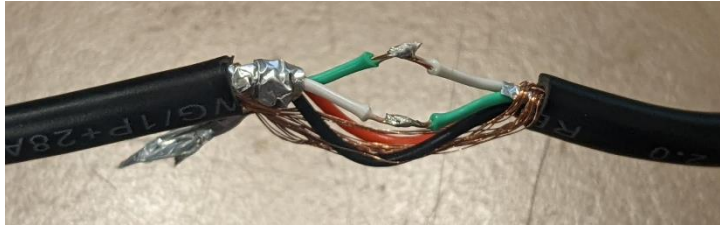


Figure 32 - Reversed cable for testing

Figure 38 shows the reversed data lines on a micro USB cable used for this test.

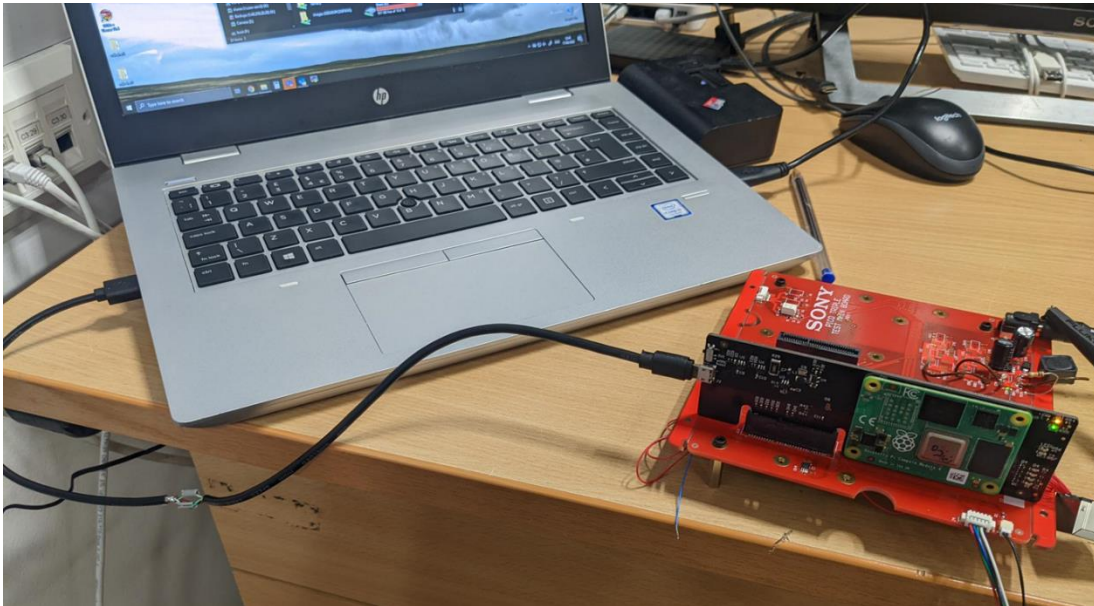


Figure 33 - CM4 EMMC programming setup using test module and modified cable

Figure 39 shows the setup used for programming the CM4s EMMC. After the modified cable was used, the EMMC could be detected by the PC without error. This proves that the reversed data lines were the cause of the issue.

9.5 TESTING THE MICROCONTROLLER PRODUCT

At the time the boards were ready to test the microcontroller product, the pinbase was not ready. To prevent a halt of progress while waiting for the pinbase mechanics, a method of testing a microcontroller was devised.

A single microcontroller was soldered to the test points on the underside of the board. This allowed the PCBs to interact to it as if it were inserted into a pinbase.

The test script was run on the board and passed without any problems.

9.6 MECHANICAL CHECK

To confirm that the PCBs fit into the mechanical pinbase correctly, parts were soldered onto the blank board and installed. The purpose of this is to confirm that all parts line up correctly to holes drilled in the front plate. The boards installed are not functionally working but will be used as a mechanical reference.



Figure 34 - Main board fitted into pinbase bottom

Figure 40 shows that the main board fits into the bottom of the pinbase correctly. All holes line up for mounting the board. The DC power jack also lines up with the hole on the front panel.

On the test module, both the ethernet and mounting holes line up with the front panel holes correctly. No issues were detected with the mechanical alignment.



Figure 35 - Alignment of mounting holes and ethernet on front panel of pinbase

RESULTS

The main outcome of this project was a working prototype design that is capable of testing the microcontroller product. There were several issues detected during the debug however all had countermeasures that were either implemented physically on the board with mod wire or were understood so that they could be implemented on the next revision of board.

The successful design of a card containing the electronics required to test the microcontroller in a much smaller form factor is a key part of this automation project. It has proven that the triple test jig idea is feasible, and this is one of the main aims of this project.

The developed project met all the criteria defined in the aims section.

REVIEW

Although the outcome of the project was a success, there were some things that could have been done better in retrospect.

Firstly, there were some simple mistakes that were made in the design of the PCBs that could have been avoided if more care was taken during the design stage. More time should be taken in reviewing the PCB designs before being sent to the manufacturer. This would include, ensuring to run design rule checks on the PCB design after completion and even peer board reviews to ensure that the designer does not work in isolation.

Moreover, when adding parts to an electrical schematic, care should be taken to ensure that the parts are connected in a way that is correct and that the part is actually suitable for use. Datasheets often have reference circuit that can be used to ensure that the correct parts are used and often have sections explaining how to select the correct components. If more care was taken when selecting the DCDC buck converter circuit then perhaps it would have been deemed unsuitable due to the required footprint size of its parts.

One of the main challenges if this project is continued is the development of revision 2 boards. The majority of components selected on the revision 1 boards were identical to the ones on the current microcontroller test jig PCB. This was to ensure that they were as similar as possible to make the debug easier. Some ICs that were used such as the ADC, high side switches and buck converters are currently out of stock on all supplier websites. This is due to global supply chain shortages of silicon that is affecting the manufacturing industry [2]. In the next revision of these boards, some parts will need to be designed out with alternate parts so the boards can be manufactured fully.

This will require some changes in the test software, for example if an alternative ADC IC is selected, the test script will be required to interface with it. This solution is better than putting a project on hold and waiting for parts for up to a year or more in some cases.

Although the hardware design has made much progress, the parallel testing is something that will have to be investigated further. The parallel test system will be required to interface with databases within the factory for logging purposes. The current test system does not support this.

A large amount of progress has been made in this project however further work will be required to get the microcontroller test to be automated in a way that is cost effective.

10 APPENDIX

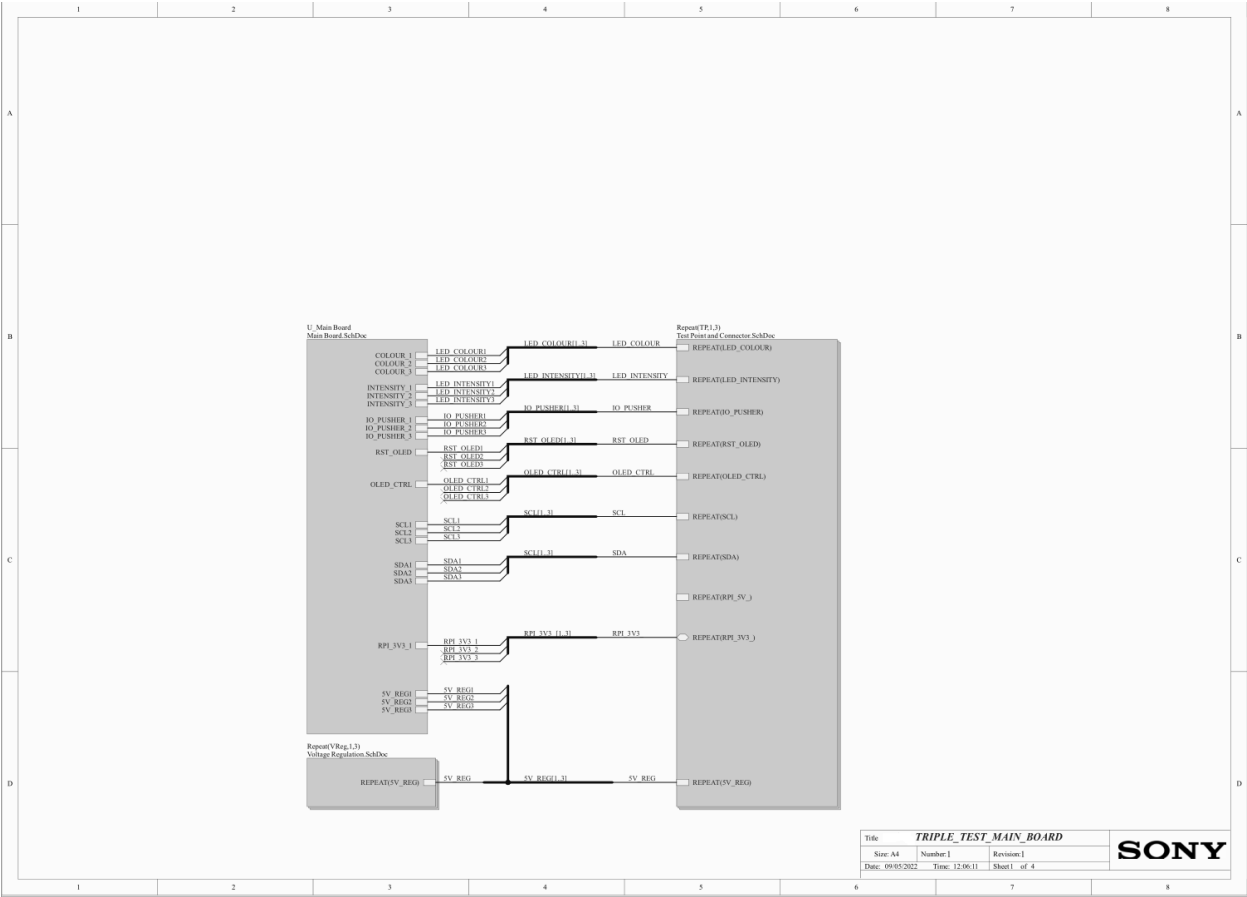
10.1 TRIPLE TEST JUSTIFICATION CALCULATIONS

The production plan for the microcontroller is 47,000 units a week. The aim for the project is to meet production quantities on a single shift. A working week at Sony is 4.5 days due to a half day on the Friday. This means that in a week, the autopod must be able to output 10,444.44 units per day (target per wk / days per week).

There are 420 minutes in a shift. This is equivalent to 25,200 seconds. The cycle time for loading / testing and unloading a single product into a single head is around 22seconds. This means that 1145.455 ($25,200 / 22$) units could be tested on a single head. To meet the production requirements around 9 (9.04) jigs would be required ($10,400 / 1145$). As the auto tester only had 4 heads, this means that multiple boards will need to be tested at the same time. 9 is divisible by 3 so it makes sense for 3 boards to be tested at the same time. 3 test heads could be utilized to meet the quantities, however the fourth could also be added to increase output of the autopod and makeup the remainder.

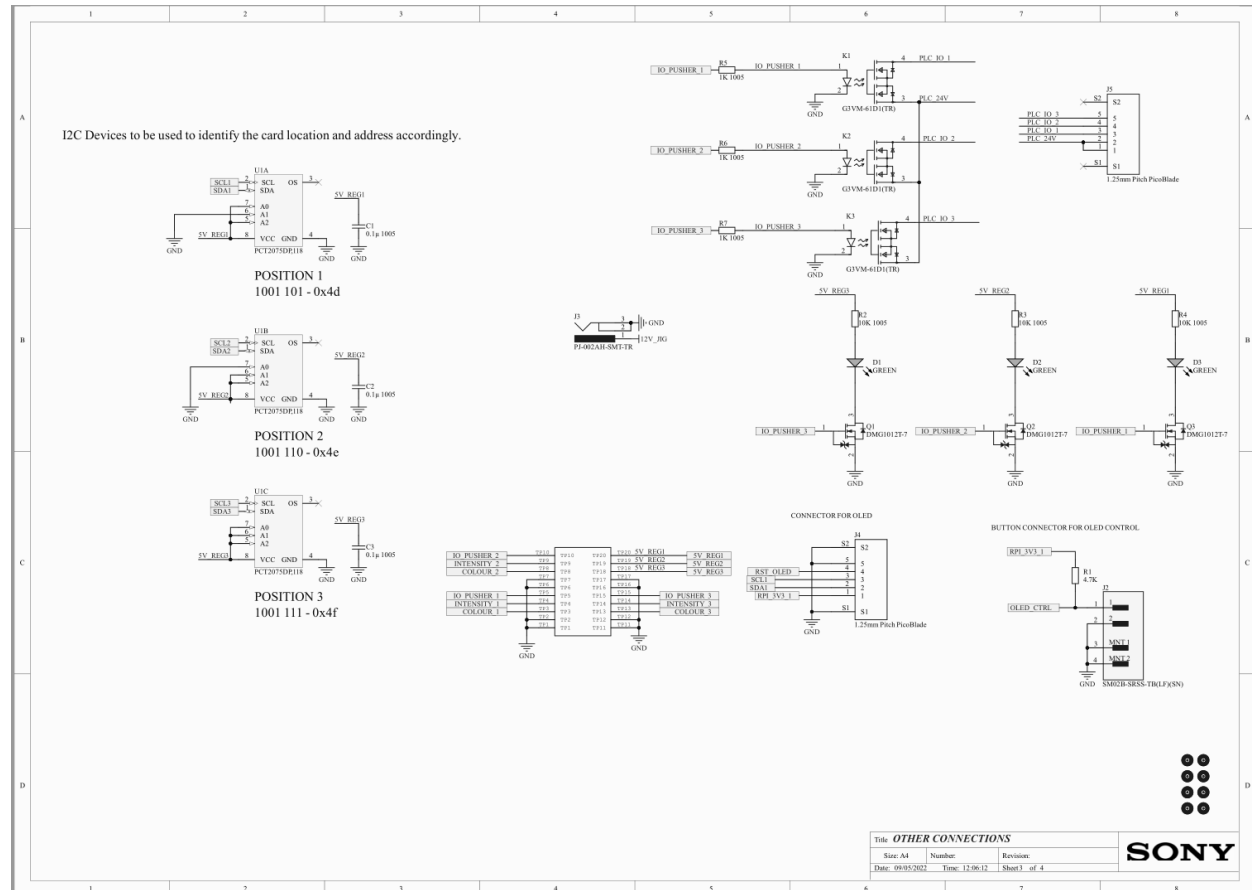
10.2 SCHEMATICS

10.2.1 MAIN BOARD(PAGE 1)



[illegible]

10.2.3 MAIN BOARD (PAGE 3)



[illegible]

Title		
Size: A4	Number:	Revision:
Date: 09/05/2022	Time: 12:06:12	Sheet 4 of 4

SONY

STATUS LED "READY LED"

STATUS LED "TESTING LED"

STATUS LED "TEST PASS LED"

STATUS LED "TEST FAIL LED"

LED CONNECTIONS

LED	Pin	Resistor	Pin	Pin
READY LED	Q1	10K	100nF	100nF
TESTING LED	Q2	10K	100nF	100nF
TEST PASS LED	Q3	10K	100nF	100nF
TEST FAIL LED	Q4	10K	100nF	100nF

ADC CONNECTIONS

Pin	Component	Value	Pin	Component	Value
1	LED	100nF	4	LED	100nF
2	LED	100nF	5	LED	100nF
3	LED	100nF	6	LED	100nF
4	LED	100nF	7	LED	100nF

ADC ADDRESS

DC ADDRESS 0x41/01001000

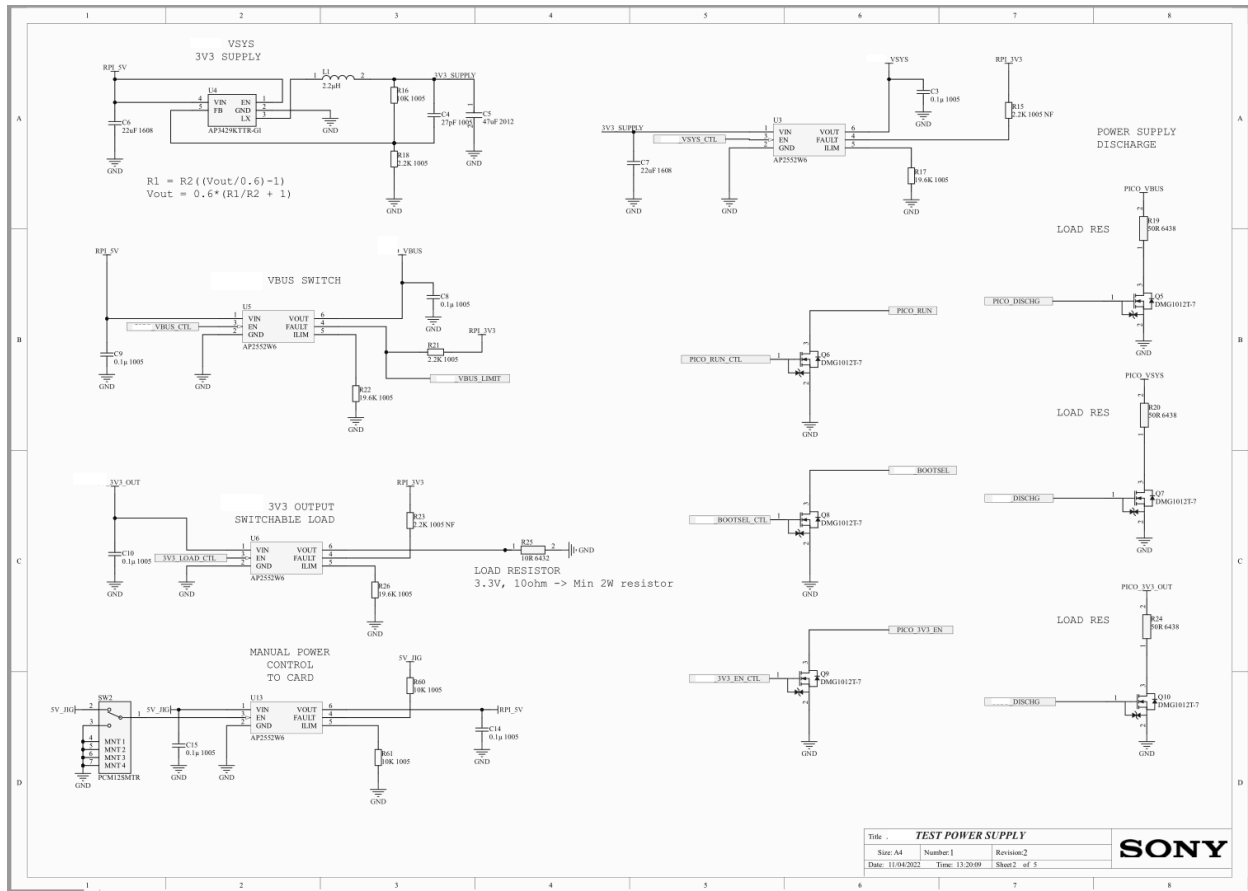
DC ADDRESS 0x49/01001001

TEST LEDS / MEASUREMENT

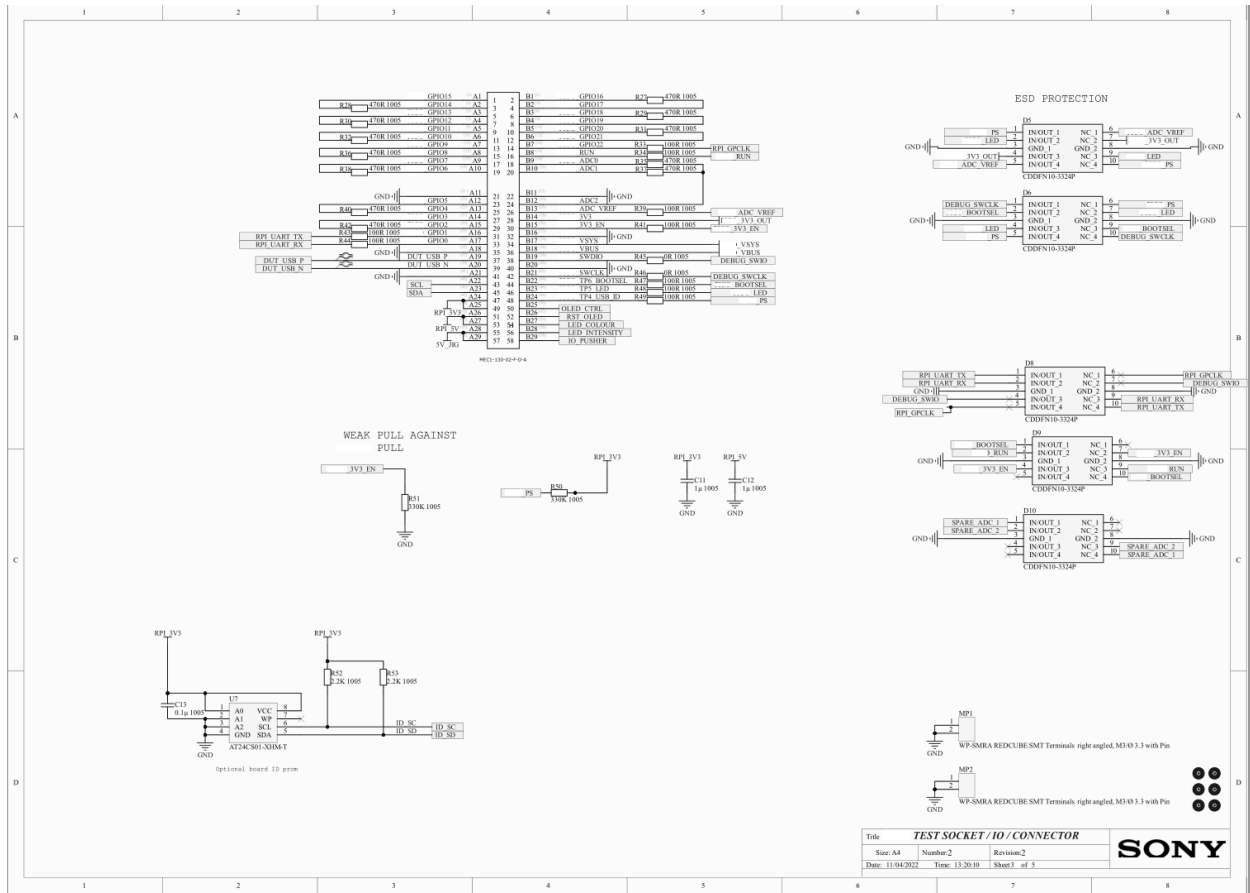
Title	Size: A4	Number: 3	Revision: 2
Date: 11/04/2024	Time: 13:20:09	Sheet: 1 of 1	

SONY

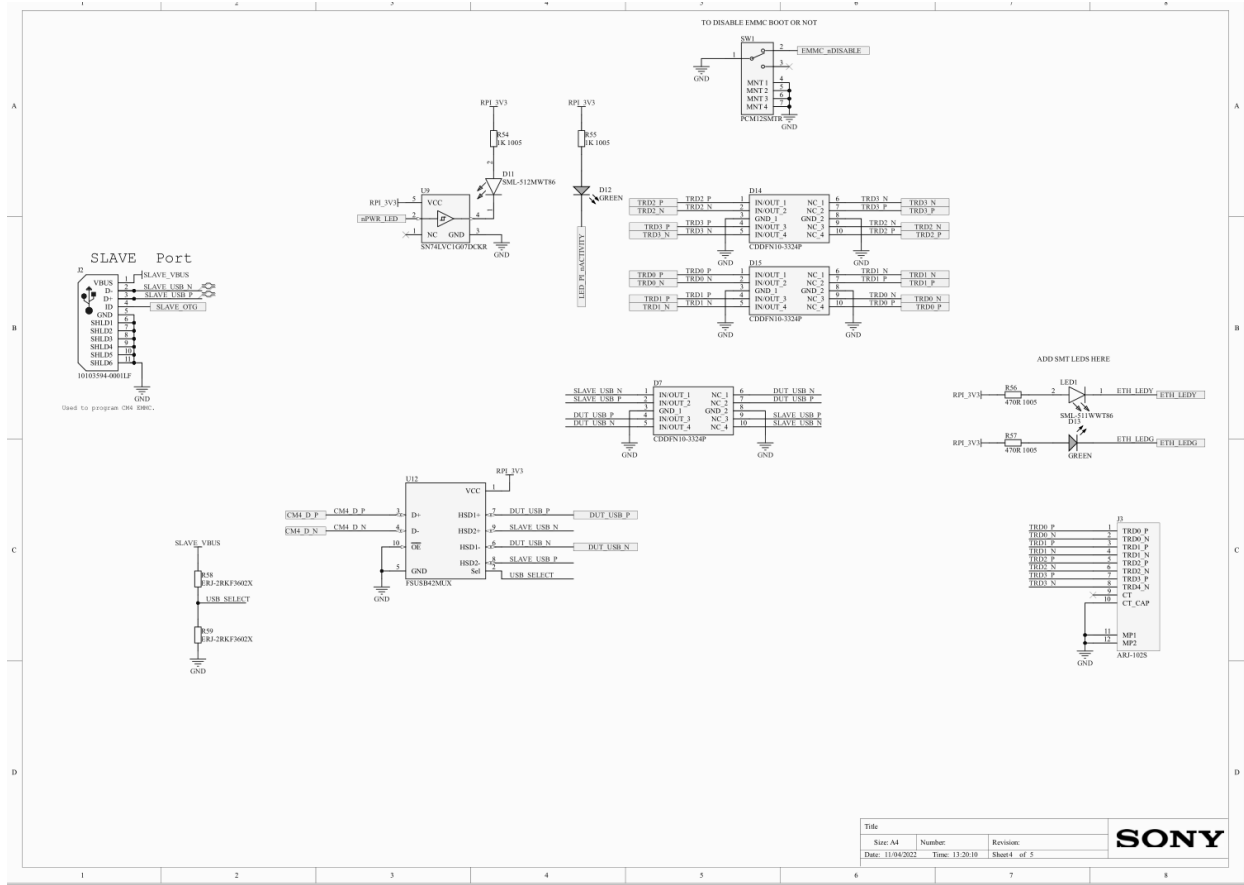
10.2.6 TEST MODULE (PAGE 2)



10.2.7 TEST MODULE (PAGE 3)



10.2.8 TEST MODULE (PAGE 4)



CM1A

GPIO load 50mA to total
GPIO_VREF

RPL_V3V3

SDA1 SDA1_58
SCL1 SCL1_54
RPL_V3V3 RPL_V3V3_54
READY_LED1 LED1_50
TESTING_LED1 LED1_48
TAIL_LED1 LED1_46
RPL_V3V3 RPL_V3V3_54
BOOTSEL_CTL1 CTL1_50

GPIO2 55 TXD0+
GPIO3 56 RXD0+
GPIO4 57 RXD0-
GPIO5 58 RXD0-
GPIO6 59 RXD0-
GPIO7 60 RXD0-
GPIO8 61 RXD0-
GPIO9 62 RXD0-
GPIO10 63 RXD0-
GPIO11 64 RXD0-
GPIO12 65 RXD0-
GPIO13 66 RXD0-
GPIO14 67 RXD0-
GPIO15 68 RXD0-
GPIO16 69 RXD0-
GPIO17 70 RXD0-
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