

**Complete, fold and seal
(see note 2 below)**

SURNAME: Lewis

FORENAME(S): Michael

Examination Answer Books

12 Pages

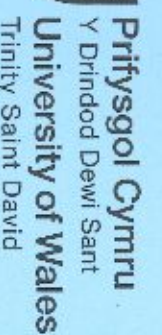
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(Gweler yr ochr arall am y fersiwn Cymraeg)

1	Student Number	140280711
2	Title of Examination Paper	ELECTRONIC DESIGN
3	Module Code	PSDE 6015
4	Date and Time of Examination	9:30
5	Examination Venue	CSE
6	Seat Number	10
7	Number of Answer Books handed in	1/1

List the numbers of the questions you have attempted	Office Use
~~ALL PART A~~	
~~B1~~	
~~B3~~	
A1	4
A2	5
A3	5
A4	6
A5	6
A6	0
A7	2
A8	0
B1	29
B3	23
Total	80



Llyfr Atebion Arholiadau

12 Tudalen

Cyfarwyddiadau i Ymgeiswyr

1. Rhwngch yr holl wybodaeth y gofynnir amdani yn y blychau isod.
2. Rhwngch eich enw yn y lle a ddarparwyd ar y dde, plygwch ef at selio i lawr (gan ddefnyddio'r label a ddarparwyd) i guddio'ch enw.
3. Rhaid i'r atebion fod mewn llawysgrifen ddarlennadwy. Gall yr Arholwyr naill ai amwybyddu sgrïpt annarlennadwy, neu drefnu iddi gael ei threipio a chael yr ymgaisydd i dalu.
4. Ysgrifennwch eich atebion mewn inc.
5. Dechreuwch bob ateb ar dudalen newydd. Gwnewch unrhyw fras nodiadau yn y llyfr atebion a thynnu llinell drwyddynt.
6. Ni ddylid rhwngo unrhyw ran o'r llyfr hwn; rhaid ei gyflwyno yn gyfan.
7. Os defnyddir mwy nag un llyfr, rhwymwch hwy gyda'i gilydd gan ddefnyddio'r tagiau sydd ar gael oddi wrth y gwyllwyr/gwylwyr.
8. Rhaid dychwelyd pob llyfr. Ni chaniateir mynd â llyfrau atebion, wedi eu defnyddio neu heb eu defnyddio, allan o'r lleoliad arholi o dan unrhyw amgylchiadau.

**Llenwch, plygwch a seliwch
(aweler nodyn 2 isod)**

CYFENWYBODAETHYD:

ENW(AU) CYNTAF:

ENW(AU) CYNTAF:

1	Rhif Mlynwr	
2	Teitl y Papur Arholiad	
3	Cod y Modwl	
4	Dyddiad ac Amser yr Arholiad	
5	Lleoliad yr Arholiad	
6	Rhif Sedd	
7	Nifer y Llyfrau Atebion a gyflwynwyd	

[illegible]

(See the other side for English version)

A1 A Ripple factor = $\frac{V_{rms}}{V_{dc}} = \frac{0.7}{18} = 0.039$

B Ripple factor = $\frac{1}{3.5} = 0.286$

PSU Rip. $B < A$

Therefore PSU B is better

A2 The circuit shown is a series regulator that maintains constant output voltage, it does this in the following ways:

If the output voltage ~~was~~ raises for any reason, the voltage across R_2 increases as its part of the output circuit. This in turn leads to more V_f ~~fed~~ across Q_1 of this causes Q_1 to draw more collector current. Most collector current flows through R_3 which causes less Volt drop across the base-emitter of Q_2 which limits its conduction pass. This results in a drop in voltage that counteracts the raise in output voltage. This ~~results~~ results in a stable output voltage.

The exact opposite is true when the output voltage drops. Less V_f feedback across Q_1 , less collector current through R_3 which increases conduction pass of Q_2 , offsetting the decrease in output voltage.

A3. $R_{S(max)} = \frac{V_{in} - V_z}{I_{L(max)} + I_{Z(min)}}$

$$I_{L(max)} = \frac{V_z}{R_{L(min)}} = \frac{4.7}{1.1K} = 4.3mA$$

$$R_{S(max)} = \frac{24 - 4.7}{4.3mA + 1.7mA} = 3.2K\Omega$$

⑤

A4(i) $T_a = T_j - Pd\phi_a = 80 - (400m \times 190) = 4^\circ C$

As $T_a = 22^\circ C$ or heatsink is not required.

(ii)

$$\phi_{SA} = \frac{T_j - T_a}{Pd} = \phi_{CS} - \phi_{SC}$$

$$\phi_{SA} = \frac{80 - 22}{3} - 1.6 - 3 = 14.73^\circ C/W$$

Heatsink required is $14.73^\circ C/W$

⑥

A5

COST

Cost of first prototype

NRE (Non recurring engineering cost)

Cell spinning very costly, re-spin even more
 Licence for cell spinning needed? If so very costly!

Time

Choice of ASIC type dramatically effects time to design

Any mistakes in design (full custom, standard cell) costly

-and Time consuming to fix.

When will first prototype be complete?

Technical feasibility

Is it fast enough.

is it low power enough

will it run on 1.5V

⑥

A6. $I_d = I_{\text{loss}} \left[1 - \frac{V_{GS}}{V_{GS(\text{off})}} \right]^2$

$$\frac{I_d}{I_{\text{loss}}} = \left[1 - \frac{V_{GS}}{V_{GS(\text{off})}} \right]^2 \rightarrow \sqrt{\frac{I_d}{I_{\text{loss}}}} = 1 - \frac{V_{GS}}{V_{GS(\text{off})}}$$

$$1 + \sqrt{\frac{I_d}{I_{\text{loss}}}} = \frac{V_{GS}}{V_{GS(\text{off})}}$$

$$1 + \sqrt{\frac{12\text{m}}{17\text{m}}} = 1.84 \rightarrow 1.84 = \frac{V_{GS}}{-4.5}$$

$$1.84 \times (-4.5) = -8.28\text{V}$$

A7 The temperature stability of Zener diode usually ~~is~~ $\pm 2.2\text{mV}/^\circ\text{C}$ or $0.04\%/^\circ\text{C}$. This means a change of 100°C means a ~~4%~~ change in voltage. This is not acceptable to produce a stable voltage at various temperatures.

However, the positive temperature coefficient of α_1 at $2.2\text{mV}/^\circ\text{C}$ opposes the temperature coefficient of the Zener diode, creating a stable reference voltage at various temperatures, ~~producing~~ with stable temperature characteristics.

A8.

B1(A) $R_s = \frac{V_{in} - V_z}{I_g + I_z} \rightarrow \frac{V_{RS(\text{max})}}{I_{RS}}$

$$I_g = \frac{I_{\text{out}}}{\beta} = \frac{2.5}{70} = 35.7\text{mA}$$

$$I_{RS} = I_g + I_{Z(\text{min})} = 35.7\text{mA} + 1.1\text{mA} = 36.8\text{mA}$$

$$V_{RS(\text{max})} = V_{in(\text{max})} - V_z = 20 - 8.5 = 11.5\text{V}$$

$$R_s = \frac{11.5}{36.8\text{mA}} = 312.5\Omega$$

(ii) $P_{RS} = \frac{(V_{RS(\text{max})})^2}{R_s} = \frac{11.5^2}{312.5} = 0.4232\text{W}$

(iii) $I_{Z(\text{max})} = I_{RS(\text{max})} = \frac{V_{RS}}{R_s} = \frac{11.5}{312.5} = 36.8\text{mA}$

$$P_z = V_z I_{Z(\text{max})} = 8.5 \times 36.8\text{mA} = 0.3128\text{W}$$

(b) The problem with a series regulator is the pass transistor can be destroyed by too much current flowing, from a short circuit for example.

To stop this occurring, a current limiting circuit is added. The circuit consists of a pass transistor Q_3 and R_4 connected between base and emitter.

When the circuit is operating normally, the current through R_4 creates a small voltage drop across it. When the circuit is operating at normal current levels, the voltage drop is so small across R_4 that Q_3 is biased off and doesn't conduct.

PTO

⑥ When the output current is increased to a high enough level, the volt drop increases across R_4 which biases Q_3 on and it conducts. Q_3 's collector current flows through R_3 which reduces the conduction pass of Q_2 .

⑦

$$\phi_{SA} = \frac{T_5 - T_0}{R_4} - \phi_{CS} - \phi_{IC} = \frac{175 - 80}{7.5} - 1.6 - 4$$

$$\phi_{SA} = 7.1^\circ\text{C/W} \quad \checkmark \text{ heatsink required}$$

$$T_5 = T_0 - (\phi_{CS} \times P_d) = 175 - (4 \times 7.5) = 145^\circ\text{C} \quad \checkmark$$

$$h_r = 1.47 \times 10^{-10} \times E \left(\frac{T_5 + T_0}{2} + 273 \right)^3$$

$$= 1.47 \times 10^{-10} \times 0.7 \left(\frac{145 + 80}{2} + 273 \right)^3 = 0.0059 \text{ W/cm}^2$$

$$\text{For } 3'' \text{ sink } H=3$$

$$h_c = 2.21 \times 10^{-3} \left(\frac{T_5 - T_0}{H} \right)^{\frac{1}{4}} = 2.21 \times 10^{-3} \left(\frac{145 - 80}{3} \right)^{\frac{1}{4}} = 0.0048 \text{ W/cm}^2$$

$$h = h_r + h_c = 0.0107 \text{ W/cm}^2$$

$$B = H/2 = 3/2 = 1.5$$

$$\text{From Graph } \alpha = 0.24 \quad \eta = \approx 95\%$$

$$\phi_{SA} = \frac{1}{2 \times H^2 \times \eta \times h} = \frac{1}{2 \times 3^2 \times 0.95 \times 0.0107} = 5.5^\circ\text{C/W} \quad \checkmark$$

PTO

$$\text{For } 2'' \text{ sink } H=2$$

$$h_c = 2.21 \times 10^{-3} \left(\frac{145 - 80}{2} \right)^{\frac{1}{4}} = 0.0053 \text{ W/cm}^2$$

$$h = 0.0112 \text{ W/cm}^2$$

$$B = H/2 = 2/2 = 1$$

$$\text{from graph } \alpha = 0.26 \quad \eta = > 100\%$$

$$\phi_{SA} = \frac{1}{2 \times H^2 \times \eta \times h} = \frac{1}{2 \times 2^2 \times 1 \times 0.0112}$$

$$\phi_{SA} = 11.2^\circ\text{C/W}$$

As at least 7.1°C/W heatsink required, the 2 inch heatsink is more suitable. ✓

(16)

Full custom

All transistors hand drawn
 Transistors ~~drawn~~ drawn on cells connected to form design
 Very power efficient ✓
 Both analogue and digital ✓
 Takes most time to design

Standard cell

Standard cells in library used ✓
 cells connected to form design

Power efficient

Takes less time than full custom ✓
 full metalization masks needed ✓

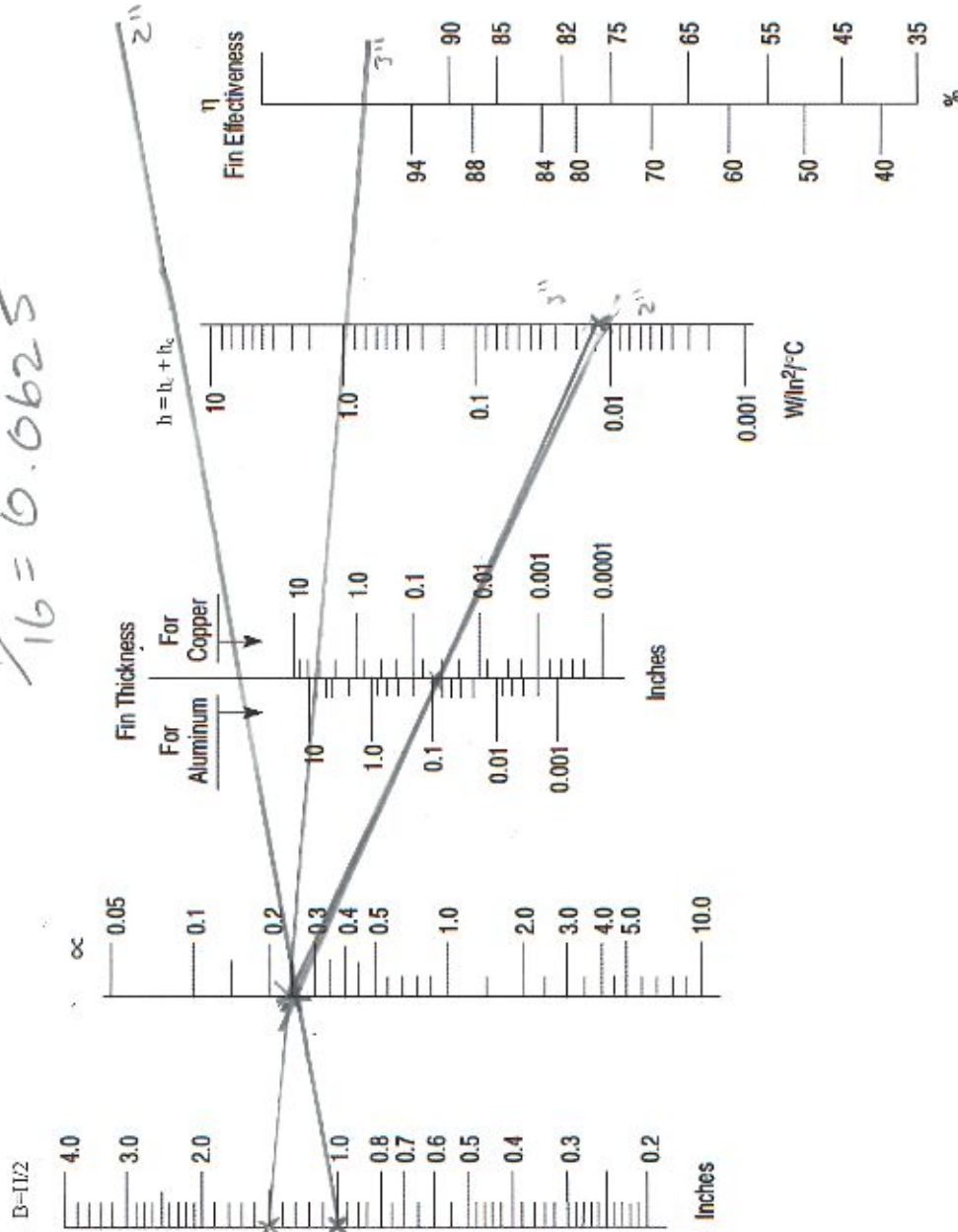
gate array

Transistors connected to form cells
 cells connected to form design ✓
 usually uses HOL and logic synthesis ✓

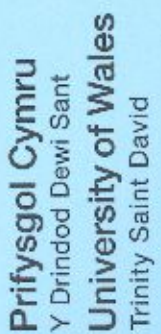
FPGA

All predesigned transistors ✓
 connections configured using 'bit' file
 cheap to buy single unit ✓
 Good for volumes < 1000 ✓
 Not very power efficient ✓
 uses HOL and logic synthesis

$$1/16 = 0.0625$$



SURFACE	EMISSIVITY, E
Polished Aluminum	0.05
Polished Copper	0.07
Rolled Sheet Steel	0.66
Oxidized Copper	0.70
Black Anodized Aluminum	0.7 - 0.9
Black Air Drying Enamel	0.85 - 0.91
Dark Varnish	0.89 - 0.93
Black Oil Paint	0.92 - 0.96



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SURNAME: WILLIAMS

FORENAME(S): LIESEL

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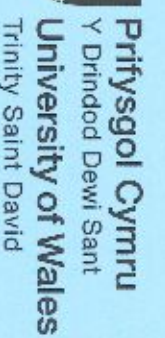
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A7	0
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B1	23
B3	3
Total	55

1	Student Number	1202933/1
2	Title of Examination Paper	Electronic Design
3	Module Code	PSPE6015
4	Date and Time of Examination	17 May 9.30
5	Examination Venue	Gym
6	Seat Number	
7	Number of Answer Books handed in	

(Gweler yr ochr arall am y fersiwn Cymraeg)



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12 Tudalen

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8. Rhaid dychwelyd pob llyfr. Ni chaniateir mynd â llyfrau atebion, wedi eu defnyddio neu heb eu defnyddio, allan o'r lleoliad arholi o dan unrhyw amgylchiadau.

**Llenwch, plygwch a seliwch
(aweler nodyn 2 isod)**

CYFENWY:

ENW(AU) CYNTAF:

1	Rhif Myfyrwr	
2	Teitl y Papur Arholiad	
3	Cod y Mlodwl	
4	Dyddiad ac Amser yr Arholiad	
5	Lleoliad yr Arholiad	
6	Rhif Sedd	
7	Nifer y Llyfrau Atebion a gyflwynwyd	

[illegible]

(See the other side for English version)

A1. PS1 18V_{DC} ripple 0.7V_{rms}
 PS2 35V_{DC} " 1V_{rms}

Ripple factor PS1. $r_f = \frac{\text{ripple}}{V_{out}}$

$$= \frac{0.7}{18} = 0.039$$

Ripple factor PS2 $r_f = \frac{\text{ripple}}{V_{out}}$

$$= \frac{1}{35} = 0.0286$$

With a lower ripple factor PS2 is better. (14)

A2 Referring to Fig A2

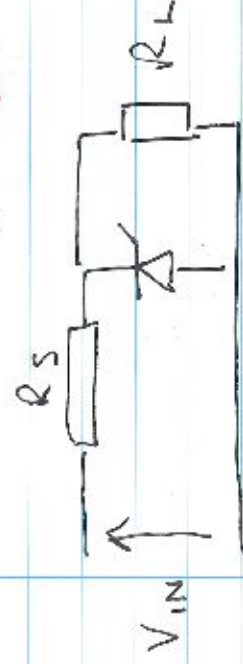
Suppose V_{out} increases this would cause V_{E2} to increase and V_F would also increase. The base current of Q_1 therefore would increase drawing more collector current through Q_1 and more current is drawn through R_3 this has the effect of reducing the base ~~current~~ ^{volume} current on Q_2 and therefore the collector current of Q_2 is lower meaning I_L to load is lower and ~~reduces~~ ^{or regulates} V_{out} . The opposite effect happens when V_{out} decreases. (5)

A3 $V_{in} = 24V$ $V_Z = 4.7V$

$$I_{Z(min)} = 1.7mA \quad R_L = 1.1 \rightarrow 1.5k\Omega$$

$$I_{L(max)} = \frac{V_{in} - V_Z}{R_{L(min)}} = \frac{24.47}{1100} = 0.022A = 22mA$$

$$R_S = \frac{V_{in} - V_Z}{I_{L(max)} + I_{Z(min)}} = \frac{24 - 4.7}{1.7mA + 22mA} = \frac{19.3}{23.7 \times 10^{-3}} = 814.35\Omega$$



A4 $P_D = 400mW$ $T_J = 80^\circ C$ $\theta_{JA} = 190^\circ C/W$
 $\theta_{JC} = 3^\circ C/W$

i) $T_A = T_J - P_D \theta_{JA} = 80 - (0.4 \times 190) = 4^\circ C$

$\therefore$ For a T_A of $22^\circ C$ then a heatsink is required.

ii) $P_D = 3W$ $\theta_{CS} = 1.6^\circ C/W$

$$\theta_{SA} = \theta_{JA} - \theta_{JC} - \theta_{CS}$$

$$= \frac{T_J - T_A}{P_D} - \theta_{JC} - \theta_{CS}$$

$$= \frac{80 - 22}{3} - 3 - 1.6 = 14.73^\circ C/W$$

A5 For choosing ASIC there are several factors

- Time to market - this has the largest impact as for every month delay there is a 10% cost implication. It is essential to get the product to market quickly.
- Cost - there is a very large cost involved with licences costing £125K it takes about £1 mil to put on market
- Technical feasibility - considerations such as speed, is it fast enough? power, is it low power enough? and can it operate on 1.2V? These must be considered.

A7 The effect is minimized by constant zener current draw, this produces a stable reference voltage and therefore stabilizes thermal effects. (6)

A8

skew rate overlap causes on/off states to merge and causes metastability. In other words instead of being in one stable state it swings between states. (6)

A6 $I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_{GS(off)}} \right]^2$ $I_D = 12 \times 10^{-3} A$
 $I_{DSS} = 17 \times 10^{-3} A$
 $V_{GS(off)} = -4.5 V$

$$\sqrt{\frac{I_D}{I_{DSS}}} = 1 - \frac{V_{GS}}{V_{GS(off)}}$$

$$\frac{V_{GS}}{V_{GS(off)}} = 1 - \sqrt{\frac{I_D}{I_{DSS}}} \therefore V_{GS} = V_{GS(off)} \left[1 - \sqrt{\frac{I_D}{I_{DSS}}} \right]$$

$$V_{GS} = -4.5 \left[1 - \sqrt{\frac{12 \times 10^{-3}}{17 \times 10^{-3}}} \right] = -0.719 V (4)$$

$$I_L = 2.5 A$$



$$V_{OUT} = V_Z - V_{BE}$$

$$V_Z = V_{OUT} + V_{BE}$$

$$= 8 + 0.7 = 8.7 V$$

$$I_C = \beta I_B \quad \therefore I_B = \frac{I_C}{\beta} = \frac{2.5}{70} = 0.036 A$$

$$= 35.7 mA$$

$$i) R_{S(max)} = \frac{V_{IN} - V_Z}{I_{L(max)} + I_{Z(min)}} = \frac{20 - 8.7}{2.5 + 0.011}$$

$$= \frac{11.3}{2.511} = 4.52 \Omega$$

$$I_{RS} = I_B + I_Z = 35.7 + 1.1 = 36.8 mA$$

$$= 36.8 \times 10^{-3} A$$

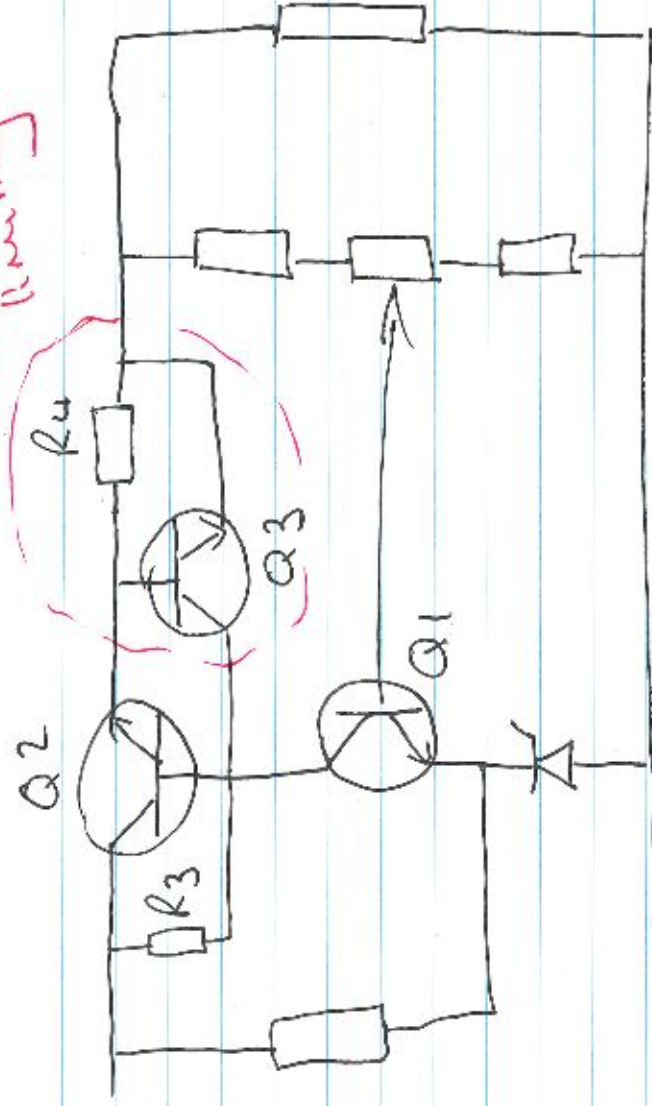
$$ii) P_{RS} = I_{RS}^2 R_{S(max)} = (36.8 \times 10^{-3})^2 \times 4.52$$

$$P_{RS} = 11.3 \times 36.8 \times 10^{-3} = 0.42 W (6)$$

$$iii) P_Z = I_Z \times V_Z = 1.1 \times 10^{-3} \times 8.7$$

$$= 9.57 mW (6)$$

B1
b)



Suppose the value of R_L drops and more load current is drawn then V_{CE} increases V_{CE} and the base current of Q3 which turns on and draws current via R_3 this has the effect of reducing the base current and Q2 and therefore less collector current flows in Q2 and hence reduces the current to the load.

(6)

$$P_D = 7.5W \quad T_A = 80^\circ C$$

fin 1/16" oxidised copper $\epsilon = 0.7$ from table p9.

$$T_J = 175^\circ C$$

$$\theta_{CS} = 1.6^\circ C/W$$

$$\theta_{JC} = 4^\circ C$$

$$\theta_{JA} = \frac{T_J - T_A}{P} = \frac{175 - 80}{7.5} = 12.667^\circ C/W$$

$$\theta_{SA} = \theta_{JA} - \theta_{JC} - \theta_{CS} = 12.667 - 4 - 1.6 = 7.067^\circ C/W$$

$$T_S = T_J - (\theta_{JC} P_D) = 175 - (4 \times 7.5) = 145^\circ C$$

$$h_r = 1.47 \times 10^{-10} \times \epsilon \left(\frac{T_S + T_A}{2} + 273 \right)^3 = 1.47 \times 10^{-10} \times 0.7 \left(\frac{145 + 80}{2} + 273 \right)^3 = 5.89 \times 10^{-3}^\circ C/Wm^2$$

$$3'' \text{ sink } h_c = 2.21 \times 10^{-3} \left(\frac{T_S - T_A}{H} \right)^{1/4} = 2.21 \times 10^{-3} \left(\frac{145 - 80}{3} \right)^{1/4} = 4.77 \times 10^{-3}^\circ C/Wm^2$$

$$h = h_c + h_r = 4.77 + 5.89 = 10.66 \times 10^{-3}^\circ C/Wm^2$$

$$2'' \text{ sink } h_c = 2.21 \times 10^{-3} \left(\frac{145 - 80}{2} \right)^{1/4} = 5.28 \times 10^{-3}^\circ C/Wm^2$$

$$h = 5.28 + 5.89 = 11.17 \times 10^{-3}^\circ C/Wm^2$$

$$\text{For } 3'' \quad \theta_{SA} = \frac{1}{2 \times H^2 \times \eta \times h}$$

$$= \frac{1}{2 \times 3^2 \times 0.96 \times 10.66 \times 10^{-3}}$$

$$= 5.429^\circ \text{C/W} \checkmark$$

$$\text{For } 2'' \quad \theta_{SA} = \frac{1}{2 \times 2^2 \times 1 \times 11.17 \times 10^{-3}}$$

$$= 11.191^\circ \text{C/W} \checkmark$$

By comparing with the calculated θ_{SA} of 7.067°C/W the $3''$ sink is a closer match.

→ A B C D
0 1 1 1
1 1 1 1

1110000 112
1111111 127

B3

c) i)

Inputs are A, B, C, D, LT, RB1, B12

Outputs are 70-76

iii) Operations

Inputs A-D are 0-15

binary count

B1 sets off to all ones

LT is lamp test sets all to zeros

RB1 sets off to decimal 1



ii)

Inputs ABCD count up from 0-15 and 7 generator random numbers

USB NSB

A	B	C	D	LT	RB1	B1	DEC
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0
1	1	0	0	0	0	0	0
0	0	1	0	0	0	0	0
1	0	1	0	0	0	0	0
0	1	1	0	0	0	0	0
1	1	1	0	0	0	0	0
0	0	0	1	0	0	0	0
1	0	0	1	0	0	0	0
0	1	0	1	0	0	0	0
1	1	0	1	0	0	0	0
0	0	1	1	0	0	0	0
1	0	1	1	0	0	0	0
0	1	1	1	0	0	0	0
1	1	1	1	0	0	0	0
0	0	0	0	1	0	0	0
1	0	0	0	1	0	0	0
0	1	0	0	1	0	0	0
1	1	0	0	1	0	0	0
0	0	1	0	1	0	0	0
1	0	1	0	1	0	0	0
0	1	1	0	1	0	0	0
1	1	1	0	1	0	0	0
0	0	0	1	1	0	0	0
1	0	0	1	1	0	0	0
0	1	0	1	1	0	0	0
1	1	0	1	1	0	0	0
0	0	1	1	1	0	0	0
1	0	1	1	1	0	0	0
0	1	1	1	1	0	0	0
1	1	1	1	1	0	0	0

15

3