



INTERNAL ASSESSMENT APPROVAL FORM (INCLUDING COLLABORATIVE PROVISION)

This form is used to ensure that assessment specifications have been through an internal review process prior to external examination/approval and release to students. It should be completed for each assessment for a particular module. The assessment tasks, criteria and marking scheme should accompany this form.

PARTNER (and taught location if relevant):	Coleg Sir Gar				
EXTERNAL EXAMINER NAME:	Dr Alison Griffiths				
ASSESSMENT AUTHOR :	Mike Hall				
MODULE TITLE:	Electronics II				
MODULE CODE:	PSDE 5006 / SGEE5000		MODULE LEVEL:	5	
COMPONENT NO. (e.g. 1 of 2):	2 of 2		COMPONENT WEIGHTING (e.g. 50% of the module):	50%	
ASSESSMENT PERIOD	☐ Semester 1	☐ Semester 1 <i>Re-sit</i>	☒ Semester 2	☐ Semester 2 <i>Re-sit</i>	<i>Other, please state</i>
TYPE OF ASSESSMENT:	☐ Coursework		☒ Examination		☐ Practical
LANGUAGE OF ASSESSMENT:	English		TRANSLATION REQUIRED (Y/N):	N	
FOR EXAMINATIONS ONLY. SPECIFY BELOW ANY ADDITIONAL MATERIAL(S) TO BE USED IN THE EXAMINATION					
<i>This box will expand as you type</i>					

INTERNAL MODERATOR PLEASE TICK TO INDICATE THAT THE ASSESSMENT INCLUDES:		Please ☒ YES ☐ NO		Comments
1	Tasks that are specified clearly, accurately and comprehensibly, with appropriate use of language and neat presentation	☒	☐	
2	Tasks which enable the module learning outcomes to be demonstrated (as per the module syllabus)	☒	☐	
3	Tasks which conform to the assessment described in the module syllabus	☒	☐	
4	Tasks which are written at the appropriate level of the Framework for Higher Education Qualifications (see http://www.qaa.ac.uk/docs/qaa/quality-code/qualifications-frameworks.pdf?sfvrsn=170af781_14).	☒	☐	
5	Clear criteria for assessment and guidance about how marking/grading will be applied	☒	☐	
6	Guidance about expected evidence for submission, e.g. essay or report, word count, bibliography and references	☒	☐	
7	Reference to good academic conduct, for example referencing, plagiarism and Turnitin	☒	☐	
8	Actions to complete <i>This box will expand as you type</i>			
SIGNATURE OF APPROVAL:		SIGNATURE		DATE
INTERNAL MODERATOR: I confirm that this version of the assessment specification is ready to be sent to the Partnership Team Leader				04/04/2019

ONLY TO BE COMPLETED IF THE ASSESSMENT IS LINKED TO A COLLABORATIVE PARTNER

PARTNERSHIP TEAM LEADER PLEASE TICK TO INDICATE THAT THE ASSESSMENT INCLUDES:		Please ✓		Comments
		YES	NO	
1	Tasks that are specified clearly, accurately and comprehensibly, with appropriate use of language and neat presentation			
2	Tasks which enable the module learning outcomes to be demonstrated (as per the module syllabus)			
3	Tasks which conform to the assessment described in the module syllabus			
4	Tasks which are written at the appropriate level of the Framework for Higher Education Qualifications (see http://www.qaa.ac.uk/docs/qaa/quality-code/qualifications-frameworks.pdf?sfvrsn=170af781_14).			
5	Clear criteria for assessment and guidance about how marking/grading will be applied			
6	Guidance about expected evidence for submission, e.g. essay or report, word count, bibliography and references			
7	Reference to good academic conduct, for example referencing, plagiarism and Turnitin			
8	Actions to complete <i>This box will expand as you type</i>			
SIGNATURE OF APPROVAL:		SIGNATURE		DATE
PTL: I confirm that this version of the assessment specification is ready to be sent to the External Examiner				

UWTSD PROVISION: please submit the completed document to the appropriate Programme Director.

COLLABORATIVE PROVISION: please submit the completed document (or make available electronically) to the Partnership Team Leader. This must be in accord with specific arrangements for sharing electronic documents (e.g. via SharePoint or similar).

The assessment tasks, criteria and marking scheme should accompany this form

LOCATION: COLEG SIR GAR

LLEOLIAD: COLEG SIR GAR

LEVEL 5

LEFEL 5

**EXAMINATION PERIOD
MAY 2019**

**CYFNOD ARHOLIADAU
MAI 2019**

MODULE CODE: PSDE 5006 / SGEE5000

Electronics II

TIME: 2½ HOURS

THIS PAPER IS IN 2 PARTS:

ANSWER ALL QUESTIONS IN PART A

ANSWER TWO QUESTIONS OUT OF THREE IN PART B

Equipment or materials required – Calculator

Adnoddau neu ddefnyddiau sydd eu hangen - Cyfrifiannell

Formulae

$$A_{vf} = \frac{A_v}{1 + A_v m_v}$$

$$f = \frac{1}{2\pi\sqrt{LC}}$$

$$m_v = \frac{C_1}{C_2}$$

$$m_v = \frac{L_2}{L_1}$$

$$f_0 = \frac{1}{2\pi CR \sqrt{6}}$$

$$BW = \frac{f_0}{Q}$$

$$R_1 = \frac{a_1}{2\pi f_c C_1}$$

$$C_2 > \frac{C_1 \times 4b}{a^2}$$

$$R_1 = \frac{1}{2\pi f_c a_1 c_1}$$

$$R_1, R_2 = \frac{a_1 C_2 \pm \sqrt{a_1^2 C_2^2 - 4b_1 C_1 C_2}}{4\pi f_c C_1 C_2}$$

$$R_1 = \frac{1}{\pi f_c \times C \times a_2}, R_2 = \frac{a_2}{4\pi f_c \times C \times b_2}$$

PART A – Answer ALL Questions.

A1. A three-stage amplifier has a first stage voltage gain of 150, second stage voltage gain of 200 and third stage voltage gain of 125. Find the gain of each stage and the total voltage gain in dB.

(4 marks)

A2. An amplifier rated at 150W output is connected to a 8Ω speaker.

- i. Calculate the input power required for full power output if the power gain is 45dB
- ii. Calculate the input voltage for the rated output if the amplifier voltage gain is 30dB

(6 marks)

A3. A multistage transistor amplifier uses transformer coupling. The output impedance of one stage is $20k\Omega$ while the input impedance of the next stage is $1.5k\Omega$. Determine the inductance of the primary and secondary of the transformer for perfect impedance matching at a frequency of 600Hz.

(5 marks)

A4. State and briefly describe 3 advantages of negative feedback.

(6 marks)

A5. Find the capacitance of the capacitor required to build an LC oscillator that uses an inductance of $L1 = 5\mu H$ to produce a sine wave of frequency 20MHz.

(4 marks)

A6. Explain the principle of operation of the Colpitts oscillator.

(6 marks)

A7. Explain the main features of the Butterworth filter type. Illustrate your answer with appropriate bode plots.

(5 marks)

A8. The VHDL code for a standard logic gate is shown below.

- i. What are the inputs and outputs for Gate1?
- ii. Draw the entity for Gate1.
- iii. Explain the operation of Gate1 with the aid of a truth table.

```
library IEEE;  
use IEEE.STD_LOGIC_1164.ALL;
```

```
entity Gate1 is
    port (
        A: in STD_LOGIC;
        B: in STD_LOGIC;
        C: in STD_LOGIC;
        D: in STD_LOGIC;
        Y: out STD_LOGIC
    );
end Gate1;

architecture BEHAVIORAL of Gate1 is

begin
    Y <= A and B and C and D;
end BEHAVIORAL;
```

(4 marks)

Total Marks for Part A = 40

PART B – Only answer 2 of the following 3 questions (B1, B2, B3)

If you answer all 3, only B1 and B2 will be marked

Question B1 – Special Amplifiers

- a. An amplifier feeding a resistive load of 2k has a voltage gain of 75dB. If the input signal is 1.2mV, find:

- The output voltage
- The load power

(4 marks)

- b. Figure B1.1 shows a direct coupled two-stage amplifier. Determine the DC voltages for both stages if V_{cc} is 15V.

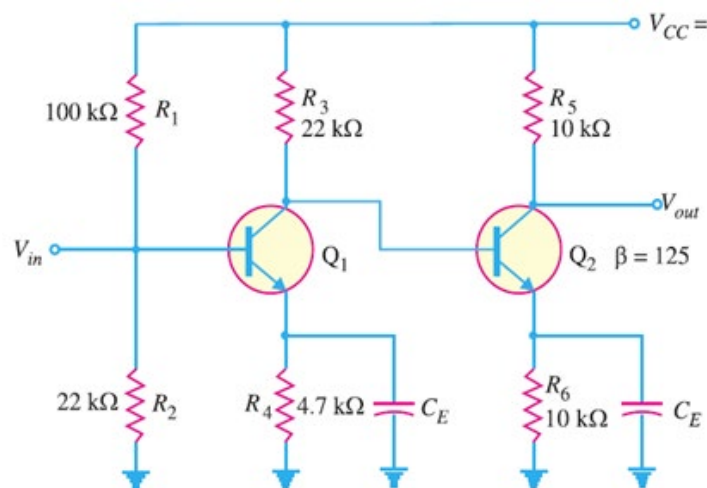


Figure B1.1

(11 marks)

- c. The Q of a tuned amplifier is 100. If the resonant frequency for the amplifier is 2MHz, find the bandwidth and the cut-off frequencies.

(3 marks)

- d. The voltage gain of an amplifier without feedback is 2400. Calculate the voltage gain of the amplifier if negative voltage feedback is introduced in the circuit. Given that the feedback fraction $m_v = 0.02$.

(3 marks)

- e. State and describe 3 advantages of tuned amplifiers.

(6 marks)

- f. For the tuned amplifier shown in Figure B1.2, determine the resonant frequency of the amplifier for the following component values: $C = 0.33\mu\text{F}$, $L = 47\text{mH}$.

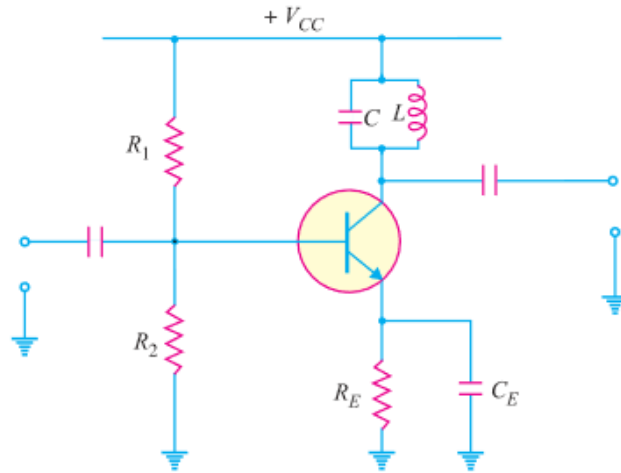


Figure B1.2

(3 marks)

Total Marks for Question B1 = 30

Question B2 – Filter and Oscillator Design

- a. Using a 220pF capacitor for all stages and with 5nF and 70nF capacitors also available for Stages 2 and 3 respectively; design a 5th order unity-gain 3dB Tschebyscheff low pass filter with corner frequency (f_c) of 100kHz.

n	i	a_i	b_i	$k_i = \frac{f_{Ci}}{f_C}$	Q_i
1	1	1.0000	0.0000	1.000	—
2	1	1.0650	1.9305	1.000	1.30
3	1	3.3496	0.0000	0.299	—
	2	0.3559	1.1923	1.396	3.07
4	1	2.1853	5.5339	0.557	1.08
	2	0.1964	1.2009	1.410	5.58
5	1	5.6334	0.0000	0.178	—
	2	0.7620	2.6530	0.917	2.14
	3	0.1172	1.0686	1.500	8.82
6	1	3.2721	11.677 3	0.379	1.04
	2	0.4077	1.9873	1.086	3.46
	3	0.0815	1.0861	1.489	12.78

(20 marks)

- b. Calculate the capacitor value required for a Colpitts oscillator so that the frequency of oscillation is 30MHz. Take m_v to be 0.25 and the inductor value to be 20uH.

(7 marks)

- c. A tuned collector oscillator circuit uses an LC tuned circuit with $L1 = 47\mu\text{H}$ and $C1 = 300\text{pF}$. Calculate the frequency of oscillator.

(3 marks)

Total Marks for Question B2 = 30

Question B3 – Finite State Machines and VHDL

- a. Using the Moore machine model, design a traffic light controller. The circuit will have 1 input (Trigger), 3 outputs (red, amber, green) and should behave as follows:

- Red
- Red/amber
- Green
- Amber
- Red

The circuit should wait when at red or green until the 'Trigger' input goes high. On red/amber and amber it should wait for 1 state then automatically progress to the next state.

(22 marks)

- b. The VHDL code for a standard logic gate is shown below.

- What are the inputs and outputs for Gate1?
- Draw the entity for Gate1.
- Explain the operation of Gate1 with the aid of a truth table.

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity GATE1 is
port (
    A , B, C, D: in STD_LOGIC;
    LT, RBI, BI: in STD_LOGIC;
    OA, OB, OC, OD, OE, OF, OG: out STD_LOGIC;
);
end GATE1;
```

```
architecture BEHAVIORAL of GATE1 is
    signal O : STD_LOGIC_VECTOR(0 TO 6);
```

```
begin
    process (BI,LT,RBI,A,B,C,D)
    begin
        if BI='0' then O<="1111111";
        elsif LT='0' then O<="0000000";
        elsif (A='0' and B='0' and C='0' and D='0' and RBI='1') then O<="0000001";
        elsif (A='1' and B='0' and C='0' and D='0') then O<="1001111";
        elsif (A='0' and B='1' and C='0' and D='0') then O<="0010010";
        elsif (A='1' and B='1' and C='0' and D='0') then O<="0000110";
        elsif (A='0' and B='0' and C='1' and D='0') then O<="1001100";
        elsif (A='1' and B='0' and C='1' and D='0') then O<="0100100";
```

```

    elsif (A='0' and B='1' and C='1' and D='0') then O<="1100000";
    elsif (A='1' and B='1' and C='1' and D='0') then O<="0001111";
    elsif (A='0' and B='0' and C='0' and D='1') then O<="0000000";
    elsif (A='1' and B='0' and C='0' and D='1') then O<="0001100";
    elsif (A='0' and B='1' and C='0' and D='1') then O<="1110010";
    elsif (A='1' and B='1' and C='0' and D='1') then O<="1100110";
    elsif (A='0' and B='0' and C='1' and D='1') then O<="1011100";
    elsif (A='1' and B='0' and C='1' and D='1') then O<="0110100";
    elsif (A='0' and B='1' and C='1' and D='1') then O<="1110000";
    elsif (A='1' and B='1' and C='1' and D='1') then O<="1111111";
  end if;
end process;
  OG<=O(6);
  OF<=O(5);
  OE<=O(4);
  OD<=O(3);
  OC<=O(2);
  OB<=O(1);
  OA<=O(0);
end BEHAVIORAL;

```

(8 marks)

Total Marks for Question B3 = 30

Programme:	HNC in Electrical & Electronic Engineering	Level:	5
Module:	PSDE5006 /SGEE5000 Electronics II		
Author:	M Hall	Page:	Page 1 of 9

Part A	Question	Marks
A1	$A_1 = 20\log 150 = 43.5\text{dB}$ $A_2 = 20\log 200 = 46\text{dB}$ $A_3 = 20\log 125 = 42\text{dB}$ Total = 131dB	1 1 1 1
A2	$P_{in} = 150 / \text{antilog}(45/10) = \textbf{4.7mW}$ $A_v = \text{antilog}(30/20) = 31.6$ $V_{out} = \sqrt{P \times R} = \sqrt{150 \times 8} = 34.6V$ $V_{in} = V_{out}/A_v = 34.6/31.6 = \textbf{1.1V}$	3 1 1 1
A3	For impedance matching, Z_{out} of transistor = $Z_{primary}$ Therefore, $Z_{out} = 2\pi f L_p$ $20000 = 2\pi \times 600 \times L_p$ $L_p = 20000 / (2\pi \times 600) = \textbf{5.3H}$ For impedance matching, Z_{in} of next stage = $Z_{secondary}$ Therefore, $Z_{in} = 2\pi f L_s$ $1500 = 2\pi \times 600 \times L_s$ $L_s = 1500 / (2\pi \times 600) = \textbf{0.4H}$	3 2
A4	<u>Consistency of Gain.</u> An important advantage of negative feedback is that the resultant gain of the amplifier can be made independent of transistor parameters or the supply voltage. $A_{vf} = \frac{A_v}{1 + A_v m_v}$ For negative voltage feedback in an amplifier to be effective, the designer deliberately makes the product ($A_v \times m_v$) much greater than unity. Therefore, in the above equation, the “1” can be neglected, the A_v's cancel and the equation becomes $1/m_v$. The gain now depends only upon the feedback fraction m_v.	3

Improves frequency response.

As feedback is usually obtained through a resistive network, the voltage gain of the amplifier is independent of signal frequency. The result is that voltage gain of the amplifier will be constant over a wide range of signal frequencies. The negative voltage feedback, therefore, improves the frequency response of the amplifier.

1

Increases thermal stability.

The output of an amplifier can change due to variations in ambient temperature. This changes the gain of the amplifier, resulting in distortion. However, by applying negative voltage feedback, voltage gain of the amplifier is stabilised. Suppose the output of an amplifier has increased because of temperature change. This means more negative feedback since feedback is being generated as a portion of the output. This increased feedback signal oppose the increase in amplification and maintains it at a constant level.

2

A5

$$f = \frac{1}{2\pi\sqrt{LC}}$$

Rearranging for C1

$$C_1 = \frac{1}{L_1 (2\pi f)^2}$$

$$= \frac{1}{5\mu \times (2\pi \times 20M)^2}$$

$$= 12.67\text{pF}$$

4

A6

It uses two capacitors placed in parallel with an inductor L and the centre of the two capacitors is tapped. The tank circuit is made up of C1, C2 and L. The frequency of oscillations is determined by the values of C1, C2 and L and is given by ;

$$f = \frac{1}{2\pi\sqrt{LC_T}}$$

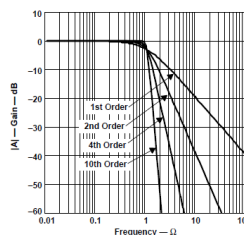
When the circuit is turned on, the capacitors C1 and C2 are charged. The capacitors discharge through L, setting up oscillations. The output voltage of the amplifier appears across C1 and feedback voltage is developed across C2. The voltage across it is 180° out of phase with the voltage developed across C1 (Vout). It is easy to see that voltage feedback (voltage across C2) to the transistor provides positive feedback. A phase shift of 180° is produced by the transistor and a further phase shift of 180° is produced by C1-C2 voltage divider. In this way, feedback is properly phased to produce continuous undamped oscillation.

6

A7

The Butterworth low-pass filter provides maximum passband flatness. Therefore, a Butterworth low-pass is often used as anti-aliasing filter in data converter applications where precise signal levels are required across the entire passband. The rate of roll-off is 20dB/decade.

3



2

A8

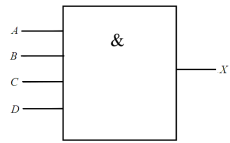
The inputs are A, B, C, D

1

The output is Y

1

The entity is:



1

The device is a 4 input AND gate

1

Q. B1	Question	Marks
a.	$V_{out} = V_{in} \times \text{antilog}(75/20) = 6.75V$ $P_{load} = V^2/R = 6.75^2/2000 = 22.8mW$	2 2
b.	<u>First Stage</u> $I_{R1} = I_{R2} = V_{cc} / (R_1 + R_2) = 15/122k = 123uA$ $V_{B1} = V_{R2} = I_{R2} \times R_2 = 123u \times 22k = 2.7V$ $V_{E1} = V_{B1} - 0.7 = 2V$ $I_{R4} = V_{E1} / R_4 = 2m / 4.7k = 425uA$ Assuming $I_{C1} = I_{R4}$, then $V_{C1} = V_{CC} - I_{C1}R_3 = 15 - (425u \times 22k) = 5.6V$ <u>Second Stage</u> $V_{B2} = V_{C1} = 5.6V$ $V_{E2} = V_{B2} - 0.7 = 4.9V$ $I_{R6} = V_{E2} / R_6 = 490uA$ Assuming $I_{C2} = I_{R6}$, then $V_{C2} = V_{CC} - I_{C2}R_5 = 15 - (490u \times 10k) = 10.1V$	2 2 2 2 1 2
c.	$BW = \frac{f_0}{Q}$ $= 2M / 100 = 20kHz$ Lower frequency = $f - \frac{1}{2} \text{ Bandwidth} = 2M - 10k = 1.99MHz$ Upper frequency = $f + \frac{1}{2} \text{ Bandwidth} = 2M + 10k = 2.01MHz$	 3
d.	$A_{vf} = \frac{A_v}{1 + A_v m_v}$ $= \frac{2400}{1 + (2400 \times 0.02)} = 49$	3
e.	<u>Small power loss.</u> A tuned parallel circuit employs reactive components L and C. Consequently, the power loss in such a circuit is very low. If a resistive load is used in the collector circuit, there will be considerable loss of power, therefore, tuned amplifiers are highly efficient. <u>High selectivity.</u> A tuned circuit has the property of selectivity i.e. it can select the desired frequency for amplification out of a large number of frequencies simultaneously impressed upon it. For instance, if a mixture of frequencies including the wanted frequency is fed to the input of a tuned amplifier, then maximum amplification	

occurs for the wanted frequency. For all other frequencies, the tuned circuit offers very low impedance and hence these are amplified to a little extent and may be thought as rejected by the circuit. On the other hand, if we use resistive load in the collector, all the frequencies will be amplified equally well i.e. the circuit will not have the ability to select the desired frequency.

Smaller collector supply voltage.

Because of little resistance in the parallel tuned circuit, it requires only a small collector supply voltage V_{CC} . On the other hand, if a high load resistance is used in the collector for amplifying even one frequency, it would mean large voltage drop across it due to zero signal collector current. Consequently, a higher collector supply will be needed.

Consistency of Gain.

An important advantage of negative feedback is that the resultant gain of the amplifier can be made independent of transistor parameters or the supply voltage.

$$A_{vf} = \frac{A_v}{1 + A_v m_v}$$

For negative voltage feedback in an amplifier to be effective, the designer deliberately makes the product ($A_v \times m_v$) much greater than unity. Therefore, in the above equation, the "1" can be neglected and the equation becomes $1/m_v$. The gain now depends only upon the feedback fraction m_v .

f.

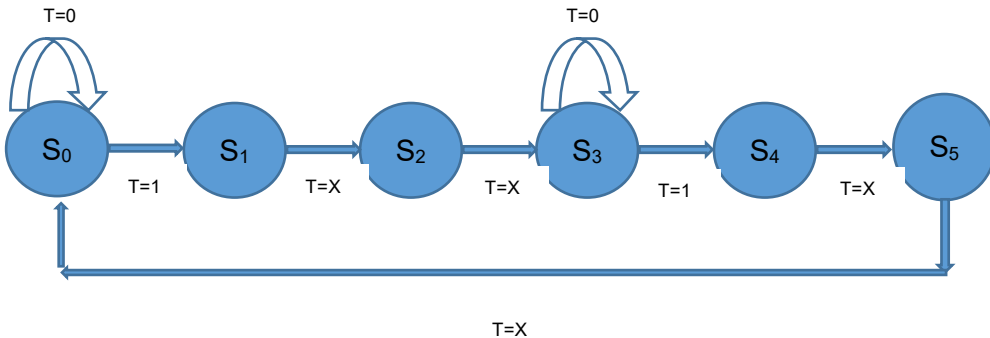
$$\begin{aligned} f_r &= \frac{1}{2\pi\sqrt{LC}} \\ &= \frac{1}{2\pi \times \sqrt{47m \times 0.33u}} \\ &= 1.28\text{KHz} \end{aligned}$$

**Any 3, 2
marks
each**

3

Q.B2	Question	Marks
a.	$a_1 = 5.6334$ $a_2 = 0.7620, b_2 = 2.6530$ $a_3 = 0.1172, b_3 = 1.0686$ <u>Stage 1</u> $R_1 = \frac{a_1}{2\pi f_c C_1}$ $= \frac{5.6334}{2\pi \times 100k \times 220p}$ = 40.75kΩ <u>Stage 2</u> $C_2 \geq \frac{C_1 \times 4b}{a^2}$ $\geq \frac{220p \times 4 \times 2.6530}{0.7620^2} \geq 4nF$ Taking C2 as 5nF $R = \frac{a_i C_2 \pm \sqrt{a_i^2 C_2^2 - 4b_i C_1 C_2}}{4\pi f_c C_1 C_2}$ $R1 = \frac{0.762 \times 5n - \sqrt{(0.762 \times 5n)^2 - 4 \times 2.653 \times 220p \times 5n}}{4\pi \times 100k \times 220p \times 5n} = 1.54k\Omega$ $R2 = \frac{0.762 \times 5n + \sqrt{(0.762 \times 5n)^2 - 4 \times 2.653 \times 220p \times 5n}}{4\pi \times 100k \times 220p \times 5n} = 3.98k\Omega$ <u>Stage 3</u> $C_2 \geq \frac{C_1 \times 4b}{a^2}$ $\geq \frac{220p \times 4 \times 1.0686}{0.1172^2} \geq 68nF$ Taking C2 as 70nF $R = \frac{a_i C_2 \pm \sqrt{a_i^2 C_2^2 - 4b_i C_1 C_2}}{4\pi f_c C_1 C_2}$ $R1 = \frac{0.1172 \times 70n - \sqrt{(0.1172 \times 70n)^2 - 4 \times 1.0686 \times 220p \times 70n}}{4\pi \times 100k \times 220p \times 70n} = 361\Omega$ $R2 = \frac{0.1172 \times 70n + \sqrt{(0.1172 \times 70n)^2 - 4 \times 1.0686 \times 220p \times 70n}}{4\pi \times 100k \times 220p \times 70n} = 487\Omega$	1 1 1 1 1 2 1 3 3 1 1 2 2

b.	$m_v = \frac{C_1}{C_2}$ 0.25 = C₁/C₂, therefore C₂ = 4C₁ $f = \frac{1}{2\pi\sqrt{LC_T}}$ Rearranging for C_T $C_T = \frac{1}{L(2\pi f)^2}$ $= \frac{1}{20\mu \times (2\pi \times 30M)^2} = 1.4\text{pF}$ $C_T = \frac{C_1 C_2}{C_1 + C_2}$ Dividing top and bottom by C₁ gives $\frac{C_2}{1 + \frac{C_2}{C_1}}$ If C₁/C₂ = 0.25, then C₂/C₁ = 4 and $1.4p = \frac{C_2}{1 + 4} = \frac{C_2}{5}$ ∴ C₂ = 1.4p × 5 = 7pF and C₁ = $\frac{C_2}{4} = 1.76\text{pF}$	1 3 2 1
c.	$f = \frac{1}{2\pi\sqrt{LC}}$ $= \frac{1}{2\pi\sqrt{47\mu \times 300p}}$ = 1.34MHz	1 2

Q. B3	Question	Marks																																																																																																																																																																																																																			
a.	<u>Allocate states and draw state diagram</u> $S_0 = \text{Red}, S_1 = \text{Red/Amber}, S_2 = \text{Red/amber}, S_3 = \text{Green}, S_4 = \text{Amber}, S_5 = \text{Amber}$  <u>Draw State table</u> <table><tr><th rowspan="3">Current</th><th colspan="2">Next</th><th colspan="6">Next</th><th colspan="3" rowspan="2">Output</th></tr><tr><th rowspan="2">T=0</th><th rowspan="2">T=1</th><th colspan="3">T=0</th><th colspan="3">T=1</th></tr><tr><th>Q_A^+</th><th>Q_B^+</th><th>Q_C^+</th><th>Q_A^+</th><th>Q_B^+</th><th>Q_C^+</th><th>R</th><th>A</th><th>G</th></tr><tr><td>S0</td><td>S0</td><td>S1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td></tr><tr><td>S1</td><td>S2</td><td>S2</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td></tr><tr><td>S2</td><td>S3</td><td>S3</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td></tr><tr><td>S3</td><td>S3</td><td>S4</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td></tr><tr><td>S4</td><td>S5</td><td>S5</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td></tr><tr><td>S5</td><td>S0</td><td>S0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td></tr></table> <u>Draw Karnaugh Maps</u> <table><caption>Q_A^+</caption><tr><th>BC</th><th>00</th><th>01</th><th>11</th><th>10</th></tr><tr><th>TA</th><td></td><td></td><td></td><td></td></tr><tr><th>00</th><td>0</td><td>0</td><td>0</td><td>0</td></tr><tr><th>01</th><td>1</td><td>0</td><td>X</td><td>X</td></tr><tr><th>11</th><td>1</td><td>0</td><td>X</td><td>X</td></tr><tr><th>10</th><td>0</td><td>0</td><td>1</td><td>0</td></tr></table><table><caption>Q_B^+</caption><tr><th>BC</th><th>00</th><th>01</th><th>11</th><th>10</th></tr><tr><th>TA</th><td></td><td></td><td></td><td></td></tr><tr><th>00</th><td>0</td><td>1</td><td>1</td><td>1</td></tr><tr><th>01</th><td>0</td><td>0</td><td>X</td><td>X</td></tr><tr><th>11</th><td>0</td><td>0</td><td>X</td><td>X</td></tr><tr><th>10</th><td>0</td><td>1</td><td>0</td><td>1</td></tr></table> <table><caption>Q_C^+</caption><tr><th>BC</th><th>00</th><th>01</th><th>11</th><th>10</th></tr><tr><th>TA</th><td></td><td></td><td></td><td></td></tr><tr><th>00</th><td>0</td><td>0</td><td>1</td><td>1</td></tr><tr><th>01</th><td>1</td><td>0</td><td>X</td><td>X</td></tr><tr><th>11</th><td>1</td><td>0</td><td>X</td><td>X</td></tr><tr><th>10</th><td>1</td><td>0</td><td>0</td><td>1</td></tr></table><table><caption>Red</caption><tr><th>BC</th><th>00</th><th>01</th><th>11</th><th>10</th></tr><tr><th>A</th><td></td><td></td><td></td><td></td></tr><tr><th>0</th><td>1</td><td>1</td><td>0</td><td>1</td></tr><tr><th>1</th><td>0</td><td>0</td><td>X</td><td>X</td></tr></table>	Current	Next		Next						Output			T=0	T=1	T=0			T=1			Q_A^+	Q_B^+	Q_C^+	Q_A^+	Q_B^+	Q_C^+	R	A	G	S0	S0	S1	0	0	0	0	0	1	1	0	0	S1	S2	S2	0	1	0	0	1	0	1	1	0	S2	S3	S3	0	1	1	0	1	1	1	1	0	S3	S3	S4	0	1	1	1	0	0	0	0	1	S4	S5	S5	1	0	1	1	0	1	0	1	0	S5	S0	S0	0	0	0	0	0	0	0	1	0	BC	00	01	11	10	TA					00	0	0	0	0	01	1	0	X	X	11	1	0	X	X	10	0	0	1	0	BC	00	01	11	10	TA					00	0	1	1	1	01	0	0	X	X	11	0	0	X	X	10	0	1	0	1	BC	00	01	11	10	TA					00	0	0	1	1	01	1	0	X	X	11	1	0	X	X	10	1	0	0	1	BC	00	01	11	10	A					0	1	1	0	1	1	0	0	X	X	2
	Current		Next		Next											Output																																																																																																																																																																																																					
			T=0	T=1	T=0			T=1																																																																																																																																																																																																													
		Q_A^+			Q_B^+	Q_C^+	Q_A^+	Q_B^+	Q_C^+	R	A	G																																																																																																																																																																																																									
	S0	S0	S1	0	0	0	0	0	1	1	0	0																																																																																																																																																																																																									
S1	S2	S2	0	1	0	0	1	0	1	1	0																																																																																																																																																																																																										
S2	S3	S3	0	1	1	0	1	1	1	1	0																																																																																																																																																																																																										
S3	S3	S4	0	1	1	1	0	0	0	0	1																																																																																																																																																																																																										
S4	S5	S5	1	0	1	1	0	1	0	1	0																																																																																																																																																																																																										
S5	S0	S0	0	0	0	0	0	0	0	1	0																																																																																																																																																																																																										
BC	00	01	11	10																																																																																																																																																																																																																	
TA																																																																																																																																																																																																																					
00	0	0	0	0																																																																																																																																																																																																																	
01	1	0	X	X																																																																																																																																																																																																																	
11	1	0	X	X																																																																																																																																																																																																																	
10	0	0	1	0																																																																																																																																																																																																																	
BC	00	01	11	10																																																																																																																																																																																																																	
TA																																																																																																																																																																																																																					
00	0	1	1	1																																																																																																																																																																																																																	
01	0	0	X	X																																																																																																																																																																																																																	
11	0	0	X	X																																																																																																																																																																																																																	
10	0	1	0	1																																																																																																																																																																																																																	
BC	00	01	11	10																																																																																																																																																																																																																	
TA																																																																																																																																																																																																																					
00	0	0	1	1																																																																																																																																																																																																																	
01	1	0	X	X																																																																																																																																																																																																																	
11	1	0	X	X																																																																																																																																																																																																																	
10	1	0	0	1																																																																																																																																																																																																																	
BC	00	01	11	10																																																																																																																																																																																																																	
A																																																																																																																																																																																																																					
0	1	1	0	1																																																																																																																																																																																																																	
1	0	0	X	X																																																																																																																																																																																																																	

Amber				
BC	00	01	11	10
A				
0	0	1	0	1
1	1	1	X	X

Green				
BC	00	01	11	10
A				
0	0	0	1	0
1	0	0	X	X

Derive Boolean Expressions

$$Q_A^+ = A\bar{C} + TBC$$

$$Q_B^+ = \bar{T}B + B\bar{C} + \bar{A}\bar{B}C$$

$$Q_C^+ = A\bar{C} + T\bar{C} + \bar{T}B$$

$$Red = \bar{A}\bar{B} + B\bar{C}$$

$$Amber = A + \bar{B}C + B\bar{C}$$

$$Green = BC$$

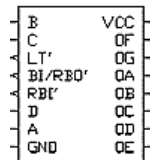
b.i

The inputs are A, B, C, D, LT, RBI and BI.

The outputs are OA, OB, OC, OD, OE, OF, OG.

ii.

The entity is:



iii.

Truth Table

DECIMAL OR FUNCTION	LT	RBI	D	C	B	A	BI/RBO	$\bar{a}$	$\bar{b}$	$\bar{c}$	$\bar{d}$	$\bar{e}$	$\bar{f}$	$\bar{g}$
0	H	H	L	L	L	L	H	L	L	L	L	L	L	H
1	H	X	L	L	L	H	H	H	L	L	H	H	H	H
2	H	X	L	L	H	L	H	L	L	H	L	L	H	L
3	H	X	L	L	H	H	H	L	L	L	L	H	H	L
4	H	X	L	H	L	L	H	H	L	L	H	H	L	L
5	H	X	L	H	L	H	H	L	H	L	L	H	L	L
6	H	X	L	H	H	L	H	H	H	L	L	L	L	L
7	H	X	L	H	H	H	H	L	L	L	H	H	H	H
8	H	X	H	L	L	L	H	L	L	L	L	L	L	L
9	H	X	H	L	L	H	H	L	L	L	H	H	L	L

LT is an active low lamp test which turns on all the segments when LT = 0

RBI and BI control the ripple blanking which turns off unused displays

A, B, C, D are the input signals and take the binary value of the decimal number to be displayed.

a, b, c, d, e, f, g are the drive signals to each of the segments in the display.

3

2

2

2

1

1

1

1

1

2

4