



12 Pages

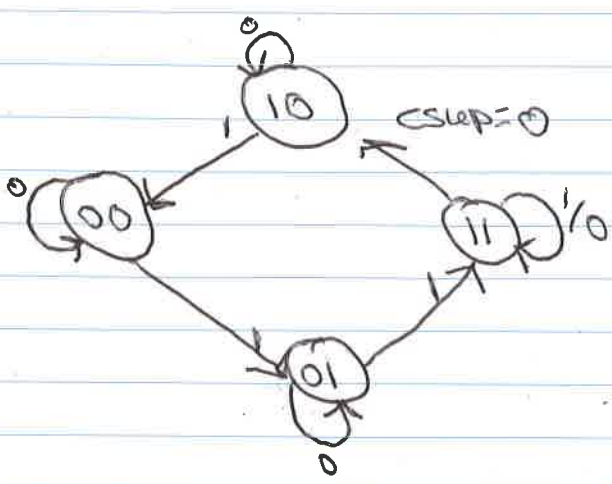
1. Please give the information requested in the boxes below.
2. Enter your name in the space provided to the right, fold over and seal down (using the label provided) to hide your name.
3. The answers must be legibly written. The Examiners can either ignore illegible script or have it typed and the expense of typing charged to the candidate.
4. Write your answers in ink.
5. Begin each answer on a fresh page. Do all rough work in the answer book and cross it through.
6. No part of this book is to be torn out; it must be handed in complete.
7. If more books than one are used, fasten them together using the tags available from the invigilator(s).
8. **Every book must be handed in. In no circumstances may answer books, used or unused, be taken out of the examination venue.**

FORENAME(S): Daniel Martin

List the numbers of the questions you have attempted	Office Use
Q1	455
Q2	113
Q3	110
Total	275

Steve Dorsey

1
2



3 ✓

3

State	Next state
00	01
01	11
11	10
10	00

State		Next state		
x	y			
0	0	0	0	0
0	1	0	0	1
1	0	0	1	0
1	1	0	0	0
1	1	0	1	1

2

AB

C	00	01	11	10
0	0	1	1	1
1	0	0	0	1

$\bar{C} \cdot B \cdot \bar{D}$
+
 $A \cdot D$

AB

C	00	01	11	10
0	0	X	1	1
1	0	0	X	1

$A \cdot \bar{C}$
+
 $A \cdot \bar{B}$

5

A	B	C	D	$\bar{C} \cdot B \cdot \bar{D}$	$A \cdot D$	$A \cdot \bar{C}$	$A \cdot \bar{B}$
0	0	0	0				
0	0	0	1				
0	0	1	0				
0	0	1	1				
0	1	0	0	1			
0	1	0	1				
0	1	1	0				
0	1	1	1				
1	0	0	0		1		
1	0	0	1		1		
1	0	1	0			1	
1	0	1	1			1	
1	1	0	0				1
1	1	0	1				1
1	1	1	0				
1	1	1	1				

8

```
1  -----
2  -- Company:
3  -- Engineer:
4  --
5  -- Create Date:    11:51:10 05/18/2018
6  -- Design Name:
7  -- Module Name:    Q3_DL - Behavioral
8  -- Project Name:
9  -- Target Devices:
10 -- Tool versions:
11 -- Description:
12 --
13 -- Dependencies:
14 --
15 -- Revision:
16 -- Revision 0.01 - File Created
17 -- Additional Comments:
18 --
19  -----
20 library IEEE;
21 use IEEE.STD_LOGIC_1164.ALL;
22
23 -- Uncomment the following library declaration if using
24 -- arithmetic functions with Signed or Unsigned values
25 --use IEEE.NUMERIC_STD.ALL;
26
27 -- Uncomment the following library declaration if instantiating
28 -- any Xilinx primitives in this code.
29 --library UNISIM;
30 --use UNISIM.VComponents.all;
31
32 entity Q3_DL is
33     Port ( x : in  STD_LOGIC;
34           CLK : in  STD_LOGIC;
35           y : out STD_LOGIC);
36 end Q3_DL;
37
38 architecture Behavioral of Q3_DL is
39
40     type state_type is (state_1, state_2, state_3, state_4, state_5, state_6,
41 state_7, state_8);
42     signal present_state : state_type;
43     signal next_state : state_type;
44
45 begin
46     state : process (x, present_state)
47     begin
48         if x = '0' then
49             case present_state is
50                 when state_1 => next_state <= state_1;
51                 when state_2 => next_state <= state_5;
52                 when state_3 => next_state <= state_4;
53                 when state_5 => next_state <= state_6;
54                 when state_6 => next_state <= state_8;
55                 when state_7 => next_state <= state_8;
56                 when state_8 => next_state <= state_2;
```

```
56         when others => null;
57     end case present_state;
58
59     else if x='1' then
60         case present_state is
61             when state_1 => next_state <= state_1;
62             when state_2 => next_state <= state_5;
63             when state_3 => next_state <= state_4;
64             when state_4 => next_state <= state_6;
65             when state_5 => next_state <= state_6;
66             when state_6 => next_state <= state_8;
67             when state_7 => next_state <= state_8;
68             when state_8 => next_state <= state_2;
69             when others => null;
70         end case present_state;
71     end if;
72 end if;
73 end process state;
74
75 clock :process (clk)
76 begin
77     if (clk='0') and (clk' last_value='1') then
78         present_state => next_state;
79     end if;
80 end process clock;
81
82
83 end Behavioral;
84
85
```