

SURNAME: PAN

FORENAME(S): Gabriel

12 Pages

1. Please give the information requested in the boxes below.
2. Enter your name in the space provided to the right, fold over and seal down (using the label provided) to hide your name.
3. The answers must be legibly written. The Examiners can either ignore illegible script or have it typed and the expense of typing charged to the candidate.
4. Write your answers in ink.
5. Begin each answer on a fresh page. Do all rough work in the answer book and cross it through.
6. No part of this book is to be torn out; it must be handed in complete.
7. If more books than one are used, fasten them together using the tags available from the invigilator(s).
8. **Every book must be handed in. In no circumstances may answer books, used or unused, be taken out of the examination venue.**

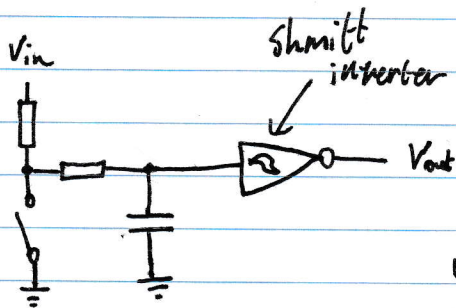
List the numbers of the questions you have attempted	Office Use
1	7
2	5
3	3
4	7
5	5
6	0
	27
Total	34%

(Gweler yr ochr arall am y fersiwn Cymraeg)

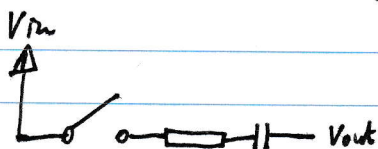
Q1.

- a). RETURN = return to subroutine = continue to the main subroutine for further commands
- b). SLEEP = standby = Enter standby mode (do nothing) until commanded otherwise
- c). ADDLW = ADD literal with W = perform an addition with the values of a specified value and the W register
- d). BCF, b = Bit check F, bitwise = check individual bits in the F register
- e). DECF = decrement F = Subtract 1 from the value of F register

Q2.

Method 1.

The First method is using a RC Switch debouncer. This uses a Schmitt inverter to produce the output when the switch is used by the energy of the capacitor, this is allowed to happen because when the switch is on the current will flow to ground, then the capacitor will discharge.

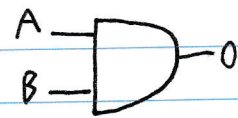
Method 2.

The Second is a simple RC circuit which operates by using a capacitor to store the voltage which is bouncing then allow it to flow as a steady increase when the switch is actuated.

Q3.

logic symbol for an AND gate:

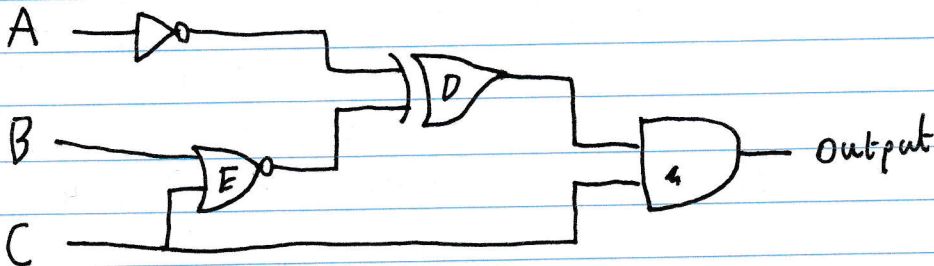
$A \cdot B = 0$ or



A	B	O
0	0	0
0	1	0
1	0	0
1	1	1

Q4.

a).



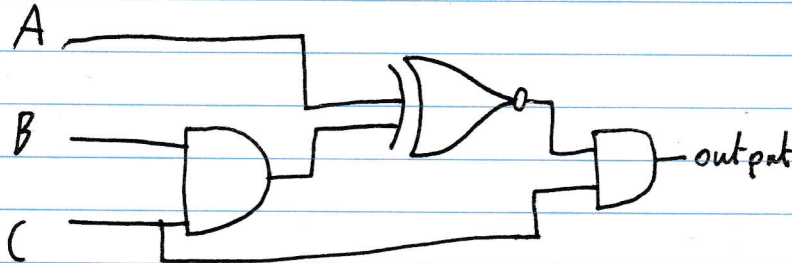
A	B	C	D	E	Output
0	0	0	0	1	0
0	0	1	1	0	1
0	1	0	1	0	0
0	1	1	1	0	1
1	0	0	1	1	0
1	0	1	0	0	0
1	1	0	0	0	0
1	1	1	0	0	0

A	B	AB	0
0	0	0	0
0	1	1	1
1	0	1	1
1	1	0	0

6). $(\bar{A} \oplus \bar{B+C}) \cdot C = \text{output}$

$$= (\bar{A} \oplus \bar{B} \cdot \bar{C}) \cdot C = (\bar{A} \oplus \bar{B} \cdot \bar{C}) \cdot C$$

• Output logic 1 when $A = 0$
and $C = 1$



Q5.

Harvard:

Arithmetic logic unit

Instruction memory

Control unit

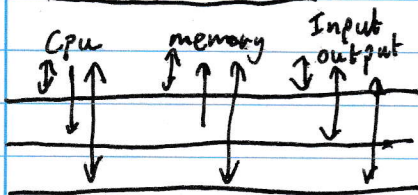
data memory

I/O

The Harvard controller architecture operates by using separate buses for all subsystems allowing simultaneous access to all memory. This allows the Harvard architecture to be very efficient and quick at processing, especially in ~~embedded~~ systems such as Embedded systems and DSP (digital signal processing).

Von neumann:

Control address data



The Von neumann controller architecture operates by using the same bus for connecting most subsystems like instructions and data. This allows the architecture to be very space efficient, but this also means that it can encounter performance bottlenecks. This means it is very useful in systems that prioritise convenience over processing power/speed, systems like PCs (personal computers) for general computing.

Question No.

6).