

**MODULE CODE:** ACDA6001  
**TITLE:** Electronics II  
**DATED:** 16/08/2018

**LEVEL:** 6  
**CREDITS:** 20

**JACS CODE:** H610

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### **AIM(S)**

To develop an advanced appreciation of the structure and design of digital systems and finite state machines in particular.

### **LEARNING OUTCOMES**

Upon the successful completion of this module, the student should be able to:

1. Synthesis and critically evaluate of innovative VHDL designs through the use of state of the art simulation and synthesis software.
2. Implement advanced digital designs including multi-input systems controllers.

### **INDICATIVE CONTENT**

- Review of combinational and sequential circuit design including finite state machines.
- System controller design: system synchronisation, handshaking, state assignment, next state decoder, output decoder.
- PLDs and FPGAs.
- VHDL: model development, behavioural modelling, the VHDL language, program design, modelling FSMs.
- Schematic capture, synthesis and simulation tools for PLD and FPGA design (e.g. Mentor Graphics, Altera and Xilinx).

### **LEARNING AND TEACHING STRATEGY**

The study time for the module is divided as follows:

| <b>Activity type</b> | <b>Hours</b> | <b>Percentage</b> |
|----------------------|--------------|-------------------|
| Scheduled learning   | 60           | 30%               |
| Independent learning | 140          | 70%               |
| Placement learning   | 0            | 0%                |
| <b>TOTAL</b>         | <b>200</b>   | <b>100%</b>       |

## ASSESSMENT

### Assessment Component 1

☐ Written exam      ☒ Coursework      ☐ Practical

| Mode of assessment | Volume     | Weighting |
|--------------------|------------|-----------|
| Assignment Report  | 2500 Words | 50%       |

### Assessment Component 2

☒ Written exam      ☐ Coursework      ☐ Practical

| Mode of assessment | Volume  | Weighting |
|--------------------|---------|-----------|
| Exam               | 2 Hours | 50%       |

### Assessment Summary

| Activity type | Percentage  |
|---------------|-------------|
| Written exam  | 50%         |
| Coursework    | 50%         |
| Practical     | 0%          |
| <b>TOTAL</b>  | <b>100%</b> |

## READING LIST

| Module Code    | ACDA6001                                                                                                                 |                                     |
|----------------|--------------------------------------------------------------------------------------------------------------------------|-------------------------------------|
| Module Title   | Electronics II                                                                                                           |                                     |
| Classification | Reading List entry                                                                                                       | Electronic*                         |
| Essential      | Ashenden, P (2007), Digital Design (VHDL): An Embedded Systems Approach Using VHDL , Morgan Kaufmann                     | <input checked="" type="checkbox"/> |
| Essential      | Brown, S and Vranesic, Z (2008), Fundamentals of Digital Logic with VHDL Design, Mc Graw Hill<br><br>ISBN-10: 0077221435 | <input type="checkbox"/>            |
| Further        | Haskell, R and Hanna, D (2015), VHDL by Example, LBE Books                                                               | <input type="checkbox"/>            |