

LEVEL 4 ASSESSMENT SPECIFICATION

Student name:	Oliver Evans	Student ID number:	
Programme:	HNC Electrical/Electronic Engineering		
Module:	Electronics		
Module code:	PCEE4006	Contribution to Overall Module Assessment (%):	50%
Lecturer:	Jason Pointer	Internal Verifier:	Nigel Richards
Assignment Title:	Diodes and Amplifiers	Word count (or equivalent):	2000
Submission deadline:	19/01/23	Return date of provisional marks & written feedback:	02/02/23
Submission method:	All written assessments, where practical and possible, must be submitted via Turnitin unless otherwise instructed by the Lecturer. (Please DO NOT put this assessment specification into Turnitin or it will match many similarities with other students' submissions.) Alternative submission method (if applicable): Late submission of the assessment will result in a late penalty mark. Penalties for late submission: Up to one week late, maximum mark of 40%. Over one week late, 0%. Only the Extenuating Circumstances Panel may approve a change to submission dates.		
Academic honesty / referencing:	Academic honesty is required. In the main body of your submission you must give credit to authors on whose research and ideas your work is based. Append to your submission a reference list that indicates the books, articles, etc. that you have used, cited or quoted in order to complete this assessment.		

Module Learning Outcomes (from module syllabus)

1. Demonstrate an understanding of semi-conductor components and characteristics and their application in **analogue** and digital electronic circuits.
2. To design, simulate, build, test and evaluate **analogue** and digital electronic circuits using information gained from datasheets.

STUDENT FEEDBACK FORM

This section details the *extent* to which the assessment criteria are demonstrated by you, which in turn determines your mark. The marks available for each category of skill are shown. Lecturers will use the space provided to comment on the achievement of the task(s), including those areas in which you have performed well and areas that would benefit from development/improvement.

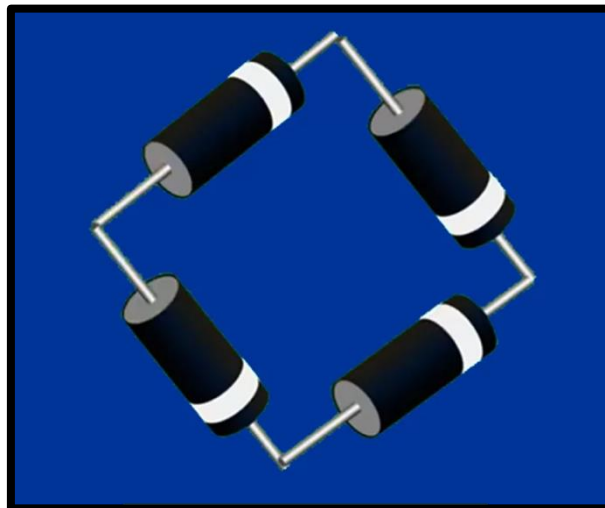
Generic Assessment Criteria	Marks available	Marks awarded
1. Engagement with Literature Skills	10	6.2
Engagement with a wide range of literature sources, including sources retrieved independently. Generally sound referencing, with very few inaccuracies or inconsistencies.		
2. Knowledge and Understanding Skills	35	25.7
Task 1 achieved 75%. Task 2 achieved 70%, Task 3 achieved 75%. Excellent knowledge and understanding of the basic underlying concepts and principles of the subject. Showed excellent understanding the calculated requirements and design work.		
3. Cognitive and Intellectual Skills	15	9.8
Sound evaluation of the underlying concepts and principles for all tasks.		
4. Practical Application Skills	30	22.8
Task 1 achieved 79%. Task 2 achieved 77%. Task 3 achieved 72%. An excellent application of practical work for all tasks, very good use of the test equipment and Multisim to obtain the required test results.		
5. Transferable Skills for Life and Professional Practice	10	7.5
Work is coherent, very fluent and is presented professionally. Excellent layout making the assignment easy to read.		

Assessment Mark (Assessment marks are subject to ratification at the Exam Board. These comments and marks are to give feedback on module work and are for guidance only until they are confirmed.)	Late Submission Penalties (tick if appropriate)		72%
	Up to 1 week late (40% Max)		
	Over 1 week late (0%)		



Diodes & Amplifiers

The design, simulation, build and testing of semi-conductor components and circuits.



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Assignment 1

PCEE4006
J Pointer

20/10/22

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Task 1 – Characteristics of Diodes

a)

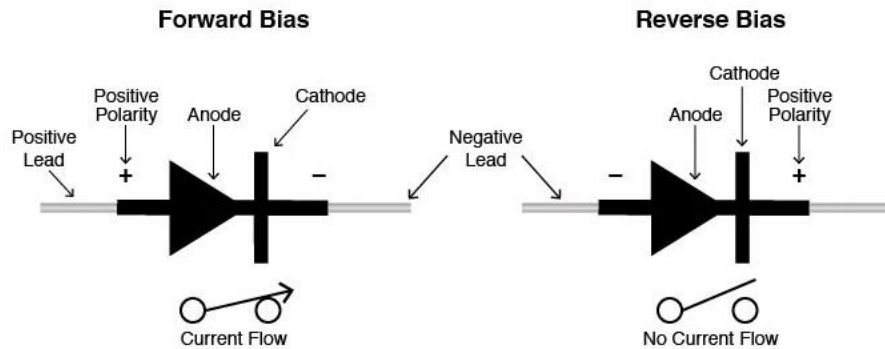


Figure 1 – Diode Working Principle Diagram

A diode is a semiconductor device that is essentially a non-return (one way) valve for current. During normal operation this device allows the current to flow through the diode with little resistance in one direction, but severely restricts current flowing in the opposite direction.

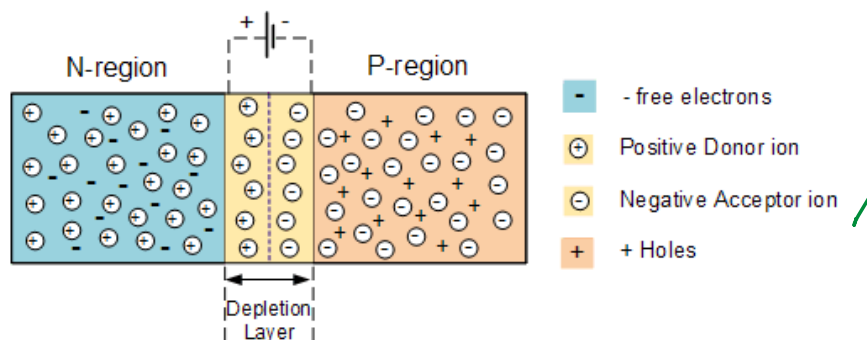


Figure 2 – P-N Junction Working Principle Diagram

A P-N junction is an interface between two types of semiconductor materials; N-type and P-type. The function of a P-N junction is to allow current in one direction, which is called a forward biased condition and to block current in the other direction, called the reverse biased condition.

In figure 2 there is the N-region which has a surplus of free electrons and the P-region which has a surplus of holes. The free electrons from the N-region start to diffuse into the P-region and the holes in the P-region start to diffuse across into the N-region. Each electron which diffuses across the junction and combines with a hole, a positive charge is left in the N-region and a negative charge in the P-region. This barrier of positive and negatively charges is called the depletion layer due to each region being depleted of electrons and holes, this what controls the flow of current.

There is a barrier potential formed across the depletion layer, this is the amount of voltage required to move the electrons through the electric field. A voltage exceeded this barrier potential must be applied in the correct polarity before electrons flow across the junction. Typical barrier potential at 25°C for silicon is 0.7V and for germanium 0.3V.

In the forward bias where positive terminal of the supply is connected to anode and negative terminal to cathode, the depletion region is narrow meaning resistance is low allowing maximum current flow. With reverse bias the positive terminal is instead connected to the cathode and the negative terminal connected to the anode. Here the depletion regions get wider restricting current flow as there is a high resistance. There is an extremely low current flow present known as leakage current. Also, to be noted breakdown can occur if a high reverse bias input voltage is placed across the diode which results in permanent damage to the diode.

Experiment

For this task the forward and reverse characteristics of both a germanium (Ge) and a silicon (Si) diode will be recorded. Following the experimental procedure, both diodes had to be checked using a multimeter, this was to confirm the polarity and ensure the reliability of the component. Due to the tolerances of $\pm 5\%$ the true value of the resistor used in the circuit is 987Ω .

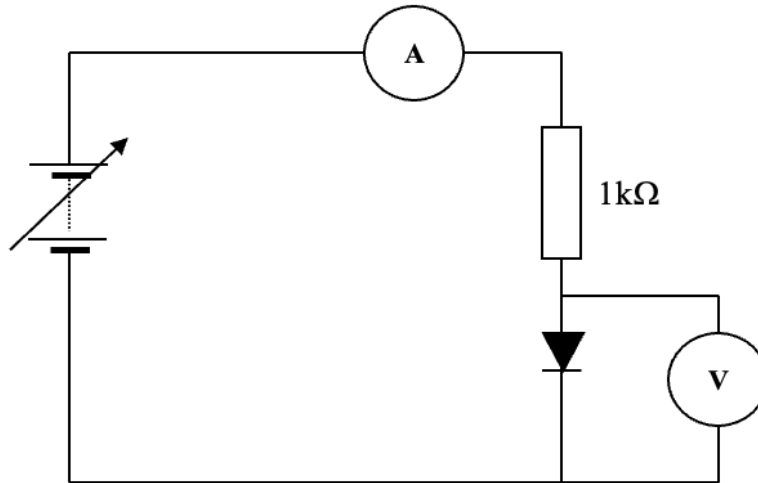


Figure 3 – Forward Bias Circuit Diagram

When conducting the test for the forward bias the circuit was set up in the configuration shown in figure 3. In this circuit one multimeter is in series with the resistor measuring amps, a second multimeter is then in parallel with the diode measuring the voltage.

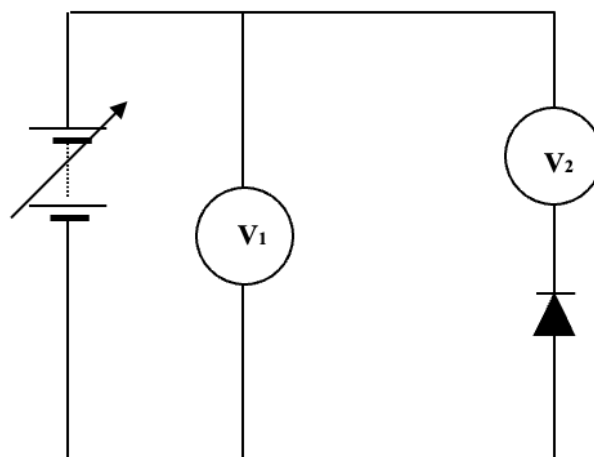


Figure 4 – Reverse Bias Circuit Diagram

The circuit shown in figure 4 is the configuration used when carrying out the test for the reverse bias. One multimeter is in parallel measuring voltage across the diode and a second multimeter is in series with the diode measuring millivoltage. The reason the voltage is measured as opposed to current is multimeter have an internal resistance of $10M\Omega$, this would alter the results as it would bypass the diode. ✓

Results

Diode Test					
Silicon Diode					
Forward Direction		Reverse Direction			
Voltage V	Current mA	V1 V	V2 mV	Diode Voltage V	Current nA
0	0	0	0	0.000	0.000
0.1	0.00003	-1.5	-56.6	-1.443	-5.660
0.2	0.002	-3	-68.9	-2.931	-6.890
0.3	0.00136	-4.5	-80.4	-4.420	-8.040
0.4	0.0104	-6	-84.3	-5.916	-8.430
0.5	0.0832	-7.5	-89.2	-7.411	-8.920
0.6	0.642	-9	-86.9	-8.913	-8.690
0.7	5.25	-10.5	-90	-10.410	-9.000
0.8	33.2	-12	-95.2	-11.905	-9.520
0.9		-13.5	-91.6	-13.408	-9.160
1		-15	-97.2	-14.903	-9.720

Figure 5 – Silicon Diode Test Results

Diode Test					
Germanium Diode					
Forward Direction		Reverse Direction			
Voltage V	Current mA	V1 V	V2 mV	Diode Voltage V	Current μA
0	0	0	0	0.000	0
0.1	0.01356	-1.5	-22.2	-1.478	-2.22
0.2	0.598	-3	-48.9	-2.951	-4.89
0.3	0.847	-4.5	-91.5	-4.409	-9.15
0.4	1.929	-6	-150	-5.850	-15
0.5	3.31	-7.5	-225	-7.275	-22.5
0.6	4.95	-9	-317	-8.683	-31.7
0.7	6.8	-10.5	-423	-10.077	-42.3
0.8	8.82	-12	-550	-11.450	-55
0.9	11.02	-13.5	-687	-12.813	-68.7
1	13.35	-15	-841	-14.159	-84.1

Figure 6 – Germanium Diode Test Results

Static Characteristics Forward Direction

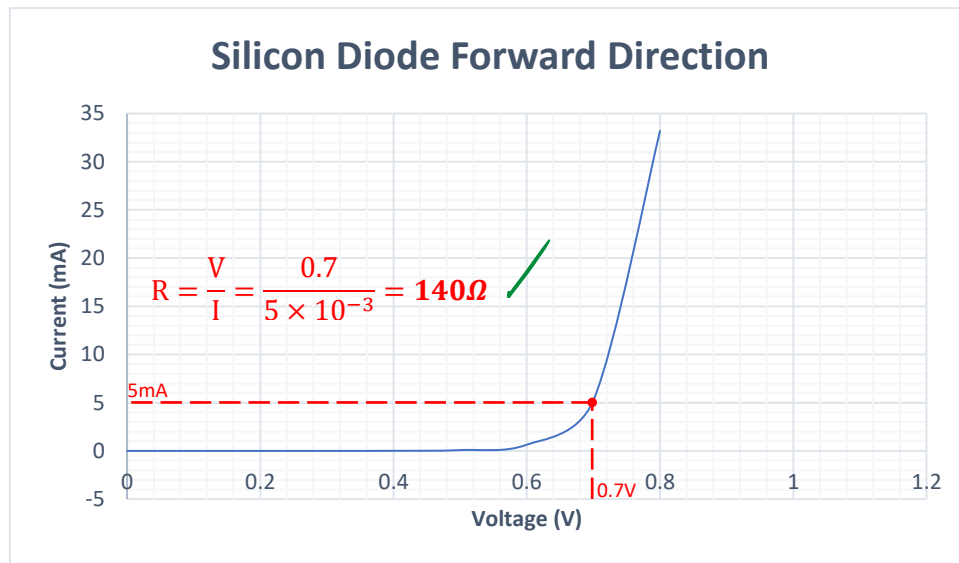


Figure 7 – Silicon Diode Forward Bias Curve (Static)

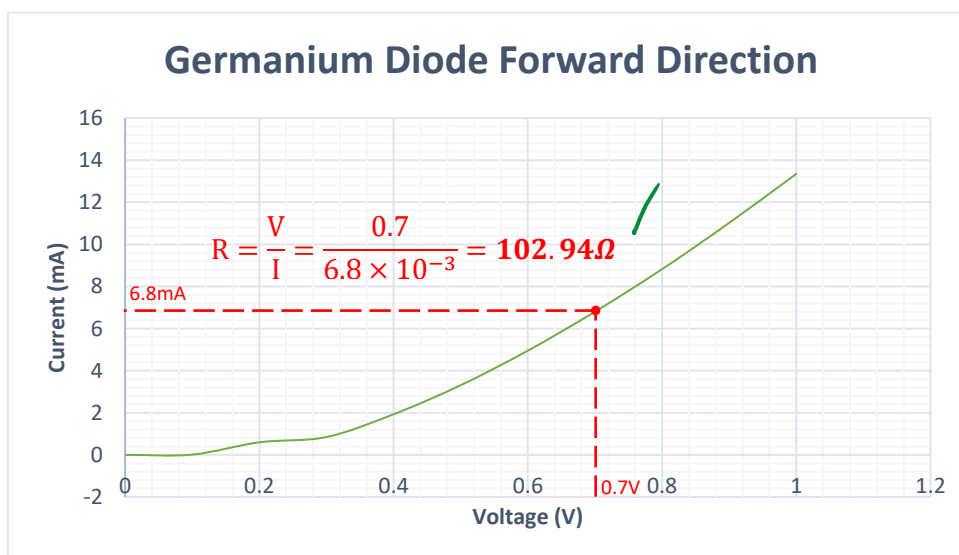


Figure 8 – Germanium Diode Forward Bias Curve (Static)

When comparing figure 7 & 8 the Ge diode conducts much sooner as it has a threshold voltage of 0.3V whereas the Si diode's threshold voltage is 0.7V. what should be stated is the Si diode conducts much more rapidly than the Ge.

The static characteristics show a higher resistance with the Si diode than the Ge, as this characteristic was taken at a fixed resistance using ohms law is it clear as the current is higher with the germanium the resistance would indeed be lower.

Dynamic Characteristics Forward Direction

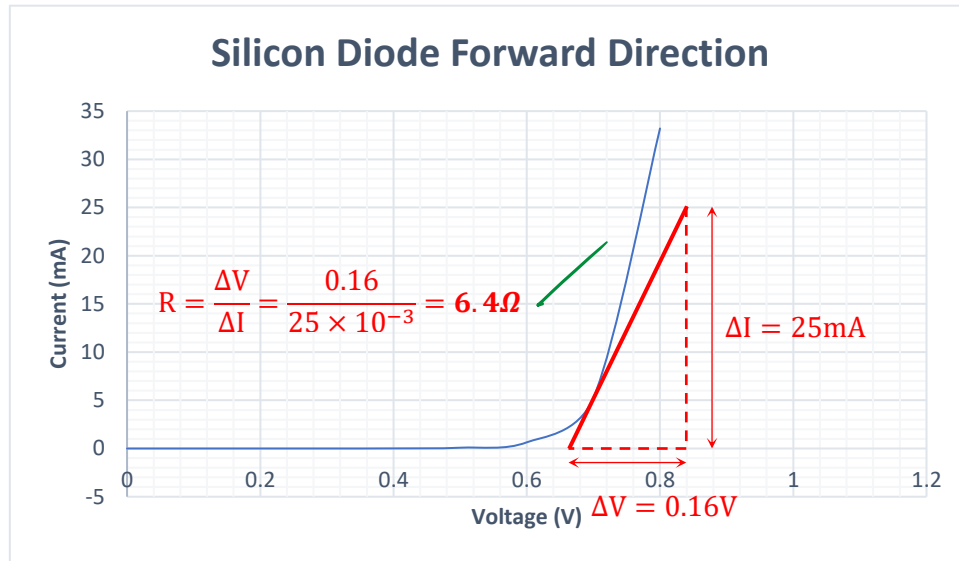


Figure 9 – Silicon Diode Forward Bias Curve (Dynamic)

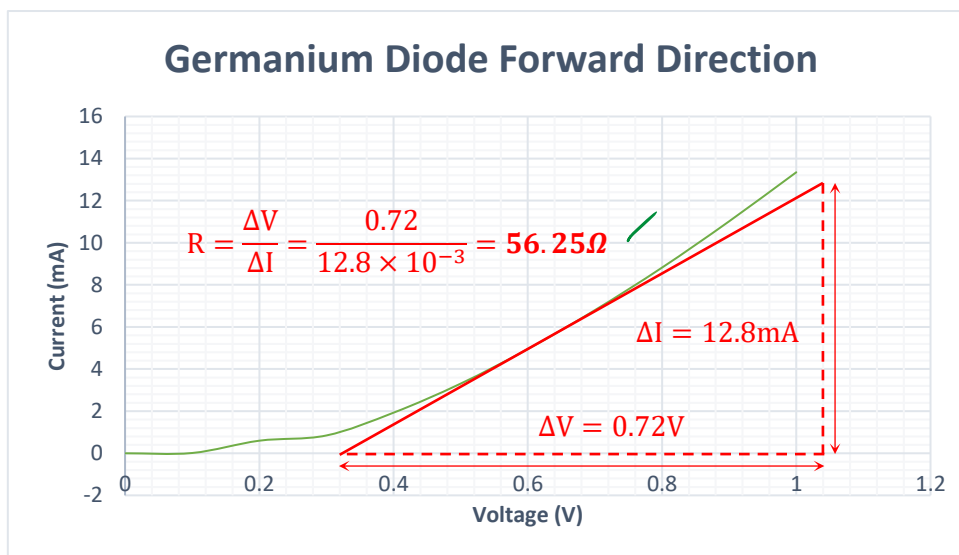


Figure 10 – Germanium Diode Forward Bias Curve (Dynamic)

When looking at figure 9 & 10 there is a lower dynamic resistance in the Si diode than there is in the Ge. This result could be due to the Ge diode conducting earlier at a lower voltage, this allowed greater range for the delta to be taken over.

Dynamic characteristics can portray the characteristics over the course of the experiment, this considers changes over time where the static characteristics is a “static” point showing a fixed time. Dynamic characteristics gives a better average reading overall compared to static.

Static Characteristics Reverse Direction

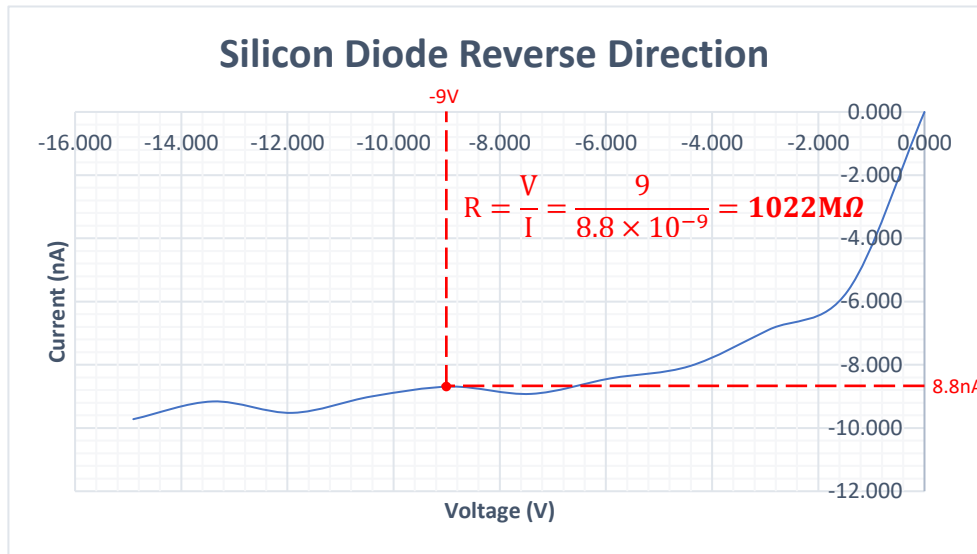


Figure 11 – Silicon Diode Reverse Bias Curve (Static)

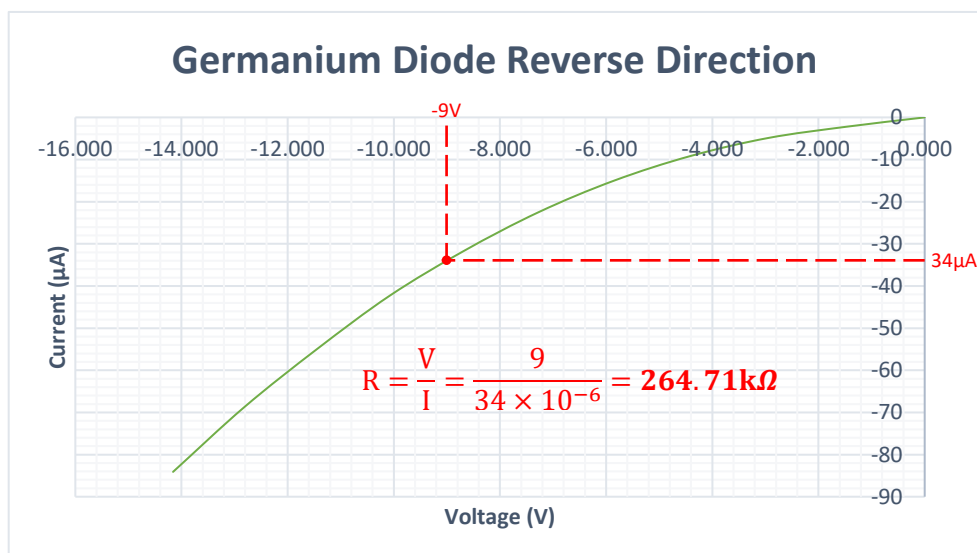


Figure 12 – Germanium Diode Reverse Bias Curve (Static)

Figures 11 & 12 show the results during reverse bias and it's clear there is a higher leakage current present in the Ge diode at a maximum of over 80μA whereas the Si diodes leakage current does not exceed 10nA.

When the static characteristics are calculated off a fixed voltage 9V, the Ge diode has the lower resistance as there is a higher current when compared to the Si diode

Dynamic Characteristics Reverse Direction

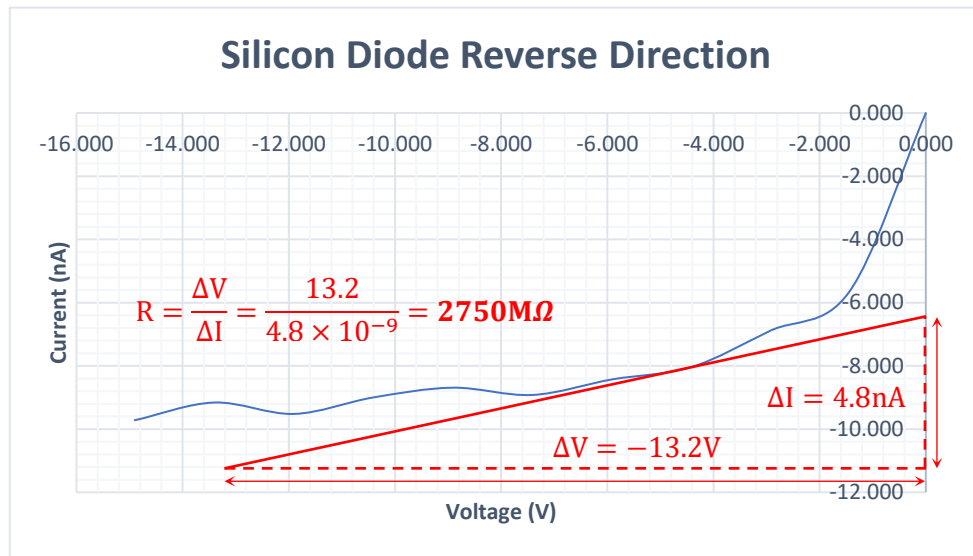


Figure 13 – Silicon Diode Reverse Bias Curve (Dynamic)

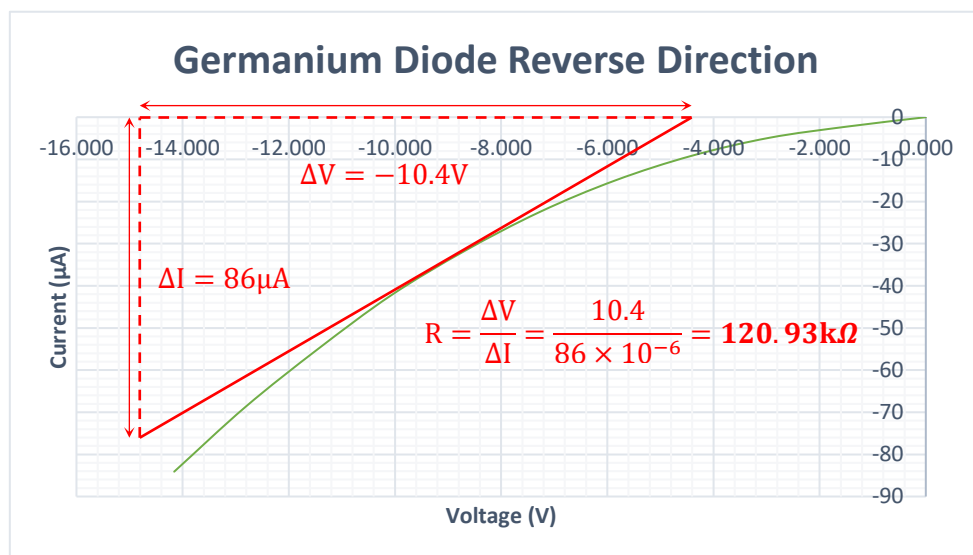


Figure 14 – Germanium Diode Reverse Bias Curve (Dynamic)

When comparing figure 13 & 14 overall there is a lower resistance with the Ge diode than the Si diode. This is from the Ge diode allowing more leakage current to pass than the Si diode, this is clear from the delta current for Ge being 86μA and Si being 4.8nA.

Task 2 – Voltage Regulator Design

a)

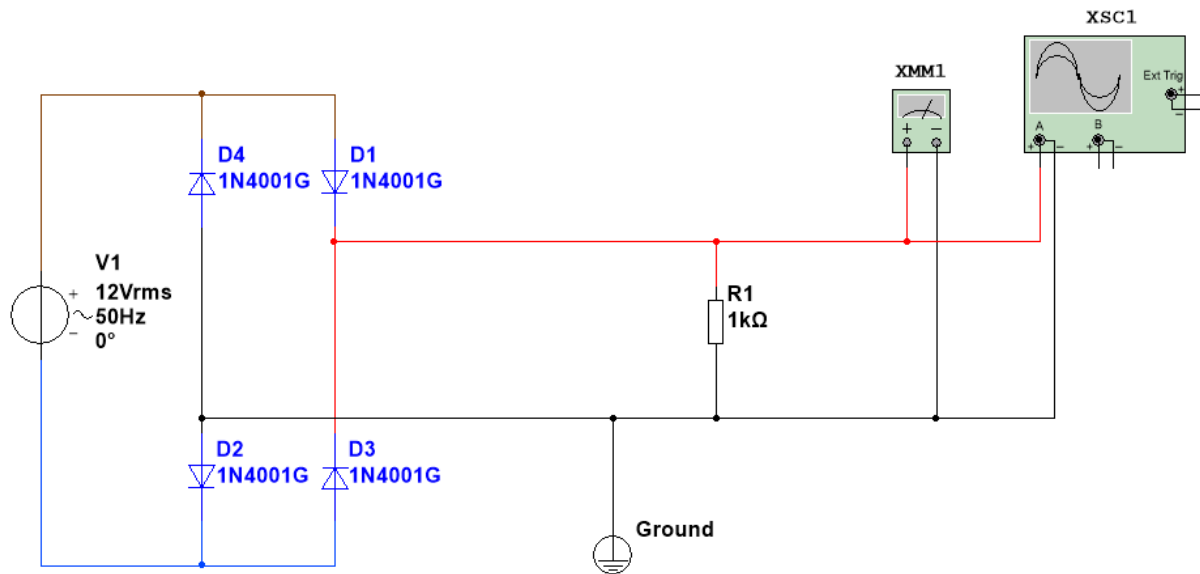


Figure 15 - Full-Wave Bridge Rectifier Multisim Circuit

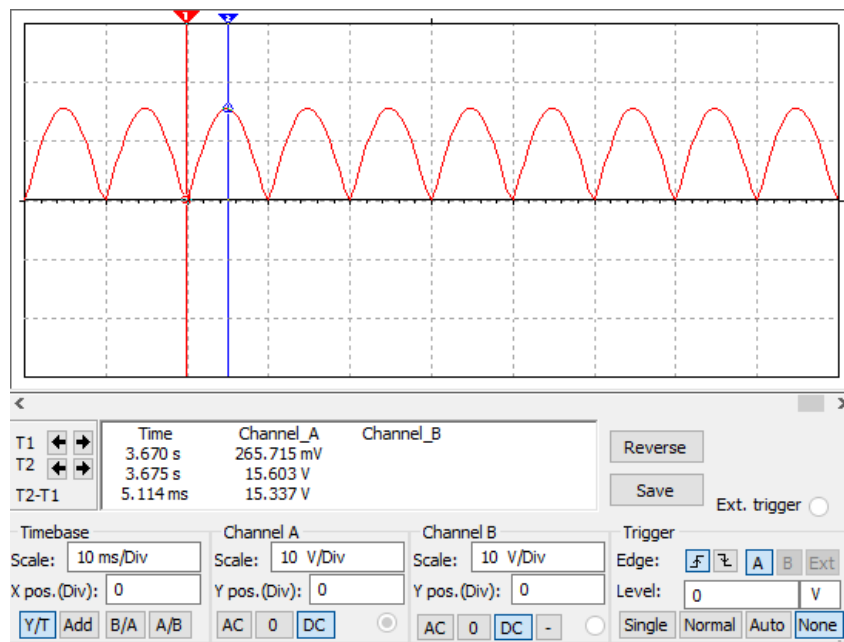


Figure 16 - Full-Wave Bridge Rectifier Waveform

Figure 15 is the Multisim simulation for a full wave bridge rectifier, by having four diodes in this configuration you can produce a DC output as seen in figure 16. This is achieved by the positive half of the AC waveform passing through D_1 and the negative half of the waveform passing through D_3 . This then introduces both halves of the waveform on to the positive rail removing the negative cycle. As D_2 & D_4 would be in the reverse bias little to no current would be passing so the output negative rail would be neutral.

In figure 16 there is a pulsing DC output as the tradition AC sinewave has been flipped to give a totally positive DC output.

b)

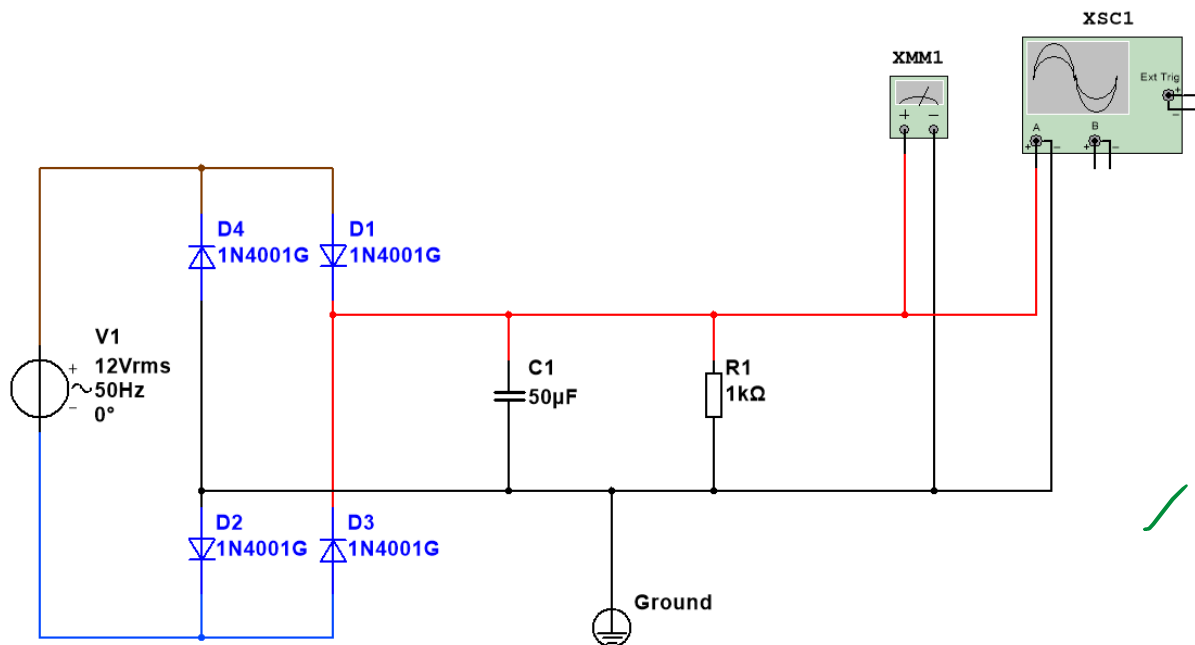


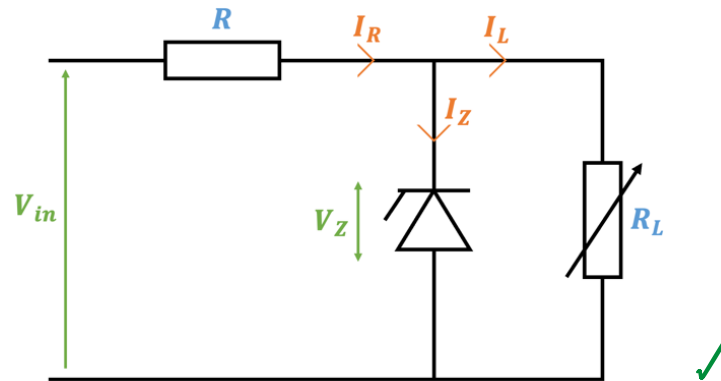
Figure 17 - Full-Wave Bridge Rectifier with Smoothing Capacitor Multisim Circuit



Figure 18 - Full-Wave Bridge Rectifier with Smoothing Capacitor Waveform

In figure 17 an addition of a capacitor is made to the circuit. From figure 18 the effect of the added capacitor is clear, the pulse effect has now smoothing effect. On the first 90° of the input cycle the capacitor is charged, once the input cycle starts to decrease from 90° to 180° the capacitor discharges, making the drop in voltage less severe. If a stronger smoothing effect is desired increasing the capacitor value would achieve this furthermore if the capacitor value was decreased, the ripple would be greater with less smoothing.

c)
Design



$$I_{Z(\min)} = 5\text{mA}$$

$$P = 300\text{mw}$$

$$I_{Z(\max)} = \frac{P}{V_Z} = \frac{300 \times 10^{-3}}{5.1} = \mathbf{58.82\text{mA}}$$

$$V_{\text{in}} = 14.5\text{V} \quad V_Z = 5.1\text{V}$$

$$I_R = I_Z + I_L$$

$$V_R = V_{\text{in}} - V_Z = 14.5 - 5.1 = \mathbf{9.4\text{V}}$$

$$R = \frac{V_R}{I_R}$$

$$\text{Let } R_L = 1\text{k}\Omega \quad V_Z = V_L = 5.1\text{V}$$

$$I_L = \frac{V_Z}{R_L} = \frac{5.1}{1000} = \mathbf{5.1\text{mA}}$$

$$I_{R(\min)} = I_{Z(\min)} + I_L = 5 + 5.1 = \mathbf{10.1\text{mA}}$$

$$I_{R(\max)} = I_{Z(\max)} + I_L = 58.82 + 5.1 = \mathbf{63.92\text{mA}}$$

$$R_{\min} = \frac{V_R}{I_{R(\max)}} = \frac{9.4}{63.92 \times 10^{-3}} = \mathbf{147.06\Omega}$$

$$R_{\max} = \frac{V_R}{I_{R(\min)}} = \frac{9.4}{10.1 \times 10^{-3}} = \mathbf{930.7\Omega}$$

Potential Resistor Values = 330Ω, 390Ω, 470Ω, 560Ω, 680Ω

Chosen Resistor Value = **560Ω**

Test

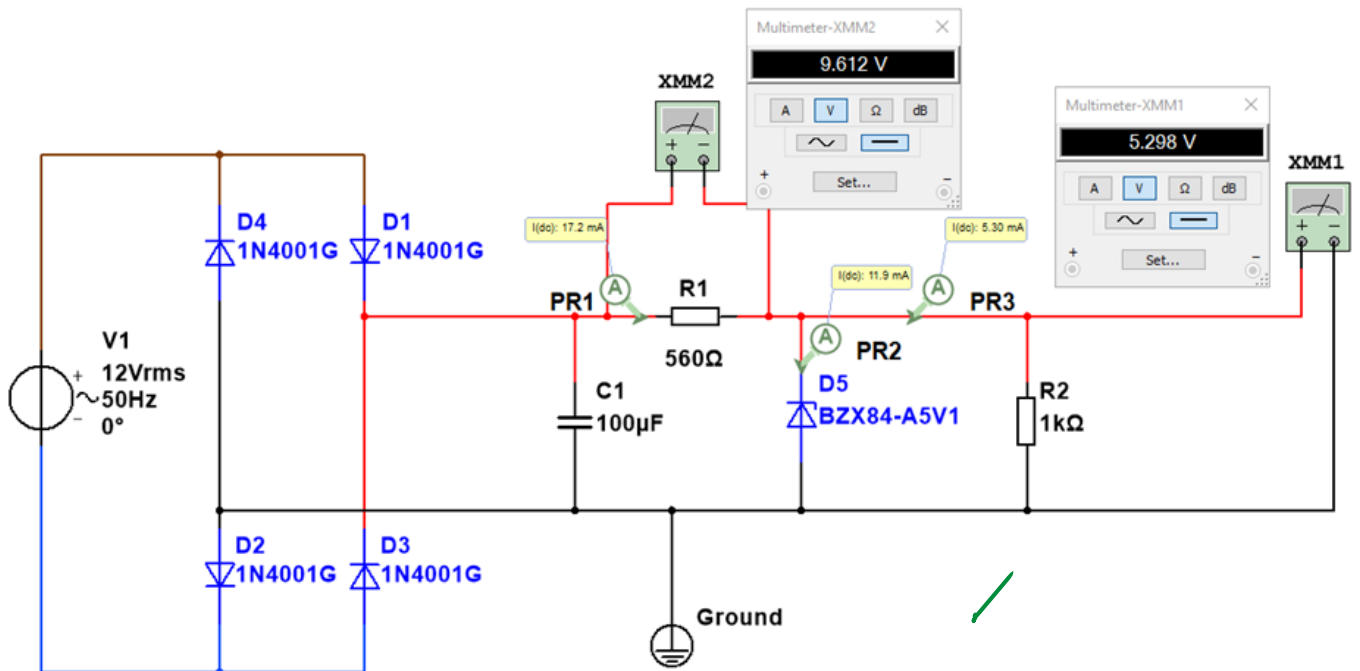


Figure 19 - Full-Wave Bridge Rectifier with Voltage Regulator Multisim Circuit

Expanding on the full-wave bridge rectifier a voltage regulator circuit has been added in figure 19. The function of this circuit is to ensure that regardless of fluctuations in the input voltage and load resistance the output voltage remains constant. This is proved in figure 19 where XMM2 is reading a line voltage of 9.612V prior to the voltage regulator and XMM1 reading 5.298V post voltage regulator. There are drawbacks to this circuit according to Bryan Witherspoon who did a related paper he stated,

“As with most voltage regulators, the source voltage must be slightly higher than the Zener voltage in order to keep the Zener diode in reverse breakdown. Otherwise, the output voltage will simply follow the input voltage.” (Witherspoon, B., 2008)

According to Bryan Witherspoon if the voltage regulator input voltage falls short of 5.1V, it would fail its function of regulating the voltage.

Well done.

Task 3 - Transistor Amplifier Design and Performance Measurement

a)

DC Supply Voltage

$$V_{CC} = 12V \quad /$$

Transistor

BC547 Transistor

Quiescent collector current

$$I_q = 4mA \quad /$$

Collector resistor

$$R_C = \frac{V_{CC}}{2 \times I_C} = \frac{12}{2 \times 4 \times 10^{-3}} = 1.5k\Omega \quad /$$

Emitter resistor

$$I_E = I_C$$

$$15\% \text{ of } V_{CC} = 15\% \text{ of } 12 = 1.8V \quad /$$

$$R_E = \frac{V_E}{I_E} = \frac{1.8}{4 \times 10^{-3}} = 450\Omega \approx 470\Omega \quad /$$

Estimated a value for base current

$$\text{Measured } h_{fe} = 337 \quad /$$

$$h_{fe} = \frac{I_C}{I_B} \quad /$$

So

$$I_B = \frac{I_C}{h_{fe}} = \frac{4 \times 10^{-3}}{337} = 11.87\mu A \quad /$$

Determining Base Voltage

$$V_{BE} \text{ from datasheet} = 0.7V \quad /$$

$$V_B = V_E + V_{BE} = 1.8 + 0.7 = 2.5V \quad /$$

Resistance for R_2

$$R_2 = \frac{V_B}{10 \times I_B} = \frac{2.5}{10 \times 11.87 \times 10^{-6}} = 21.06k\Omega \approx 22k\Omega \quad /$$

Resistance for R_1

$$R_1 = \frac{V_{CC} - V_B}{11 \times I_B} = \frac{12 - 2.5}{11 \times 11.87 \times 10^{-6}} = 72.76k\Omega \approx 68k\Omega \quad /$$

well done.

**Values obtained from data sheet found in appendix A*

b)

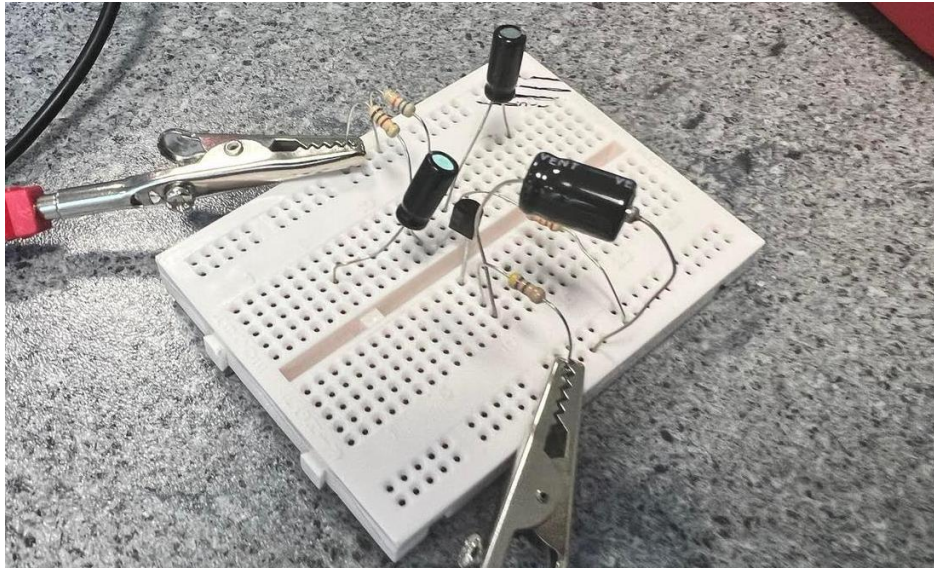


Figure 20 – Practical Common Emitter Amplifier Circuit

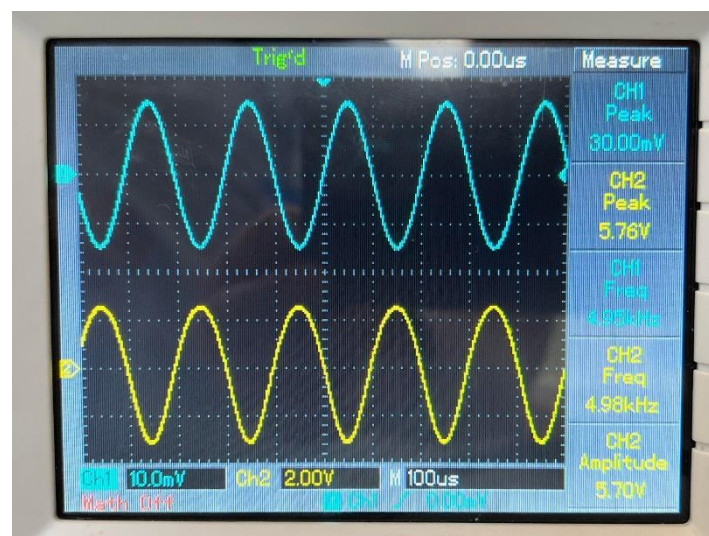


Figure 21 – Practical Circuit Oscilloscope Display

Practical Test Results			
DC Conditions		AC Conditions	
V _c	5.53V	V _{in}	30mV
V _b	2.63V	V _{out}	5.76V
V _e	1.97V	Gain	192
V _{be}	0.65V		
I _c	4.27mA		

Figure 22 – Practical Test Results Table

c)

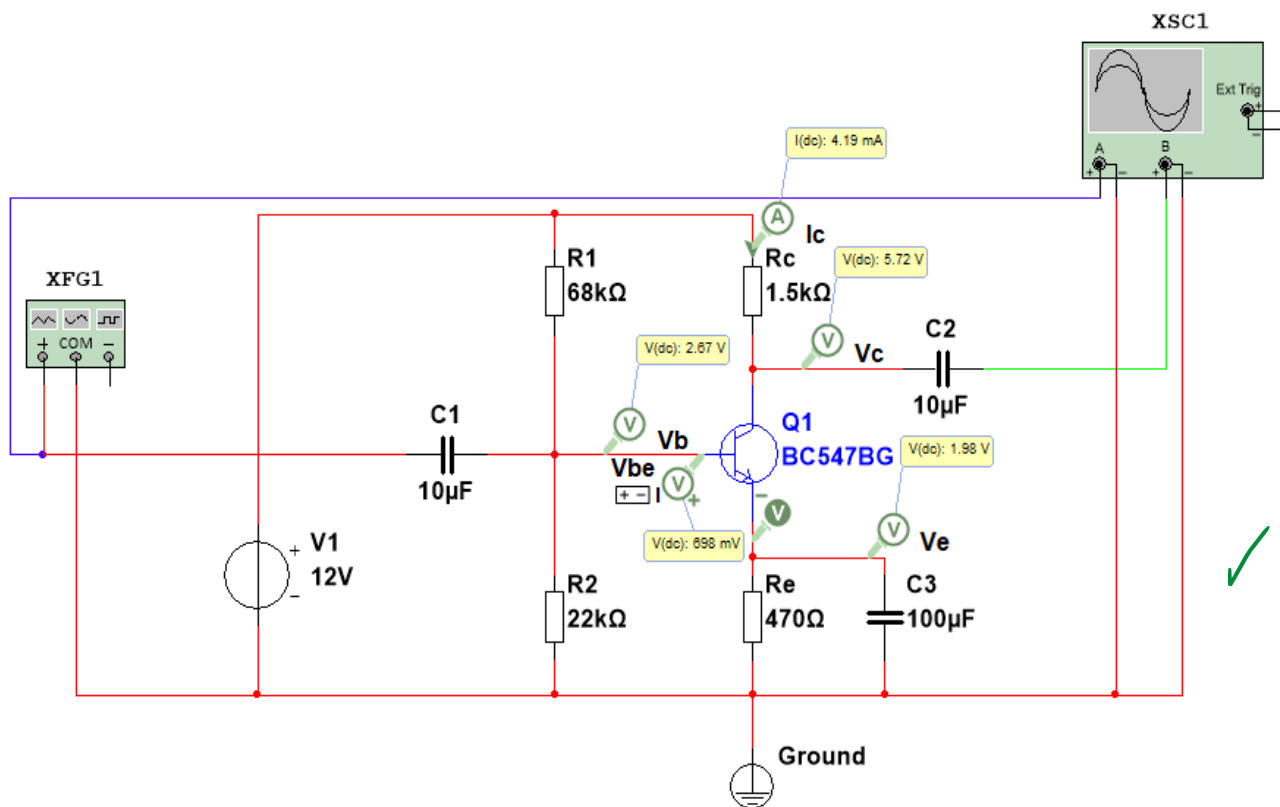


Figure 23 – Simulated Common Emitter Amplifier Circuit

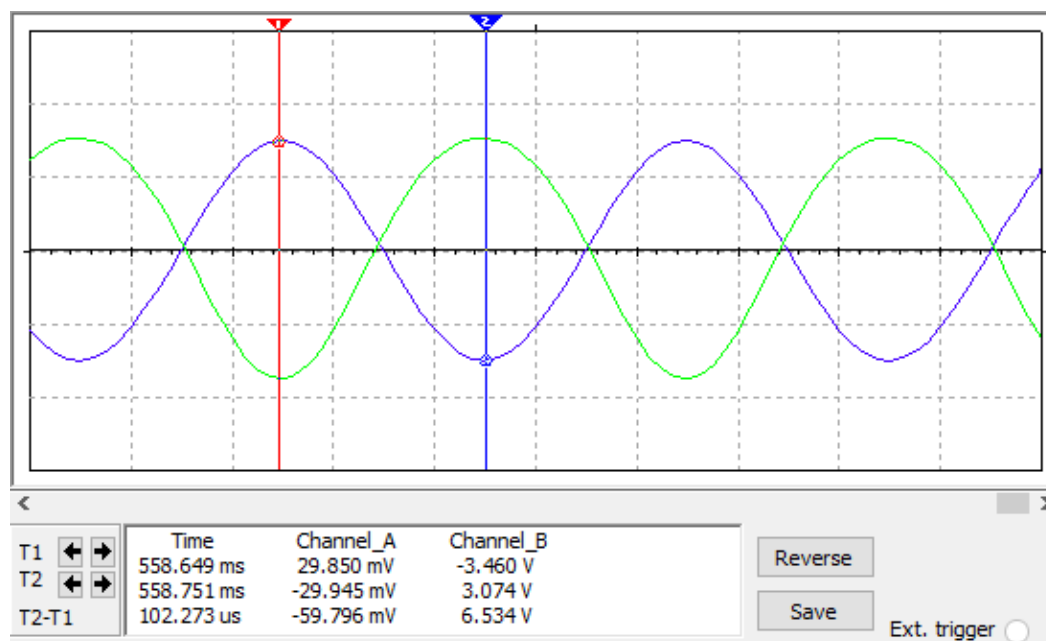


Figure 24 – Simulated Circuit Oscilloscope Display

Practical vs Simulation Test Results							
DC Conditions				AC Conditions			
Value	Practical	Simulation	Difference	Value	Practical	Simulation	Difference
V _c (V)	5.530	5.720	-0.190	V _{in} (mV)	30.000	59.796	-29.796
V _b (V)	2.630	2.670	-0.040	V _{out} (V)	5.760	6.534	-0.774
V _e (V)	1.970	1.980	-0.010	Gain	192.000	109.272	82.728
V _{be} (V)	0.650	0.698	-0.048				
I _c (mA)	4.270	4.190	0.080				

Figure 25 – Practical versus Simulation Test Results Table

Good.

A practical experiment was conducted as seen in figure 20 – 22, this is where a common emitter amplifier was built based calculations in task 3a (pg 15). The same circuit was then simulated in Multisim as seen in figure 23 & 24 and complied all results from both the practical and simulation into the table in figure 25.

Under DC conditions the results where very similar with the biggest difference only being 0.19V in the collector voltage.

An oscilloscope was used to gather results for AC conditions (*for both tests these can be seen in figure 21 for practical and figure 24 for simulated*).

There is a greater difference under AC conditions with the gain having a difference of 82.7, there are many causes for this such as the difference in input voltage being almost double in the simulated. Another cause is the real-world conditions of practical versus the ideal conditions of the simulation software. When testing the hfe it was clear that temperature could greatly affect the value, where in the simulation this value would not vary throughout testing. Other variables present in the practical experiment is the tolerance of the resistors being up to $\pm 5\%$ where in Multisim that value is exact. Also, resistances for R_1 & R_2 could not be exact to calculations due to the limitation of values available when conducting the experiment. ✓

d)

Common Emitter Amp Frequency Response			
Freq (Hz)	Vout (V)	Gain	Gain (dB)
50	1.36	45.33	33.13
100	2.5	83.33	38.42
300	4.56	152.00	43.64
500	5.04	168.00	44.51
800	5.44	181.33	45.17
1000	5.68	189.33	45.54
2000	5.68	189.33	45.54
5000	5.76	192.00	45.67
10000	5.76	192.00	45.67
20000	5.68	189.33	45.54
30000	5.68	189.33	45.54
40000	5.6	186.67	45.42
50000	5.6	186.67	45.42
80000	5.6	186.67	45.42
100000	5.52	184.00	45.30
200000	5.28	176.00	44.91
300000	4.96	165.33	44.37
400000	4.56	152.00	43.64
500000	4.24	141.33	43.00
600000	3.92	130.67	42.32
700000	3.52	117.33	41.39
1000000	2.72	90.67	39.15

Figure 26 – Frequency Response Table of Practical Circuit

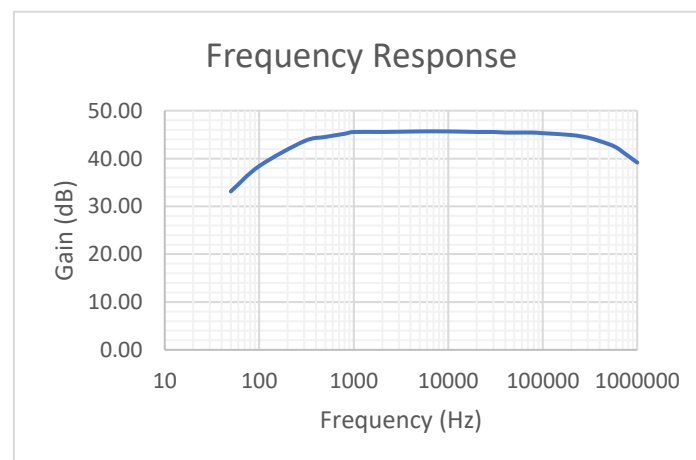


Figure 27 – Frequency Response Graph of Practical Circuit

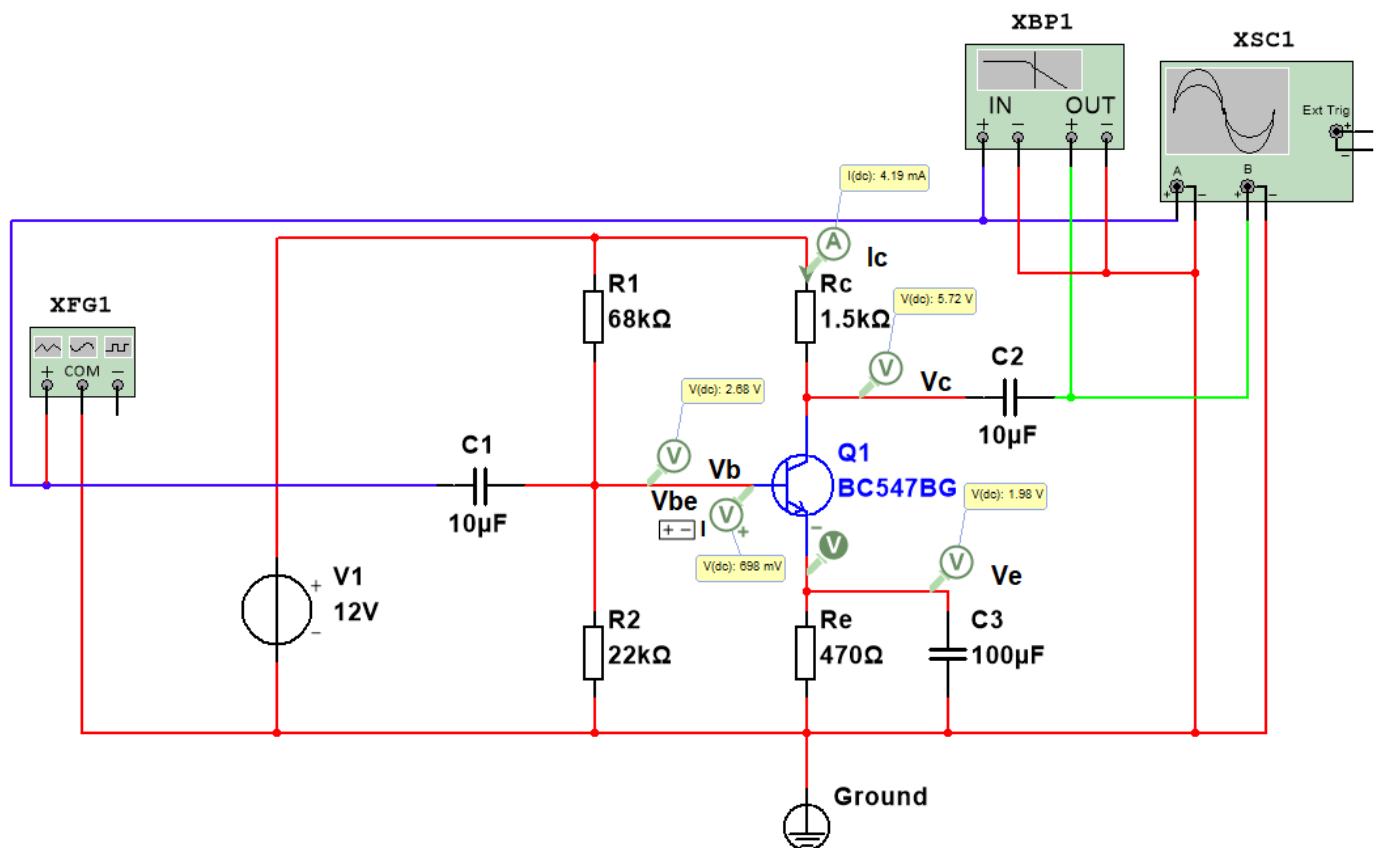


Figure 28 – Simulated Common Emitter Amplifier Circuit with Bode Plotter

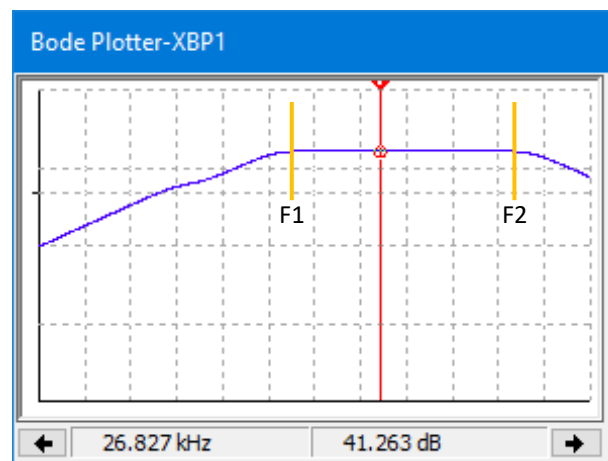


Figure 29 – Bode Plotter of Simulated Circuit

$$\text{Gain} = \frac{V_{\text{out}}}{V_{\text{in}}} = \frac{6.5}{59.8 \times 10^{-3}} = 108.7$$

$$\text{Max gain} = 41.26\text{dB}$$

$$\frac{1}{2} \text{ power point} = \text{Max gain (dB)} - 3\text{dB} = 41.26 - 3 = 38.26\text{dB}$$

$$F2 = 51.35\text{MHz}$$

$$F1 = 131.72\text{Hz}$$

$$\text{Bandwidth} = F2 - F1 = 51.35 \times 10^6 - 131.72 = 51.34986828\text{MHz}$$

$$\text{Gain (dB)} = 20 \times \log\left(\frac{V_{\text{out}}}{V_{\text{in}}}\right) = 20 \times \log\left(\frac{6.5}{59.8 \times 10^{-3}}\right) = 40.724\text{dB}$$

The frequency response of the practical circuit is in figure 26 & 27, for the simulated circuit the bode plotter graph is shown in figure 29 and annotated showing the F1 & F2 points.

The bandwidth can be calculated by F2 minus F1, between these two F points is the operating frequency range of the amplifier circuit. The cut off points (F1 & F2) show where the output falls to half its maximum value, these are known as the $\frac{1}{2}$ power point, which is calculated to a fall in gain of 3dB of the max value.

Task 4 – Inverting Operational Amplifier

a)

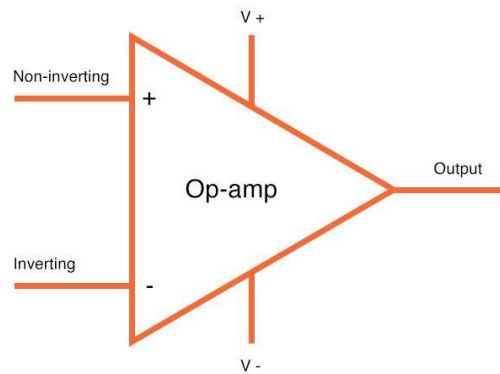


Figure 30 – Op Amp Diagram

An op-amp is an analogue integrated circuit (IC) chip built up of resistors, transistors, and capacitors. These ICs can amplify the input signal using an external power supply applied to V_+ & V_- in figure 30. Other applications of op-amps include carrying out mathematical operations such as addition, subtraction, differentiation, and integration. op-amps can amplify AC and DC signals. ✓

To use an op-amp as an inverting amplifier V_{in} must be applied to the negative terminal of the op-amp and the positive terminal is grounded. When in an inverting configuration a negative gain is achieved. In AC conditions, V_{out} the polarity would be 180° to V_{in} inverting the sine wave. ✓

Inverting op amps when used as amplifiers have negative feedback where V_{out} is connected to the negative terminal of the op amp through a resistor (*this can be seen in figure 31*). Negative feedback is where the signal fed back is 180° out of phase to that of the original input signal.

Negative feedback causes the overall gain of the amplifier to be reduced. The reason for this is it ensures the gain is constant over a wider range of input frequencies and input voltages, greater stability, linear amplification, and gain can be controlled by altering the values of R_1 (R_{in}) and R_2 (R_f) ✓

b)

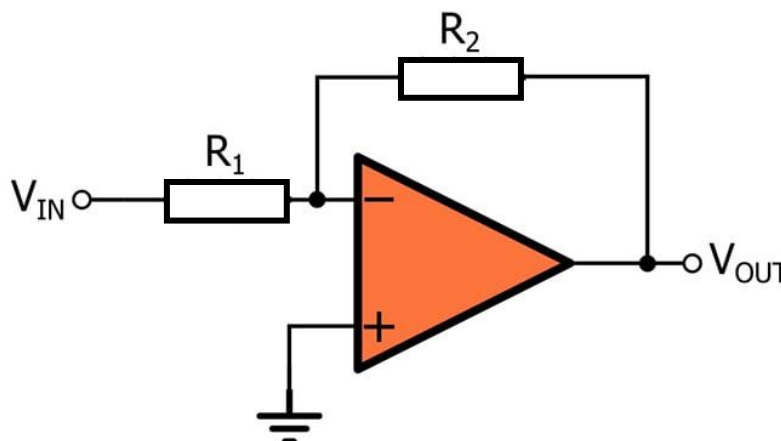


Figure 31 – Inverting Op Amp Diagram

A circuit diagram for the pre-amplifier circuit is shown in figure 31. Below are the calculations for bandwidth and values for R_1 (R_{in}) and R_2 (R_f).

$$\text{Gain} = 18$$

$$\text{Bandwidth} = 20\text{kHz (audio max frequency)}$$

Op Amp LM741, gain bandwidth product (GBP) of 1MHz *

$$\text{Bandwidth} = \frac{\text{GBP}}{\text{Gain}} = \frac{1 \times 10^6}{18} = 55.5\text{kHz}$$

$$\text{Gain} = \frac{V_{out}}{V_{in}} = -\frac{R_f}{R_{in}}$$

$$R_f = \text{Gain} \times R_{in} = 18 \times 2.2 = 39.6 \approx 39\text{k}$$

Good.

*Values obtained from data sheet found in appendix B

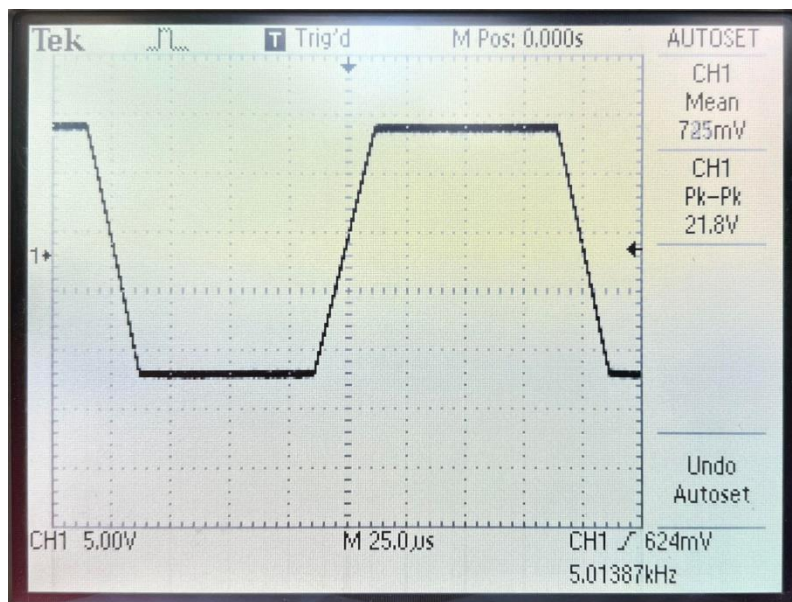


Figure 32 – Oscilloscope Clipped Waveform

This is evidence of the waveform clipping in figure 32. This is expected as the datasheet for the op amp in appendix B states a maximum voltage of $\pm 22\text{V}$ and the peak-to-peak voltage on the oscilloscope is 21.8V.

Other data obtained from appendix B pin arrangement to set up the practical circuit.

c)

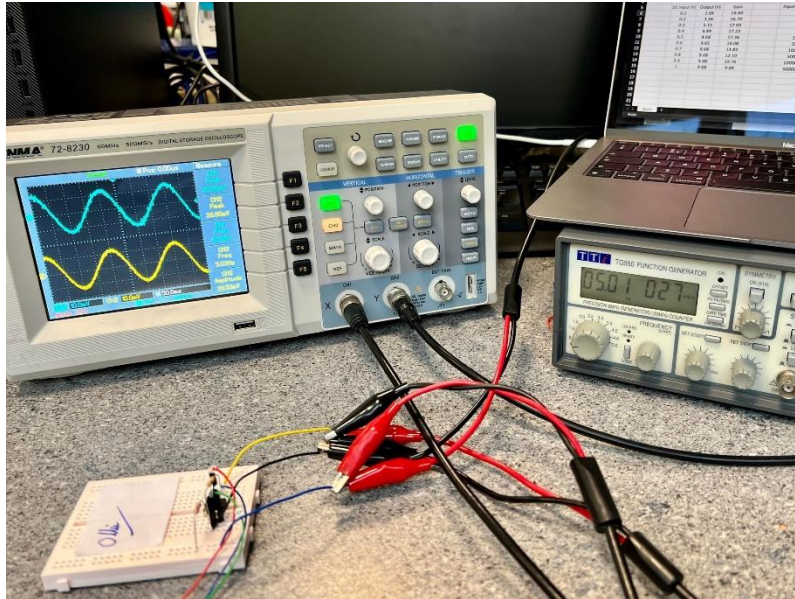


Figure 33 – Op Amp Practical Circuit

Practical Op-Amp					
DC			AC		
DC Input (V)	Output (V)	Gain	Input (mV)	Output (mV)	Gain
0.1	1.66	16.60	20	320	16.00
0.2	3.34	16.70	50	720	14.40
0.3	5.11	17.03	100	1500	15.00
0.4	6.89	17.23	500	6800	13.60
0.5	8.68	17.36	1000	14000	14.00
0.6	9.65	16.08	5000	21000	4.20
0.7	9.68	13.83	10000	22000	2.20
0.8	9.68	12.10	15000	21800	1.45
0.9	9.68	10.76	20000	21800	1.09
1	9.68	9.68			

Figure 34 – Op Amp Practical Results Table

Figure 33 & 34 is evidence of the op amp circuit and test results for the analysis of DC and AC amplification. From these results it is clear the circuit clips the output past a DC input of 0.6V and an AC input of 1V. The AC results are not linear when compared to the DC results this could be due to the experiments being conducted on different days with different equipment, human error or the tolerances and variables associated with AC.

d)
Frequency Response

Op-Amp Frequency Response			
Freq (Hz)	Vout (V)	Gain	Gain (dB)
100	6.88	13.76	22.77
200	6.88	13.76	22.77
500	6.88	13.76	22.77
1000	6.92	13.84	22.82
2000	6.92	13.84	22.82
5000	6.84	13.68	22.72
10000	6.84	13.68	22.72
20000	6.6	13.2	22.41
30000	6.32	12.64	22.03
50000	5.4	10.8	20.67
80000	3.88	7.76	17.80
100000	3.2	6.4	16.12
120000	2.03	4.06	12.17
150000	1.9	3.8	11.60
200000	1.72	3.44	10.73
500000	0.6	1.2	1.58



Figure 35 – Op Amp Frequency Response Table

In figure 35 the gain was calculated using the equations below.

$$\text{Gain (dB)} = 20 \times \log \left(\frac{V_{\text{out}}}{V_{\text{in}}} \right)$$

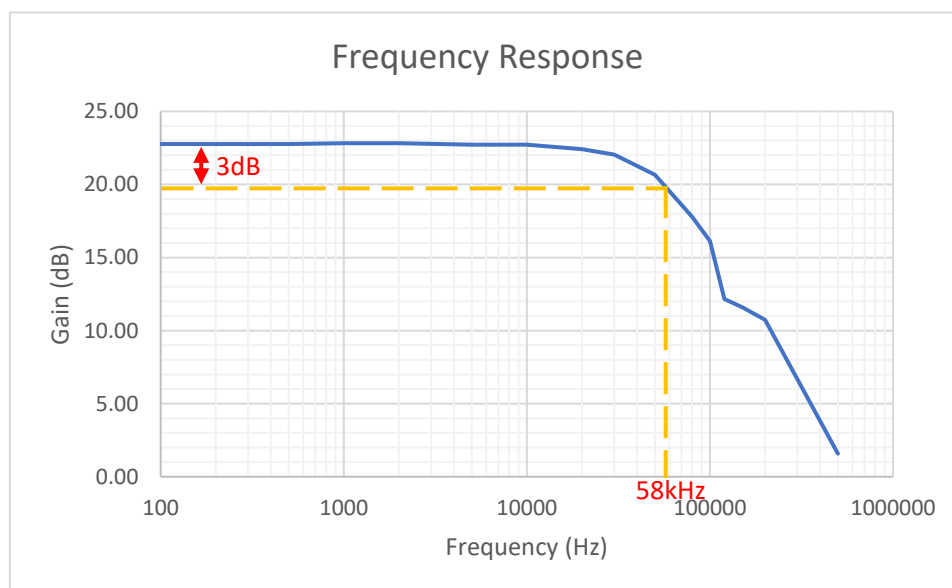


Figure 36 – Op Amp Frequency Response Graph

Figure 36 is annotated showing the $\frac{1}{2}$ power point of which is -3dB of the max gain. This $\frac{1}{2}$ power point can then be used to find the frequency cut off, this indicates if the pre-amplifier circuit has reached the brief of exceeding 20kHz (maximum frequency of the human ear). This circuit has indeed reached and bypassed the brief having a bandwidth up to 58kHz. ✓

The expectation for the curve in figure 36 to be linear but there is one inconsistent result, as there is one anomaly this could be from several reasons such as error in reading results, input error from notebook to excel document or fault in the instrument or equipment. ✓

Slew Rate

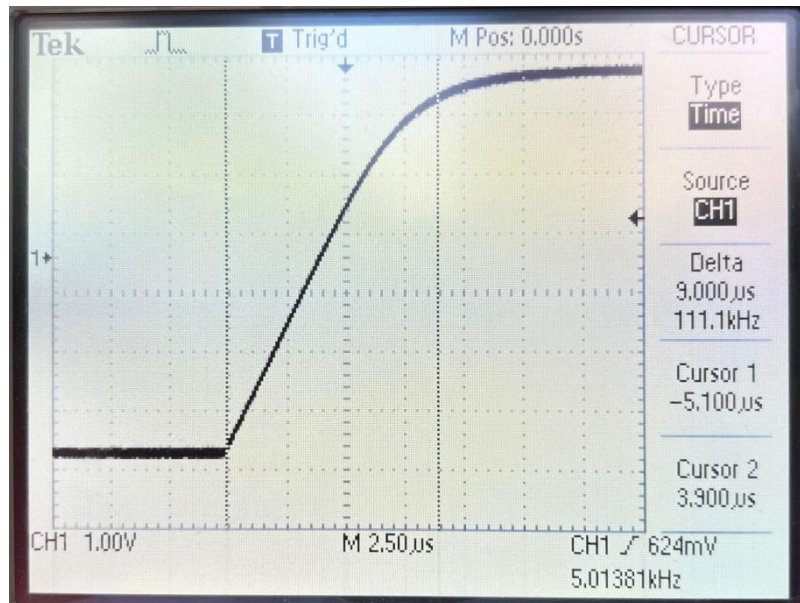


Figure 37 – Op Amp Slew Rate Wave

A square wave was inputted to the circuit from a function generator, from this square wave the slew rate can be obtained. The slew rate is the maximum rate of change of the output voltage and is expressed in voltage per microsecond ($V/\mu s$). In the datasheet seen in Appendix B this op amp has a slew rate of $0.5V/\mu s$ which is slow reacting when compared to other op amps on the market which boasts a slew rate of $20/\mu s$. ✓

Conclusion

Throughout this assignment there has been a clear divide in results from real world practical experiments conducted in the classroom compared to simulation software.

In the real world there are no exacts there are many variables such as inaccurate equipment, incorrect components, and environmental factors such as temperature.

All of these factors are not present in simulation software as it has all ideal values creating the perfect circumstances for an experiment.

Simulation software is a great tool in the society of the future but is still unable to replicate the real-world practical elements of experiments. ✓

Figure Index

Figure 1 – Diode Working Principle Diagram - www.fluke.com. (n.d.). What is a Diode? [online] Available at: <https://www.fluke.com/en-us/learn/blog/electrical/what-is-a-diode>.

Figure 2 – P-N Junction Working Principle Diagram - ElectronicsTutorials (2018). PN Junction Theory for Semiconductor Diodes. [online] Basic Electronics Tutorials. Available at: https://www.electronicstutorials.ws/diode/diode_2.html.

Figure 3 – Forward Bias Circuit Diagram – Circuit Diagram Provided in the assignment brief

Figure 4 – Reverse Bias Circuit Diagram – Circuit Diagram Provided in the assignment brief

Figure 5 – Silicon Diode Test Results – Results table created in Excel by author Ollie Evans

Figure 6 – Germanium Diode Test Results – Results table created in Excel by author Ollie Evans

Figure 7 – Silicon Diode Forward Bias Curve (Static) – Graph created in Excel and annotated by author Ollie Evans

Figure 8 – Germanium Diode Forward Bias Curve (Static) – Graph created in Excel and annotated by author Ollie Evans

Figure 9 – Silicon Diode Forward Bias Curve (Dynamic) – Graph created in Excel and annotated by author Ollie Evans

Figure 10 – Germanium Diode Forward Bias Curve (Dynamic) – Graph created in Excel and annotated by author Ollie Evans

Figure 11– Silicone Diode Reverse Bias Curve (Static) – Graph created in Excel and annotated by author Ollie Evans

Figure 12 – Germanium Diode Reverse Bias Curve (Static) – Graph created in Excel and annotated by author Ollie Evans

Figure 13 – Silicone Diode Reverse Bias Curve (Dynamic) – Graph created in Excel and annotated by author Ollie Evans

Figure 14 – Germanium Diode Reverse Bias Curve (Dynamic) – Graph created in Excel and annotated by author Ollie Evans

Figure 15 - Full-Wave Bridge Rectifier Multisim Circuit – Simulated using Multisim by author Ollie Evans

Figure 16 - Full-Wave Bridge Rectifier Waveform – Simulated using Multisim by author Ollie Evans

Figure 17 - Full-Wave Bridge Rectifier with Smoothing Capacitor Multisim Circuit – Simulated using Multisim by author Ollie Evans

Figure 18 - Full-Wave Bridge Rectifier with Smoothing Capacitor Waveform – Simulated using Multisim by author Ollie Evans

Figure 19 - Full-Wave Bridge Rectifier with Voltage Regulator Multisim Circuit – Simulated using Multisim by author Ollie Evans

Figure 20 – Practical Common Emitter Amplifier Circuit – Practical Circuit built by author Ollie Evans

Figure 21 – Practical Circuit Oscilloscope Display – Picture taken by author Ollie Evans

Figure 22 – Practical Test Results Table – Results table created in Excel by author Ollie Evans

Figure 23 – Simulated Common Emitter Amplifier Circuit – Simulated using Multisim by author Ollie Evans

Figure 24 – Simulated Circuit Oscilloscope Display – Simulated using Multisim by author Ollie Evans

Figure 25 – Practical versus Simulation Test Results Table – Results table created in Excel by author Ollie Evans

Figure 26 – Frequency Response Table of Practical Circuit - Table created in Excel by author Ollie Evans

Figure 27 – Frequency Response Graph of Practical Circuit – Graph created in Excel by author Ollie Evans

Figure 28 – Simulated Common Emitter Amplifier Circuit with Bode Plotter – Simulated using Multisim by author Ollie Evans

Figure 29 – Bode Plotter of Simulated Circuit – Simulated using Multisim by author Ollie Evans

Figure 30 – Op Amp Diagram – Allaboutcircuits.com. (2015). Introduction to Operational Amplifiers (Op-amps) | Operational Amplifiers | Electronics Textbook. [online] Available at: <https://www.allaboutcircuits.com/textbook/semiconductors/chpt-8/introduction-operational-amplifiers/>

Figure 31 – Non-Inverting Op Amp Diagram – Allaboutcircuits.com. (2015). Basic Amplifier Configurations: the Inverting Amplifier - Video Tutorial. [online] Available at: <https://www.allaboutcircuits.com/video-tutorials/the-basic-op-amp-inverting-amplifier/>.

Figure 32 – Oscilloscope Clipped Waveform – Picture taken by author Ollie Evans

Figure 33 – Op Amp Practical Circuit – Picture taken by author Ollie Evans

Figure 34 – Op Amp Practical Results Table – Table created in Excel by author Ollie Evans

Figure 35 – Op Amp Frequency Response Table – Graph created in Excel by author Ollie Evans

Figure 36 – Op Amp Frequency Response Graph – Graph created in Excel by author Ollie Evans

Figure 37 – Op Amp Slew Rate Wave – Picture taken by author Ollie Evans



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National Semiconductor Corporation, 2004, LM741 Operational Amplifier

Acknowledgement

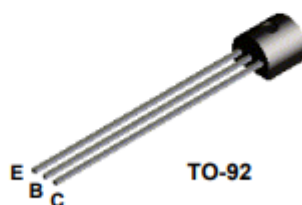
Thanks to Puma Terminals for the practical experience.

Appendix A



**Discrete POWER & Signal
Technologies**

**BC547
BC547A
BC547B
BC547C**



TO-92

NPN General Purpose Amplifier

This device is designed for use as general purpose amplifiers and switches requiring collector currents to 300 mA. Sourced from Process 10. See PN100A for characteristics.

Absolute Maximum Ratings*

TA = 25°C unless otherwise noted

Symbol	Parameter	Value	Units
V _{CEO}	Collector-Emitter Voltage	45	V
V _{CES}	Collector-Base Voltage	50	V
V _{EB0}	Emitter-Base Voltage	6.0	V
I _C	Collector Current - Continuous	500	mA
T _J , T _{stg}	Operating and Storage Junction Temperature Range	-55 to +150	°C

*These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.

NOTES:

- 1) These ratings are based on a maximum junction temperature of 150 degrees C.
- 2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.

Thermal Characteristics

TA = 25°C unless otherwise noted

Symbol	Characteristic	Max	Units
		BC547 / A / B / C	
P _D	Total Device Dissipation Derate above 25°C	625 5.0	mW mW/°C
R _{θJC}	Thermal Resistance, Junction to Case	83.3	°C/W
R _{θJA}	Thermal Resistance, Junction to Ambient	200	°C/W

BC547 / BC547A / BC547B / BC547C

NPN General Purpose Amplifier (continued)					
Electrical Characteristics TA = 25°C unless otherwise noted					
Symbol	Parameter	Test Conditions	Min	Max	Units
OFF CHARACTERISTICS					
$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage	$I_C = 1.0 \text{ mA}, I_B = 0$	45		V
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage	$I_C = 10 \text{ } \mu\text{A}, I_E = 0$	50		V
$V_{(BR)CES}$	Collector-Base Breakdown Voltage	$I_C = 10 \text{ } \mu\text{A}, I_E = 0$	50		V
$V_{(BR)EBO}$	Emitter-Base Breakdown Voltage	$I_E = 10 \text{ } \mu\text{A}, I_C = 0$	6.0		V
I_{CBO}	Collector Cutoff Current	$V_{CB} = 30 \text{ V}, I_E = 0$ $V_{CB} = 30 \text{ V}, I_E = 0, T_A = +150 \text{ } ^\circ\text{C}$		15 5.0	nA μA
ON CHARACTERISTICS					
h_{FE}	DC Current Gain	$V_{CE} = 5.0 \text{ V}, I_C = 2.0 \text{ mA}$ 547 547A 547B 547C	110 110 200 420	800 220 450 800	
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	$I_C = 10 \text{ mA}, I_B = 0.5 \text{ mA}$ $I_C = 100 \text{ mA}, I_B = 5.0 \text{ mA}$		0.25 0.60	V V
$V_{BE(on)}$	Base-Emitter On Voltage	$V_{CE} = 5.0 \text{ V}, I_C = 2.0 \text{ mA}$ $V_{CE} = 5.0 \text{ V}, I_C = 10 \text{ mA}$	0.58	0.70 0.77	V V
SMALL SIGNAL CHARACTERISTICS					
h_{fe}	Small-Signal Current Gain	$I_C = 2.0 \text{ mA}, V_{CE} = 5.0 \text{ V},$ $f = 1.0 \text{ kHz}$	125	900	
NF	Noise Figure	$V_{CE} = 5.0 \text{ V}, I_C = 200 \text{ } \mu\text{A},$ $R_S = 2.0 \text{ k}\Omega, f = 1.0 \text{ kHz},$ $B_W = 200 \text{ Hz}$		10	dB

BC547 / BC547A / BC547B / BC547C

Reference: Fairchild Semiconductor Corporation, 1997, BC547ABC, Rev B

Appendix B



August 2000

LM741

Operational Amplifier

General Description

The LM741 series are general purpose operational amplifiers which feature improved performance over industry standards like the LM709. They are direct, plug-in replacements for the 709C, LM201, MC1439 and 748 in most applications.

The amplifiers offer many features which make their application nearly foolproof: overload protection on the input and

output, no latch-up when the common mode range is exceeded, as well as freedom from oscillations.

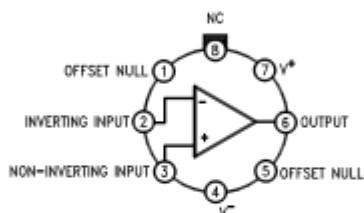
The LM741C is identical to the LM741/LM741A except that the LM741C has their performance guaranteed over a 0°C to +70°C temperature range, instead of -55°C to +125°C.

Features

LM741 Operational Amplifier

Connection Diagrams

Metal Can Package

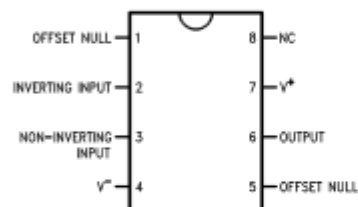


00934102

Note 1: LM741H is available per JM38510/10101

Order Number LM741H, LM741H/883 (Note 1),
LM741AH/883 or LM741CH
See NS Package Number H08C

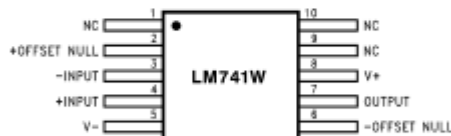
Dual-In-Line or S.O. Package



00934103

Order Number LM741J, LM741J/883, LM741CN
See NS Package Number J08A, M08A or N08E

Ceramic Flatpak

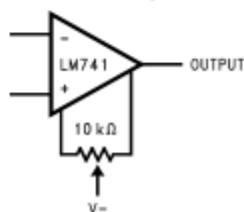


00934105

Order Number LM741W/883
See NS Package Number W10A

Typical Application

Offset Nulling Circuit



00934107

LM741

Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

(Note 7)

	LM741A	LM741	LM741C
Supply Voltage	±22V	±22V	±18V
Power Dissipation (Note 3)	500 mW	500 mW	500 mW
Differential Input Voltage	±30V	±30V	±30V
Input Voltage (Note 4)	±15V	±15V	±15V
Output Short Circuit Duration	Continuous	Continuous	Continuous
Operating Temperature Range	–55°C to +125°C	–55°C to +125°C	0°C to +70°C
Storage Temperature Range	–65°C to +150°C	–65°C to +150°C	–65°C to +150°C
Junction Temperature	150°C	150°C	100°C
Soldering Information			
N-Package (10 seconds)	260°C	260°C	260°C
J- or H-Package (10 seconds)	300°C	300°C	300°C
M-Package			
Vapor Phase (60 seconds)	215°C	215°C	215°C
Infrared (15 seconds)	215°C	215°C	215°C
See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.			
ESD Tolerance (Note 8)	400V	400V	400V

Electrical Characteristics (Note 5)

Parameter	Conditions	LM741A			LM741			LM741C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$T_A = 25^\circ\text{C}$ $R_S \leq 10\text{ k}\Omega$ $R_S \leq 50\Omega$		0.8	3.0		1.0	5.0		2.0	6.0	mV mV
	$T_{AMIN} \leq T_A \leq T_{AMAX}$ $R_S \leq 50\Omega$ $R_S \leq 10\text{ k}\Omega$			4.0			6.0			7.5	mV mV
				15							$\mu\text{V}/^\circ\text{C}$
Average Input Offset Voltage Drift				15							$\mu\text{V}/^\circ\text{C}$
Input Offset Voltage Adjustment Range	$T_A = 25^\circ\text{C}$, $V_S = \pm 20\text{V}$	±10				±15			±15		mV
Input Offset Current	$T_A = 25^\circ\text{C}$		3.0	30		20	200		20	200	nA
	$T_{AMIN} \leq T_A \leq T_{AMAX}$			70		85	500			300	nA
Average Input Offset Current Drift				0.5							nA/ $^\circ\text{C}$
Input Bias Current	$T_A = 25^\circ\text{C}$		30	80		80	500		80	500	nA
	$T_{AMIN} \leq T_A \leq T_{AMAX}$			0.210			1.5			0.8	μA
Input Resistance	$T_A = 25^\circ\text{C}$, $V_S = \pm 20\text{V}$	1.0	6.0		0.3	2.0		0.3	2.0		M Ω
	$T_{AMIN} \leq T_A \leq T_{AMAX}$, $V_S = \pm 20\text{V}$	0.5									M Ω
Input Voltage Range	$T_A = 25^\circ\text{C}$							±12	±13		V
	$T_{AMIN} \leq T_A \leq T_{AMAX}$				±12	±13					V

LM741

Electrical Characteristics (Note 5) (Continued)

Parameter	Conditions	LM741A			LM741			LM741C			Units	
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
Large Signal Voltage Gain	$T_A = 25^\circ\text{C}$, $R_L \geq 2\text{ k}\Omega$ $V_S = \pm 20\text{V}$, $V_O = \pm 15\text{V}$ $V_S = \pm 15\text{V}$, $V_O = \pm 10\text{V}$	50			50	200		20	200		V/mV V/mV	
	$T_{AMIN} \leq T_A \leq T_{AMAX}$, $R_L \geq 2\text{ k}\Omega$, $V_S = \pm 20\text{V}$, $V_O = \pm 15\text{V}$ $V_S = \pm 15\text{V}$, $V_O = \pm 10\text{V}$ $V_S = \pm 5\text{V}$, $V_O = \pm 2\text{V}$	32			25			15			V/mV V/mV V/mV	
		10										
Output Voltage Swing	$V_S = \pm 20\text{V}$ $R_L \geq 10\text{ k}\Omega$ $R_L \geq 2\text{ k}\Omega$	± 16 ± 15									V V	
	$V_S = \pm 15\text{V}$ $R_L \geq 10\text{ k}\Omega$ $R_L \geq 2\text{ k}\Omega$				± 12 ± 10	± 14 ± 13		± 12 ± 10	± 14 ± 13		V V	
Output Short Circuit Current	$T_A = 25^\circ\text{C}$	10	25	35		25			25		mA	
	$T_{AMIN} \leq T_A \leq T_{AMAX}$	10		40							mA	
Common-Mode Rejection Ratio	$T_{AMIN} \leq T_A \leq T_{AMAX}$ $R_S \leq 10\text{ k}\Omega$, $V_{CM} = \pm 12\text{V}$ $R_S \leq 50\Omega$, $V_{CM} = \pm 12\text{V}$	80	95		70	90		70	90		dB dB	
Supply Voltage Rejection Ratio	$T_{AMIN} \leq T_A \leq T_{AMAX}$, $V_S = \pm 20\text{V}$ to $V_S = \pm 5\text{V}$ $R_S \leq 50\Omega$ $R_S \leq 10\text{ k}\Omega$	86	96		77	96		77	96		dB dB	
Transient Response	$T_A = 25^\circ\text{C}$, Unity Gain		0.25	0.8		0.3			0.3		μs	
			6.0	20		5			5		%	
Bandwidth (Note 6)	$T_A = 25^\circ\text{C}$	0.437	1.5								MHz	
Slew Rate	$T_A = 25^\circ\text{C}$, Unity Gain	0.3	0.7			0.5			0.5		V/ μs	
Supply Current	$T_A = 25^\circ\text{C}$					1.7	2.8		1.7	2.8	mA	
Power Consumption	$T_A = 25^\circ\text{C}$ $V_S = \pm 20\text{V}$ $V_S = \pm 15\text{V}$		80	150							mW mW	
	$V_S = \pm 20\text{V}$					50	85		50	85	mW	
	$T_A = T_{AMIN}$ $T_A = T_{AMAX}$			165 135							mW mW	
	$V_S = \pm 15\text{V}$ $T_A = T_{AMIN}$ $T_A = T_{AMAX}$					60 45	100 75				mW mW	

Note 2: "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits.

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