

Module: Microcontrollers and Peripherals

Online Exam

ACDA4004

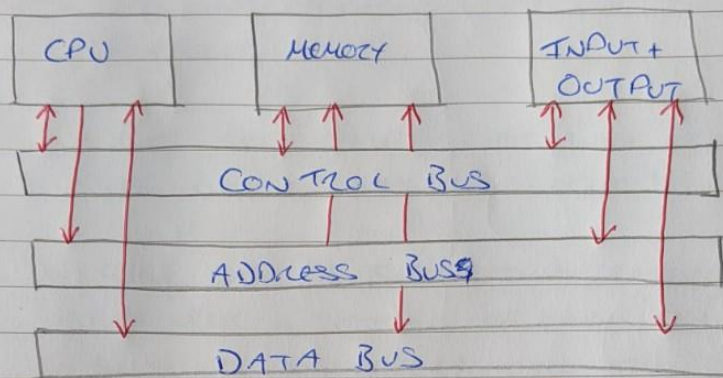
Start time 15:00

Duration: 3 Hours

Tuesday May 19th 2020

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1803514

Q1)
a)

CONTROL, ADDRESS + DATA BUS ARE PART OF THE SYSTEM BUS.

CONTROL BUS WILL CARRY CONTROL/COMMAND SIGNALS FROM THE CPU TO OTHER COMPONENTS AND DEVICES.

ADDRESS BUS ~~that~~ CARRIES ADDRESSES OF DATA BUT NOT THE ACTUAL DATA FROM PROCESSOR TO MEMORY + INPUT/OUTPUT.

DATA BUS CARRIES THE ACTUAL DATA AFTER THE ADDRESS OF THE DATA HAS BEEN SENT

Bus widths vary from 8-64 bits. THE GREATER THE WIDTH OF THE ALLOWS MORE DATA TO BE PROCESSED/TRANSFERRED AT 1 CLOCK CYCLE.

b)

DECF - WILL DECREMENT THE VALUE STORED IN FILE ADDRESS F

NOP. HAS NO OPERATION, USED FOR TIMING PURPOSES

BTFSS - BIT TEST, SKIP IF SET. WILL NEXT LINE IF BIT IS SET TO LOGIC 1

CALL - WILL CALL A SUBROUTINE, RATHER THAN REENTER A SECTION OF CODE FOR A FUNCTION SUCH AS DELAY, CAN CALL THE SUBROUTINE

CURWDT - CLEAR WATCHDOG TIMER WITH RESET THE WATCHDOG TIMER.

c)

IF THE WATCHDOG TIMER IS ACTIVATED ON A PIC IT HAS THE ABILITY TO RESET THE WHOLE PROGRAMME AND ANY STORED DATA WILL BE LOST. CLEARING THE TIMER WILL RESET ITS INTERNAL COUNTER PREVENTING AN ~~ALTERATION OF~~ ~~THE~~ UNDESIRABLE PROGRAM RESET. THIS OFFERS THE USER DATA STORAGE AND

Q2

a) RAMP COMPARE ADC

- SLOW SAMPLE TIME, HAS TO COUNT FROM 0 AT EACH NEW CLOCK CYCLE. DEPENDS ON CLOCK FREQUENCY AND ANALOGUE INPUT VOLTAGE TO CONVERT. CHEAP AND SIMPLE DESIGN DOES GIVE THIS METHOD SOME ADVANTAGES.

SUCCESSIVE APPROXIMATION ADC.

- MOST COMMON ANALOGUE TO DIGITAL CONVERTER FOR APPLICATIONS BETWEEN 8-16 BITS. CONVERTS IN FAR FEWER CYCLES THAN RAMP CONVERSION

FLASH OR ADC

- MOST EFFICIENT METHOD OF CONVERSION AND IS THE FASTEST. HOWEVER LARGE AMOUNTS OF VOLTAGE COMPARATORS ARE USED AND THAT INCREASES WITH THE SIZE OF BITS. A 3BIT CONVERTOR WOULD NEED 7 COMPARATORS.

b) THE 16F887 USES A SUCCESSIVE APPROXIMATION ADC

c) USING A 10 BIT ADC OVER AN 8 BIT WITH RESULT IN A MORE ACCURATE OUTPUT. THE LARGER THE BIT SAMPLES THE MORE PRECISE THE OUTPUT.

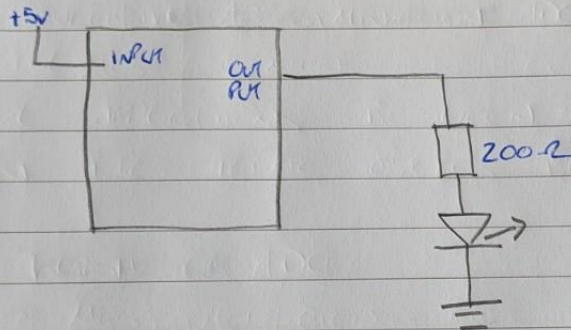
Q3

- a) 5V SUPPLY
2.2V DROP ACROSS LED
NEED 15mA

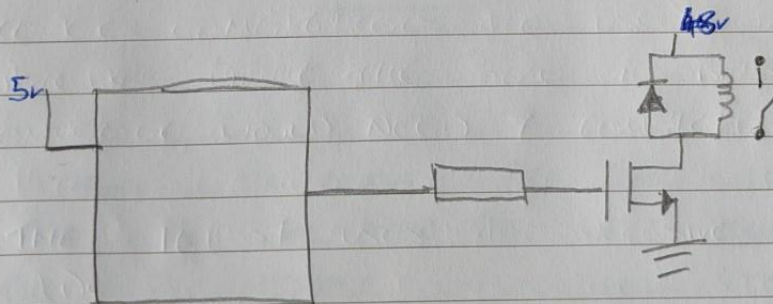
$$5 - 2.2 = 2.8 / 15\text{mA}$$

$$= 186.6\Omega$$

USE 200Ω RESISTOR AS STANDARD



b)



FET USED TO OPERATE RELAY, FLYBACK TO PROTECT

C

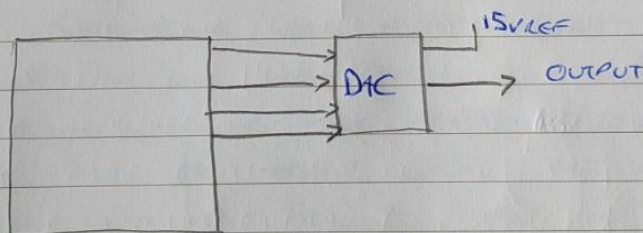
SOURCE CURRENT MEANS THAT THE DIGITAL INPUT/OUTPUT CAN SUPPLY CURRENT, WHEN CONNECTED TO A LOAD BECAUSE OF AN INTERNAL TRANSISTOR ~~CONNECTED~~ NOW BEING CONNECTED TO A GROUND LOAD.

SINKING CURRENT MEANS THE INPUT/OUTPUT CAN RECEIVE CURRENT FROM A LOAD BECAUSE OF AN INTERNALLY CONNECTED TRANSISTOR.

Q

9)

DAC CHIP



THIS IS A ROUGH 4 BIT DAC CIRCUIT. THE INPUT FOR THE DAC IS 4 OUTPUTS FROM THE PIC THESE OUTPUTS WILL EITHER BE LOGIC 1 OR LOGIC 0. WITH 4 INPUTS AND A MAXIMUM VOLTAGE OF 15V AS REFERENCE DEPENDING ON THE BINARY VALUE OF THE 4 ~~BIT~~ PIC OUTPUT PINS WILL BE THE ANALOGUE VOLTAGE BETWEEN 0-15V. THE RESOLUTION OF THIS ~~PIC~~ ~~BIT~~ DAC CHIP IS 1V

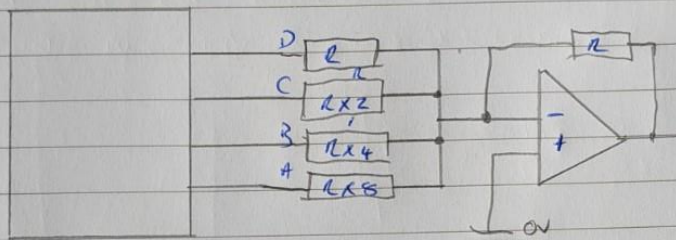
$$V_{OUT} / (2^4 - 1)$$

$$= 15/15$$

$$= 1V$$

BECAUSE OF LOW RESOLUTION THE WAVE FORM WILL BE JAGGERED, AND STEP LIKE. FOR A SMOOTHER WAVE FORM A LARGER BIT DAC CHIP WOULD BE USED.

PWM TECHNIQUE



THIS TECHNIQUE USES AN ~~INVERTING~~ INVERTING AMPLIFIER. THE INPUT FOR THE MOST SIGNIFICANT VALUE IS THE SAME RESISTANCE AS THE FEEDBACK RESISTOR. THE RESISTORS FOR THE OTHER INPUTS ARE DOUBLED IN VALUE FROM THE PREVIOUS. THE VARIATION IN ~~RESISTORS~~ RESULT IN THE ~~MESSAGE~~ SIGNAL BEING AMPLIFIED. THE ISSUE WITH THIS METHOD IS FOR A LARGER BIT SAMPLE RESISTOR VALUES WOULD BE INCREASINGLY DIFFICULT TO SOURCE. THIS CAN BE AVOIDED BY THE USE OF A RESISTOR LADDER RESULTING IN ONLY 2 DIFFERENT VALUES BEING NEEDED.

