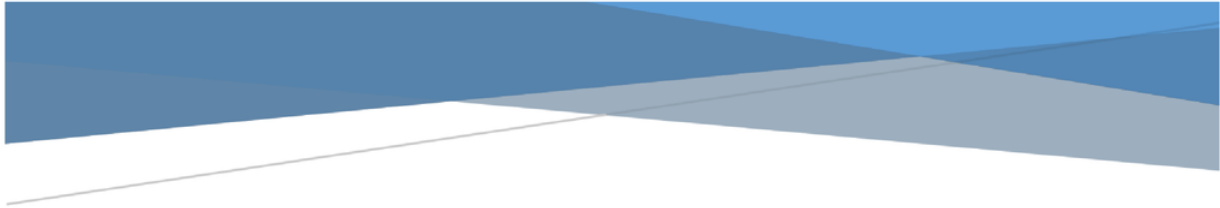


PSDE 5029 Assn 2

by Nathan Smith

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HND ELECTRICAL & ELECTRONIC ENGINEERING

PSDE 5029 VIRTUAL INSTRUMENTATION & CONTROL

ASSIGNMENT 2 NI LABVIEW MAGNITUDE COMPARATOR

Nathan Smith

Word Count = 6896

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1. Introduction

This assignment will include the use of the LabVIEW programs along with the Nexys 4 FPGA boards and NI ELVIS II boards to produce an 8 bit digital comparison between two 8 bit signals to indicate if the comparison is greater than, equal to or less than a set value into the program.

The first part of the assignment will look into research of the data icons which will be used in LabVIEW and what their functions are, this research will list the common icons found in LabVIEW along with the icons used for the assignment tasks. The next part of the research will look at the digital magnitude comparators and (ADC) analogue to digital convertors. The final part of the research will look at load cells with the LCKD 1kg cell being researched. The information has been researched from creditable sources and cross checked against other sources for accuracy, the research was accompanied by a number of images further explaining text used to show a better understanding.

The next part looks at designing and testing an 8 bit magnitude comparator in the multisim PLD mode, this simulation will be tested for the three output expected which is less than, equal to and more then. The next task is the downloading of the program to the Nexys 4 DDR board to analyse the same results as above with comments on the simulation, theory and practical findings. The assignment will then move on to designing a multisim program to test the signal conditioning method to give an output of 0-5v over the full load range.

Task 5 and 6 will look at designing a LabVIEW program to interface to the FPGA containing the 8 bit comparator, this is to produce the same results as above with the less than, equal to and more than results to be shown on the boards.

In task 7 then assignment will be adapted to output the load cell value on grams over its full range value, this will be used with a graph produced in task 8 to show the actual load over the range for a period of time. A scatter graph will be created to back up these results.

The assignment is finished with a conclusion explained what was learnt from the assignment, if the assignment and tasks met the expected results and if any

problems were faced an explanation of this. The assignment includes a contents page above, a table of figures, and a bibliography with all citations included.

Very detailed introduction given

2. Research

NI DAQmx Icons used in LabVIEW program

LabVIEW uses a large variety of icons which can be used inside the program to perform different function and tasks depending on what they are assigned to do, some icons require modification and inputting of data, and other can work solely for the purpose stated in their description. Below is a list of common icons used in LabVIEW and some icons used for this assignment to build the programs stated above in the introduction.

Round to Nearest

The round to nearest icon is used to round the input to the nearest integer, the function will return to the nearest even integer if the value of the input is halfway between 2 integers. This icon was used in the assignment and will be shown in the sections below during the construction of the programs. Figure 1 below shows the 'round to nearest icon'.

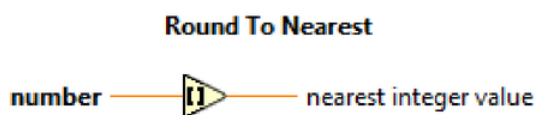


Figure 1: Round to nearest

Formulae icon

This icon is used to create formulas or calculations, it uses an interface from a calculator and with the expression VI used, most calculations that a scientific calculator can perform can be achieved in this icon. This icon was used multiple times in the assignment and will be explained to why it was used each time in the explanations below in the report. Figure 2 below shows the icon in LabVIEW. The VI expression is configured as follows; $(x1 \div 5) \times 256$.

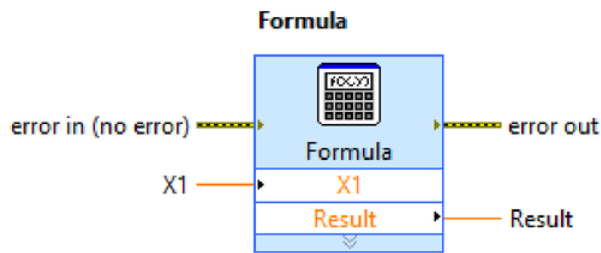


Figure 2: Formula Icon

Create channel voltage basic Icon

The create channel icon is used as a voltage measure icon by creating channels. The AI custom voltage with excitation instance of VI is used if an internal excitation is required or voltage scaling is needed. Figure 3 below shows the create channel icon and was used multiple times in the assignment programs.

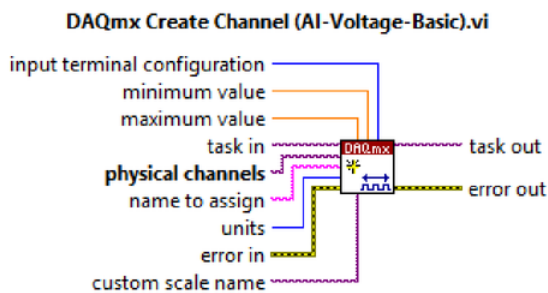


Figure 3: Create Channel

Read Icon

The read icon used in LabVIEW is used to read an individual sample of floating point that comes from a task which includes an individual input analogue channel. Figure 4 below shows this icon is LabVIEW and was used in the programs below in the assignment.

DAQmx Read (Analog DBL 1Chan 1Samp).vi



Figure 4: Read icon

Clear Icon

This clear icon is used to as stated clear a task, once the clear icon has been used the task can no longer be re used and prior to clearing the task the icon will abort the task and all resources that have been reserved will be released. Figure 5 below shows the clear icon and was used in the assignment stated below in the analysis.

DAQmx Clear Task.vi



Figure 5: Clear icon

Error out icon

The error out icon is used to output the error information, this include the standard error out functions. Figure 6 below shows the error out icon as used in the assignment.



Figure 6: Error out

While loop

A while loop is a function which is selected around a series of icons to repeat the code inside its sub diagram until the time when it sees a condition to end the loop. The while loop will execute at least once when used. Figure 7 below shows the while loop icon.

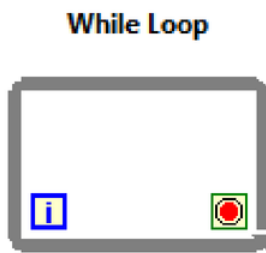


Figure 7: While loop

Create channel digital output

This create channel for the digital output is used to create a digital signal, digital lines can be grouped to one channel or can be separated to produce a variety of digital channels. Figure 8 below shows the create channel digital.

DAQmx Create Channel (DO-Digital Output).vi

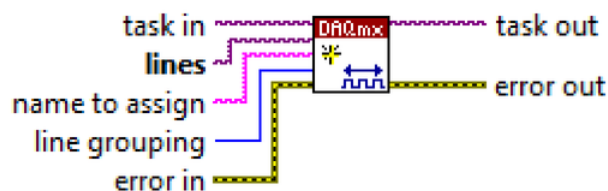


Figure 8: Create channel digital output

Write Digital icon

This icon is used to write a 32 bit unsigned integer into a task which will contain an individual output which is digital channel. For devices which have 32 lines per port use an instance which will write 32 bit integers which are unsigned. Figure 9 below shows the icon for the write channel.

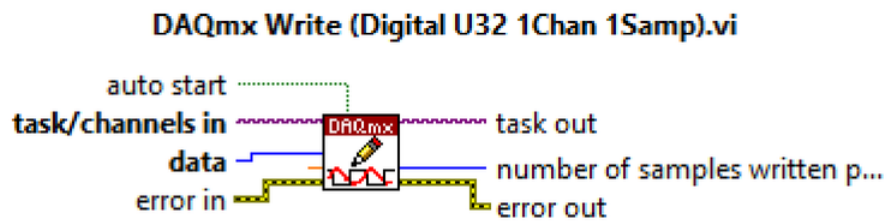


Figure 9: Write digital

Add icon

The add icon is used to add together the two inputs into the icon, this icon is used multiple times in the assignment and is shown below in figure 10.

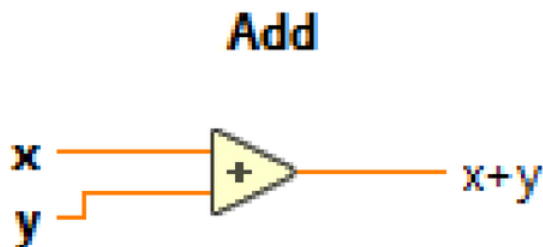


Figure 10: Add icon

Read digital Boolean

This icon is used to take information or read information from an array of Boolean numbers coming from a task which will contain an individual digital input. Figure 11 below shows a digital Boolean icon.

DAQmx Read (Digital 1D Bool 1Chan 1Samp).vi



Figure 11: Read digital Boolean

Data Icon

The data icon is used to return a 1D array of samples in Boolean form. The elements of the array will directly correspond with a digital line inside the channels. Figure 12 below shows the data icon in LabVIEW.

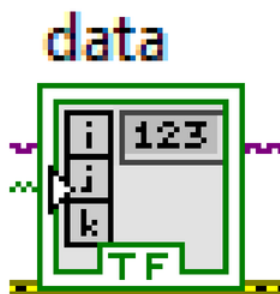


Figure 12: Data icon

Number to Boolean array

This number to Boolean array is used to convert a fixed-point number or integer into an array. When the integer to number is wired the Boolean array will give an array of 8, 16, 32 or 64, which is all dependent on the number of bits inside the integer.

Number To Boolean Array



Figure 13: Number to Boolean array

Wait (MS)

The wait icon is used to wait or delay the selected or inputted amount of milliseconds and will return the number of the milliseconds timer. Figure 14 below shows the wait icon used in LabVIEW.

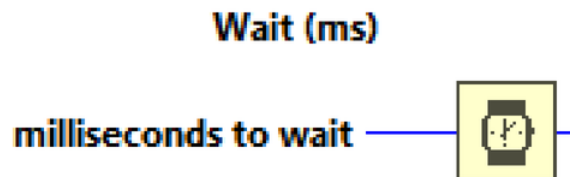


Figure 14: Wait icon

Very good detail shown in the use of the DAQmx icons within the assignment

Digital Magnitude Comparators

Digital magnitude comparators are combinational circuits which have the ability to compare two binary numbers or two digital numbers to produce a result to find out if the input value for the binary numbers is more than, equal to or less than the other binary value. The circuit is designed to have two inputs and three outputs, the inputs will be for the A&B values and the outputs will be for the A<B, A=B, A>B values. (GeeksforGeeks, 2017).

An 8 bit digital magnitude comparator like the one used in the assignment will compare values from the two 8 bit values with the use of cascading two 4 bit comparators. The configuration for the comparators connection can be seen below in figure 15 via the circuit diagram of the 8 bit comparator.

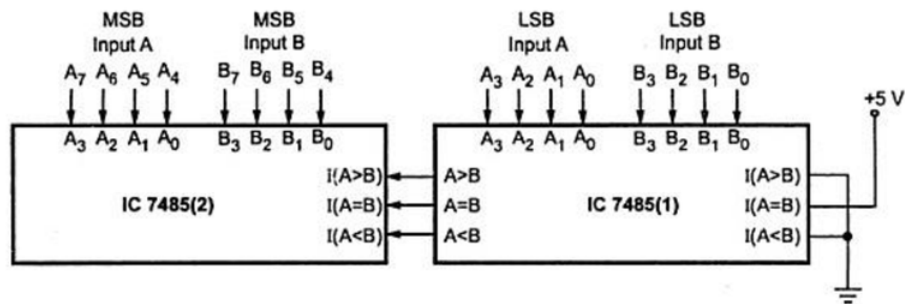


Figure 15: 8 bit comparator

The configuration shows the low order comparator connecting the values for 'a<b', 'a=b', 'a>b' connecting to the matching values for the high order comparator. In the low order comparator the, 'a=b' input is linked to the high comparator but the cascading inputs 'B' and 'A' are linked to the low comparator. The outputted values from the 8 bit comparator are taken from the high order comparator.

Comparators are used for many application such as decoding the address circuits for computers and processors to choose inputs and outputs to store their data. Other uses include control applications where number from binary source like temperatures are compared with references to indicate whether the controller needed to adjust under or over the set value to achieve the desired value of temperature, this can be used in other similar application such as positions etc. (Electronics Hub, 2015).

Good, general information given, but how does the comparator make a decision

Analogue to Digital Convertors

Analogue to digital convertors (ADC) will convert an analogue signal to a digital signal with no internal content or information being disrupted or changed. The analogue signal is a continuous variable signal and the digital is a multilevel signal. The data from the analogue source is sent or modulated through a signal transmission which is continuous, this signal is then amplified or the frequency is changed to take away or give data to the transmission. The ADC is fed by a varying voltage which can change around a number of value which are infinite. The output from the ADC consists of defined states, which in the simplest form are binary states with two states. The reason these signal are converted to digital signals is because these signals are transmitted much more efficiently as a digital pulse, making it easier to read or recover with a circuit as opposed to an analogue signal which will contain a lot of noise and interference.

Analogue to digital convertors can come in a variety of sizes which range from 8b to 24b, the voltage supply to these can also be found in different sizes from -9v to 22v depending on what circuits are used. These ADC's are used in many applications which include computers using them to convert analogue signal to digital prior to the signal being interpreted. An example is where the computer modem converts the signal from digital to analogue and then sends the signal over telephone lines which only use analogue signals, these signal is then converted back to digital so the computer can reads the digital data. (Future Electronics, 2017). Figure 16 below shows an analogue to digital convertor.

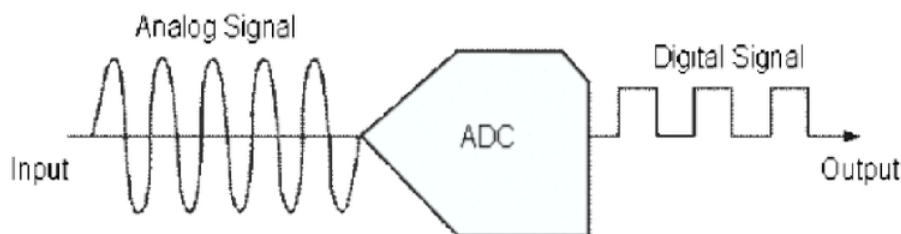


Figure 16: ADC diagram (Analog Devices, 2013).

Basic research carried out on ADC's and their configuration

Load Cells

Loadcells are a type of transducer which has the ability to change a force acting on the load cell into an electronic output which can be measured. These load cells were designed and brought into industry to replace the mechanical lever scales for carrying out applications such as industrial weighing. The strain gauge load cell dominated the industry for weighing, if an intrinsically safe atmosphere is present or high levels of accuracy are required a pneumatic load cell would be used. The strain gauge type load cell work within accuracy's of 0.03% - 0.25% for the full scale and can be used for most industrial applications.

The strain gauge load cell will change the load which acts on them and output that as an electronic signal. To achieve maximum sensitivity 4 strain gauge will be used with two of them acting in tension and the other acting in compression. Once a weight is detected or put on the strain gauge then resistance in the gauge will change with proportion to the load.

Figure 17 below shows a LCKD – 1kg load cell.



Figure 17: LCKD Load Cell (Omega, 2016).

The LCKD type load cell will measure the range from 0-1000g and will output a voltage of 0-5v.

*The output voltage would be 2mV/excitation voltage applied
Good general detail but incorrect output voltage shown, this voltage (5V) would be correct after the signal conditioning unit*

3. Design of assignment requirements

This part of the assignment makes up task 2, the task requires an 8 bit magnitude comparator to be built simulated and tested in multisim. This comparator as researched will look at three value which will include the less than, equal to and more than a set input value. The test will compare the binary values for 'B' and 'A' with 'A' being used to compare from. For example you would say 'A' is bigger or less than 'B' not the other way around. 'B7' and 'A7' are the most significant bits and are counted in binary form. Middle LED is equal, Left is 'A' higher than 'B' and Right is 'B' higher than 'A'.

The circuit was built below in multisim to produce the circuit shown in figure 18, this circuit consists of two 4 bit magnitude comparators which are connected as explained in the research along with binary inputs and LED outputs.

The first test below was carried out once the circuit was built to simulate the equal to value of '11101001' which is the value of 151. The yellow LED in the centre on the left shows the indication for the equal to value showing the simulation was successful.

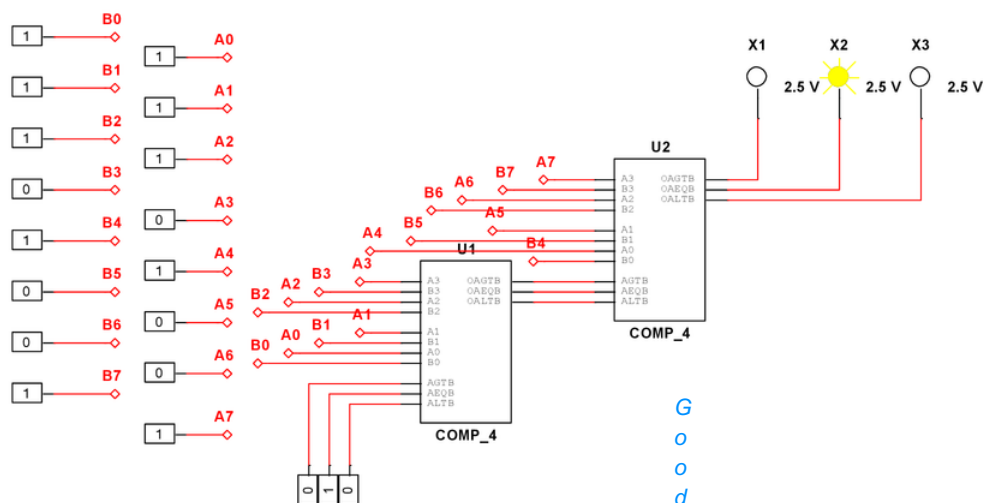


Figure 18: Equal to 11101001.

The next simulation was for the greater than value with 'A' set to '11101001' and 'B' set to '01101001' which would make 'A' greater than 'B' and should illuminate the left LED to show this simulation, figure 19 below show this left LED illuminated proving the simulation successful.

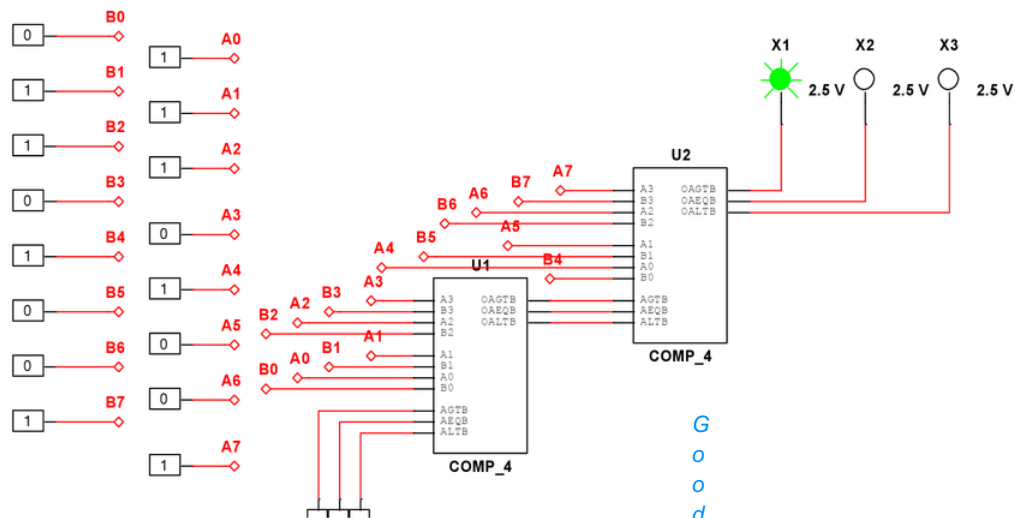


Figure 19: A greater than B

The last simulation was for the less than value with 'A' set to '01101001' and 'B' set to '11101001' which would make 'A' less than 'B' and should illuminate the right LED to show this simulation, figure 20 below show this left LED illuminated proving the simulation successful.

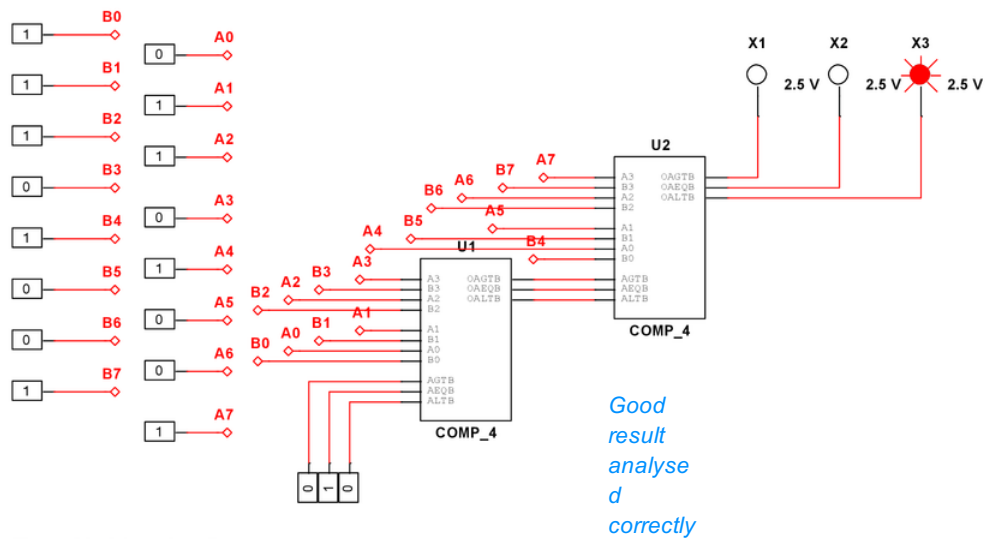


Figure 20: A less than B

3 good results shown and analysed correctly but isn't this the design stage and not the analysis stage?

The circuit will be downloaded to the Nexys 4 DDR FPGA board and tested to see if the program runs smoothly and if there is any difference compared to the simulated valued. This part will be included in the next section of the report under analysis of the signal conditioning, multisim and LabVIEW results.

Task 4 required a signal conditioning unit to be designed in multisim to give and output of 0-5v with the 0-1000gms input. The excitation voltage will be 5v. The circuit consists of four potentiometers and they are set up in a diagonal way so top left and bottom right are for increasing the value and top right and bottom left are for decreasing the values. I will take ten readings wilts varying the R1 and R4 potentiometers to increase the input value in 5% steps to 100%. The screenshots below will show this increase for the values up to 100%

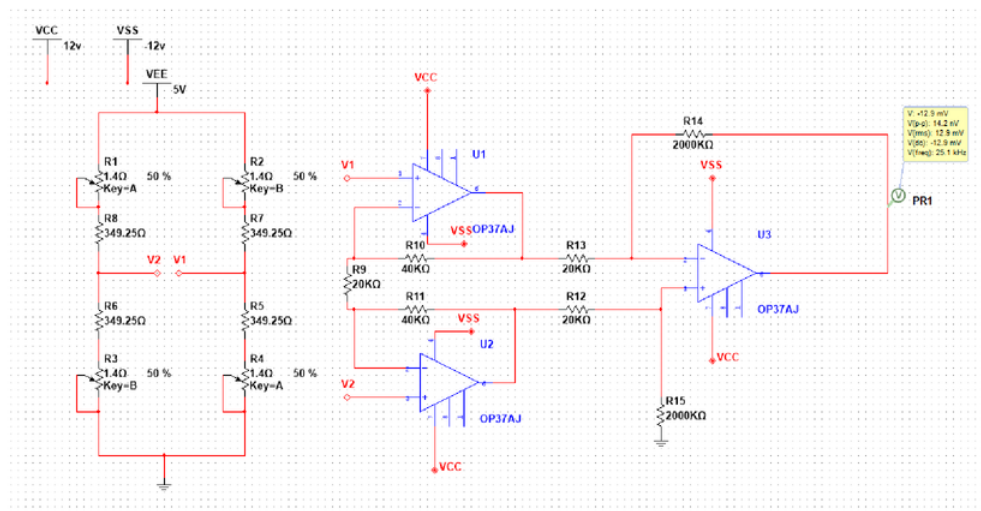


Figure 21: 0gms

Figure 21 above gave the output of 12.9mv at 0gms.

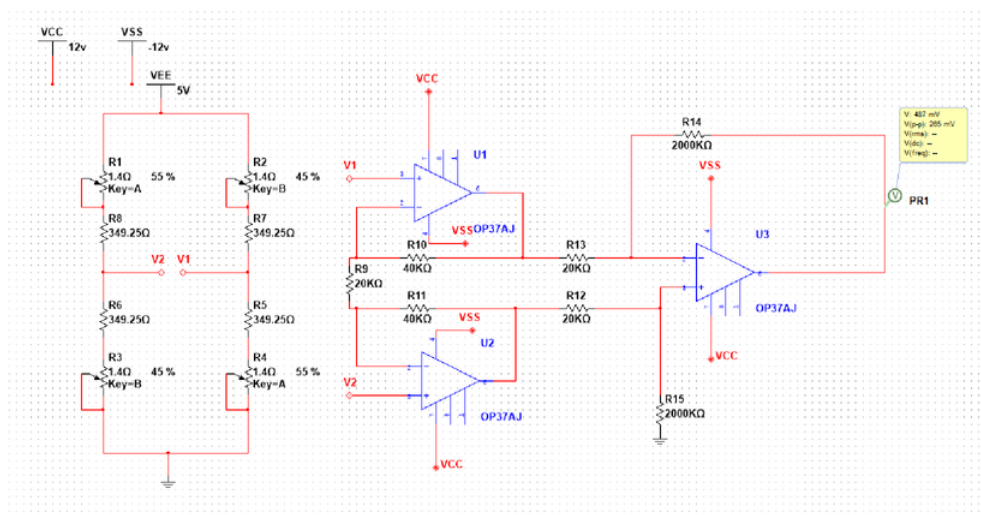


Figure 22: 100gms

Figure 22 above shows the value of 100gms which gave 487mv.

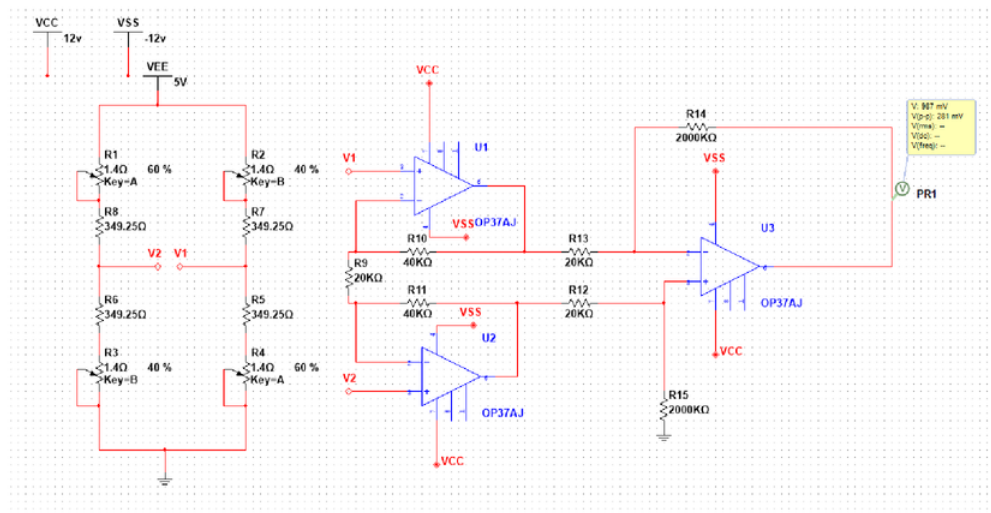


Figure 23: 200gms

Figure 23 above shows the value for 200gms which gave a reading of 987mv.

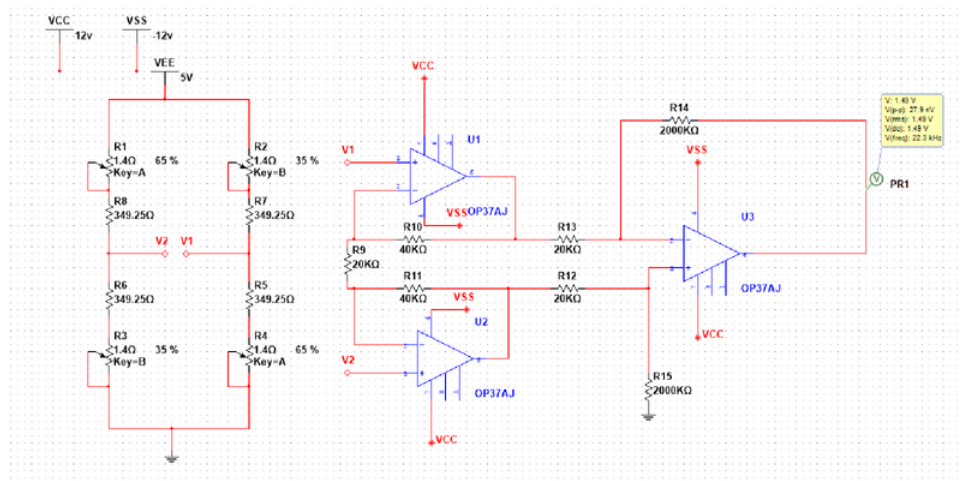


Figure 24: 300gms

Figure 24 above shows the value for 300gms which gave a reading of 1.49v.



The circuit diagram illustrates a 4-bit digital-to-analog converter (DAC) using two OP37A/J operational amplifiers. The circuit is powered by a 5V supply (VSS) and a 12V supply (VCC). The input signals are V1 and V2, which are connected to the non-inverting inputs of the two op-amp stages. The output of the first stage (U1) is connected to the inverting input of the second stage (U2) through a resistor network. The output of the second stage (U2) is connected to a potentiometer (PR1) and a 2000K resistor (R15) to ground. A yellow box indicates the output voltage V1 = 2.49 V.

Figure 26:500gms

Figure 26 above shows the value for 500gms which gave a reading of 2.49v.

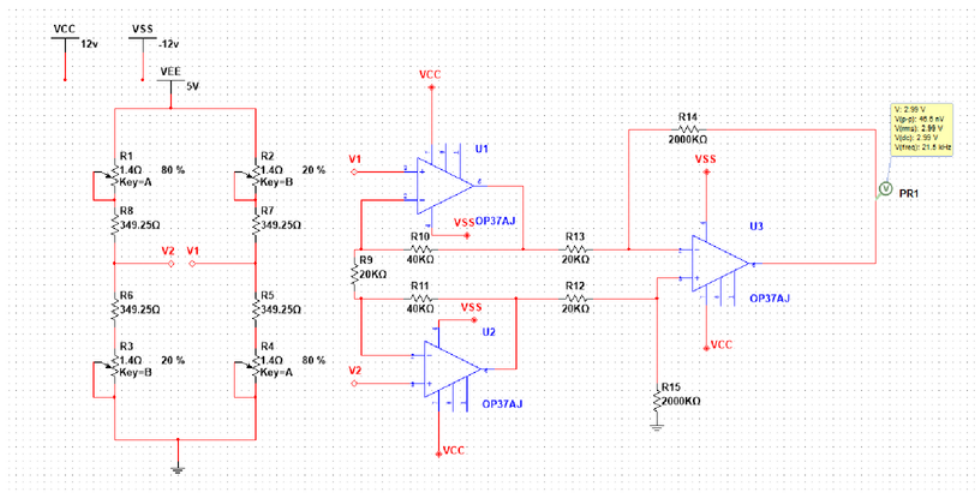


Figure 27:600gms

Figure 27 above shows the value for 600gms which gave a reading of 2.99v.

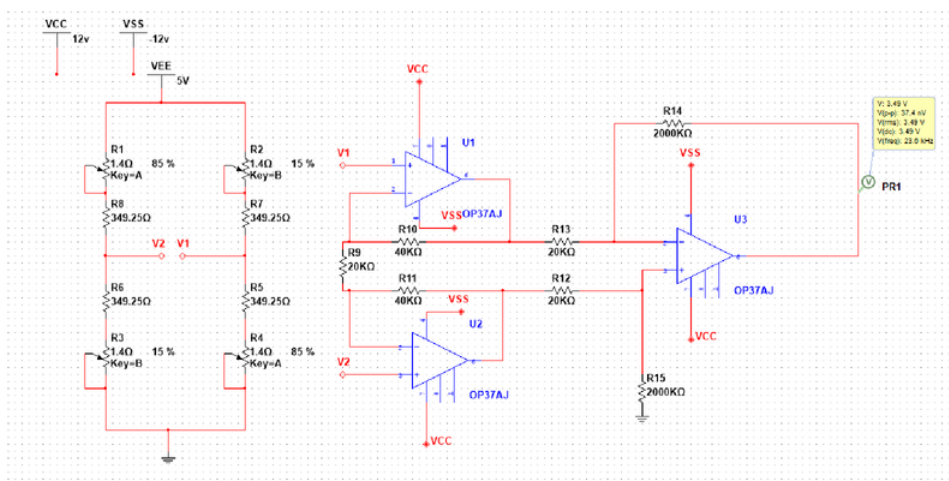


Figure 28: 700gms

Figure 28 above shows the value for 700gms which gave a reading of 3.49v.

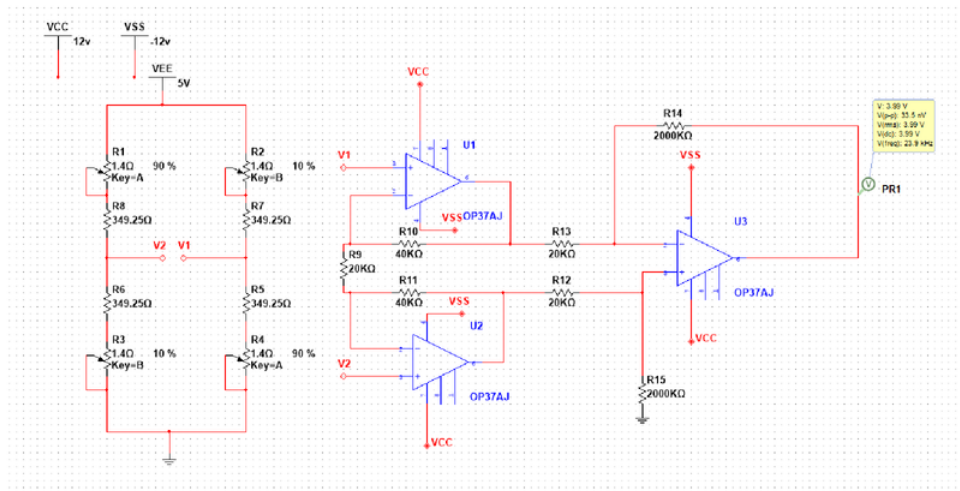


Figure 29: 800gms

Figure 29 above shows the value for 800gms which gave a reading of 3.99v.

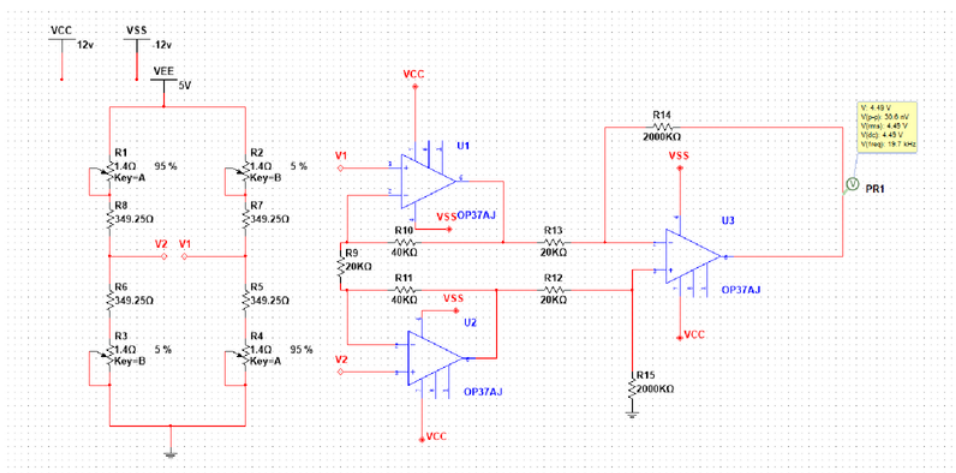


Figure 30: 900gms

Figure 30 above shows the value for 900gms which gave a reading of 4.49v.

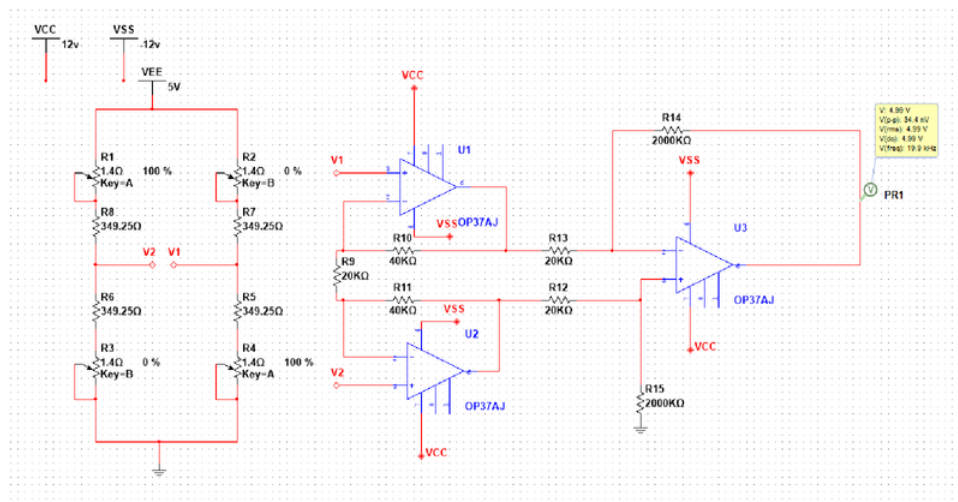


Figure 31: 1000gms

Figure 31 above shows the value for 1000gms which gave a reading of 4.99v.

A table and Graph was created on Microsoft excel with a scatter graph which is shown in figure 32 below to show the results as from the screenshots above. The table is set up to show the percentage of R1 and R4 with the grams and voltage output alongside.

%	GMS	V
50	0	0.0129
55	100	0.487
60	200	0.987
65	300	1.49
70	400	1.99
75	500	2.49
80	600	2.99
85	700	3.49
90	800	3.99
95	900	4.49
100	1000	4.99

Good schematic diagram shown but values of resistors chosen not explained. You did not need to show as many screen shots and again this is the design section and not the analysis section

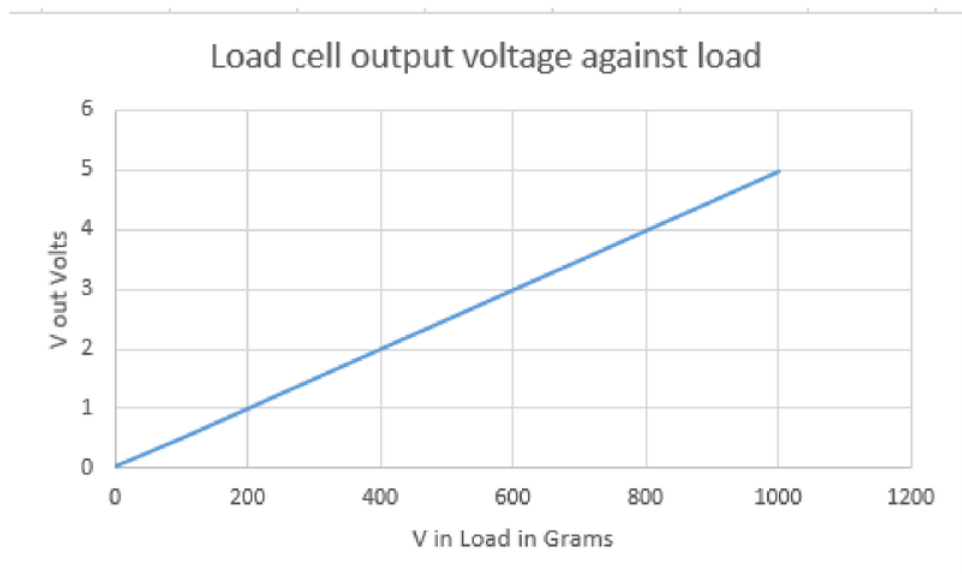


Figure 32: Voltage against load

The results from this table and graph shows the effect of the force changing the electrical value. This related to the research above and shows the weight acting on the load cell from 0-1000gms.

Section 5 will show the build for the LabVIEW 'vi' as it will incorporate into the practical section.

Good graphical representation of the signal conditioned output showing 0-5V over the load range 0-1000gms

4. Analysis of Signal Conditioning circuit, NI LabVIEW & Multisim

This part of the assignment makes up task 3 and will develop the circuit to be used on the Nexys 4 FPGA board. The mutism circuit needed to be altered so that it was compatible to be used with the Nexys 4 board, this meant changing the Highs and Lows which were in digital form to PLD components which were switched and led labelled.

Figure 33 below shows the circuit changed to the new format for transporting and exporting PLD FPGA board.

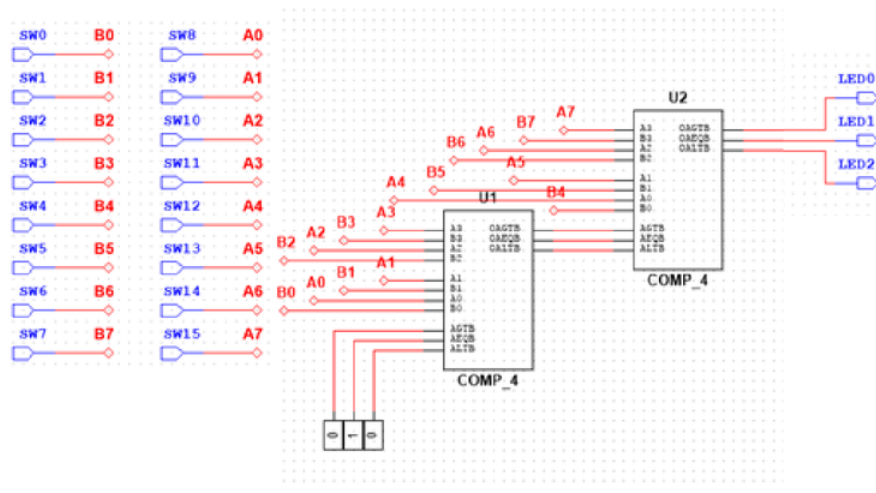
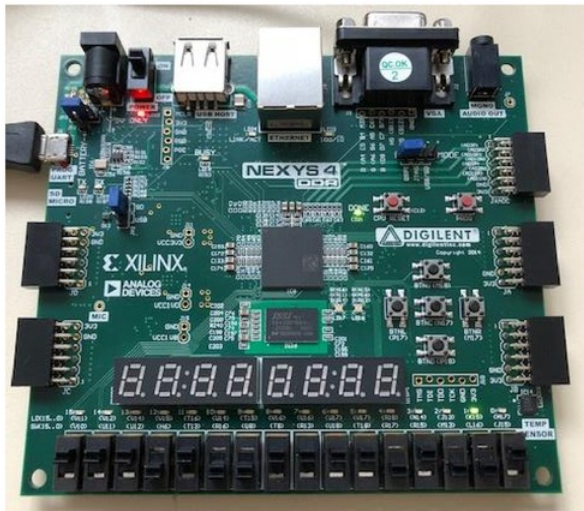


Figure 33: Multisim program to suit FPGA board

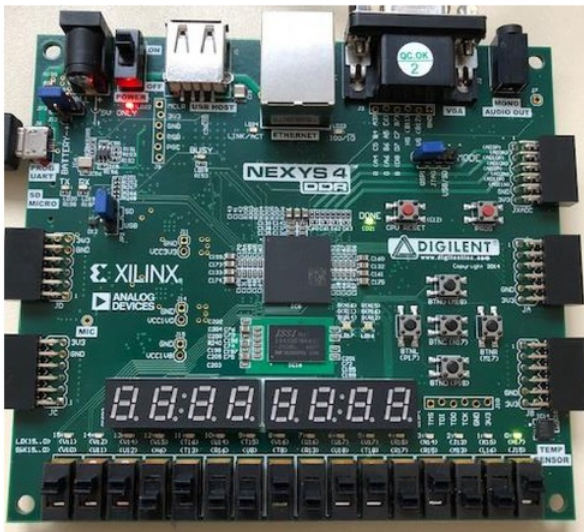
The tested results to the FPGA board are shown below in the screen shots.



Good result analysed correctly

Figure 34: Equal to test

Figure 34 above shows the switches set out with 'B' is right bank of switched and 'A' is left bank. The same binary input was set up on the switched to show the equal to value of 151. The LED illuminated is in the middle of the three LED's proving successful.



Good result analysed correctly

Figure 35: A less than B test

Figure 35 above shows 'A' set to 01101001 and 'B' set to 11101001 which should show 'A' less than 'B' and illuminate the right LED. The result above shows the right LED on meaning the test was a success.

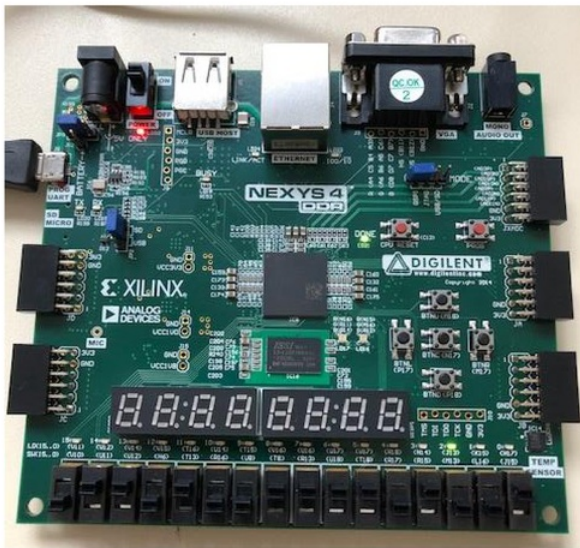


Figure 36: A more than B

Figure 36 above shows 'A' set to 11101001 and 'B' set to 01101001 which should show 'A' more than 'B' and illuminate the left LED. The result above shows the left LED on meaning the test was a success.

The above results have proved that the simulation and testing results have proven to show the same results as expected. This means the circuit can be designed and tested successfully with no problems created.

G
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5. Practical build and test via NI ELVIS board

This part of the assignment looked at task 5, this required a LabVIEW 'vi' to be designed to interface to the FPGA which will contain the 8 bit magnitude comparator through the NI ELVIS 11 board to give then comparison as above for less than, equal to and more than. The signal for 1 will be through an analogue input with the range of 0-5v which is to represent the load or 0-1000kg, and will be the digital signal output in 8 bits out of the FPGA. The signal for 2 will be taken from a set vale in LabVIEW for the range of 0-1000gms and then changed to the 8 bit digital signal output to the FPGA.

The first step was to create a 'VI' program on LabVIEW using help from the research which explained each icon and what functions they performed. The program uses the icons shown in the below screenshots and works by taking an input analogue voltage of 0-5v, the actual reading is sent to and pickup up by the input tool for the analogue which will activate the formula tool and process the signal. The formulae icon will take the read voltage form the read icon before and work out with the formulae 5×256 , the digital output. The output is then transferred to the 'right' tool were it is outputted as a digital value taken from the voltage input as explained above.

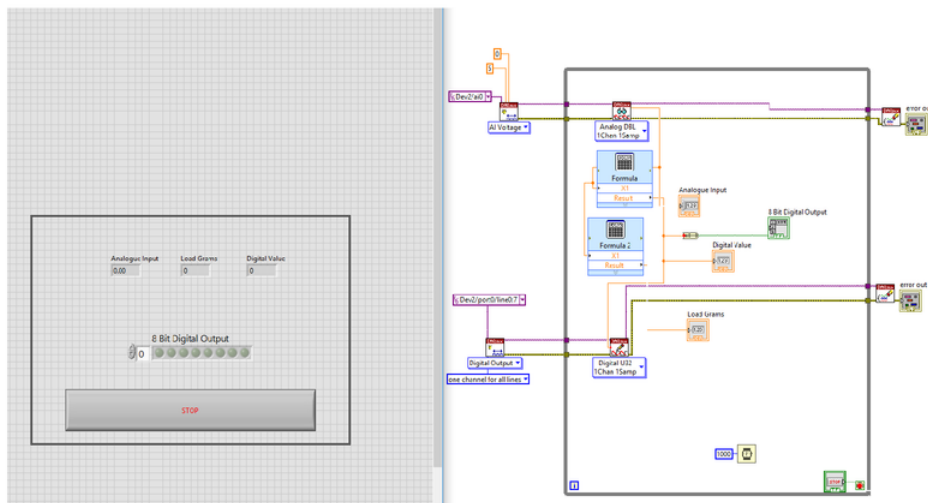


Figure 37: Task 5 VI

*Good representation of the 8 bit ADC within
LabVIEW*

Prior to adapting the design to work with the 8 bit comparator the design had to be tested for its operation, this would include setting up a test variable power supply instrument and simulating a voltage input to test if the digital value output matched with the binary LED's also illuminating. This was carried out prior to the adaption and proved a success meaning the 'vi' was operational and working correctly.

Next involved the adaption of the first 'vi' to be used alongside the multisim magnitude comparator. Figure 38 below shows this new 'vi' circuit.

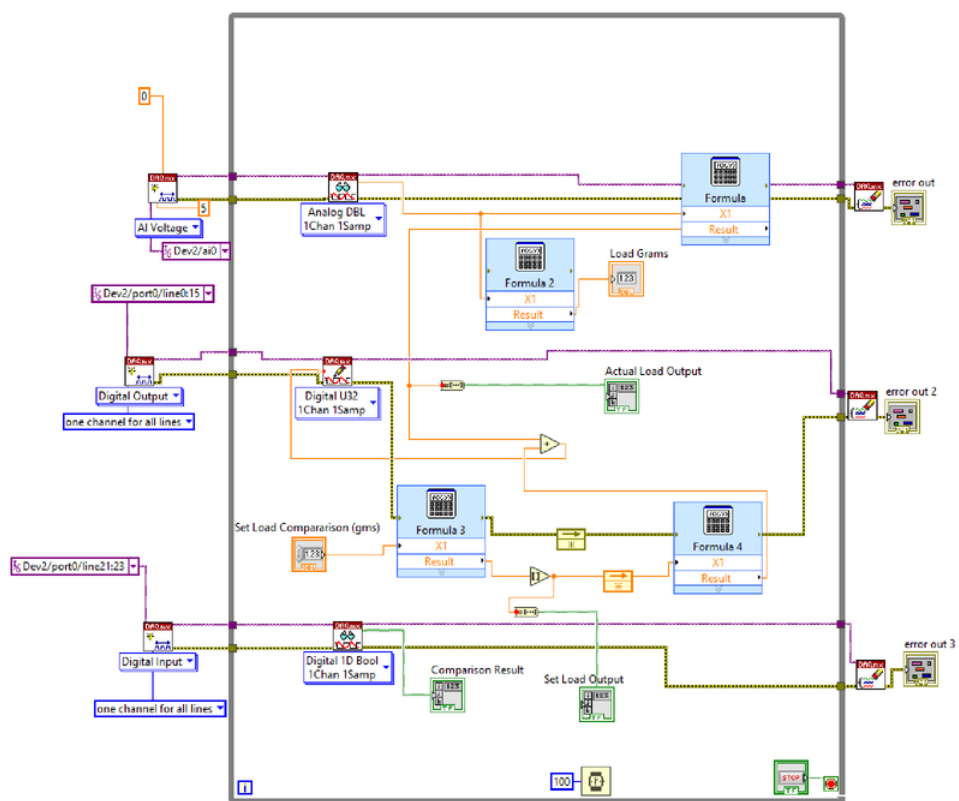


Figure 38: Task 5 adapted VI

Good design shown of the full LabVIEW 'vi' for the assignment

The circuit operates by again receiving an input voltage of 0-5v for the load (gms). The signal is then sent along to the formula 2 and formulae icons, these divide the input signal with 5×256 as above, which then go to the icon for 'actual load output', and used for a value for comparison. The formulae 2 icon is used to divide the analogue value with 5×1000 and then send it to the load output icon which has converted it into grams. This output value is send to the display part at the load grams icon. The clear part will end the first part of the program.

The digital output uses a signal from 0-15 as shown in the icon and will write with the sum of the formulae and formulae 4 icons. Formulae 3 uses $X1 / 1000 \times 256$ which is the set load input for the first set of bits in the comparator. Formulae 4 is the first set of bits times by the value of 256 to make another 8 bit comparator. The equation entered is $X1 \times 256$. *The actual formulae are $(x1/5) \times 100$ and $(x1/5) \times 256$*

The last section of the program is for the outputting the value of greater then, equal to or less than value coming from line 21 to 23 which are digital inputs. There is a 100ms wait in the circuit acts as a delay of this 100ms before the values are started again or inputted back into the system. The final part is the stop button to act as an emergency stop or reset to stop the system on demand.

Figure 39 below shows the multisim program changed to a PMOD program, jb5 and jb6 are ground and a dc connector hence why it jumps from jb4 to jb7.

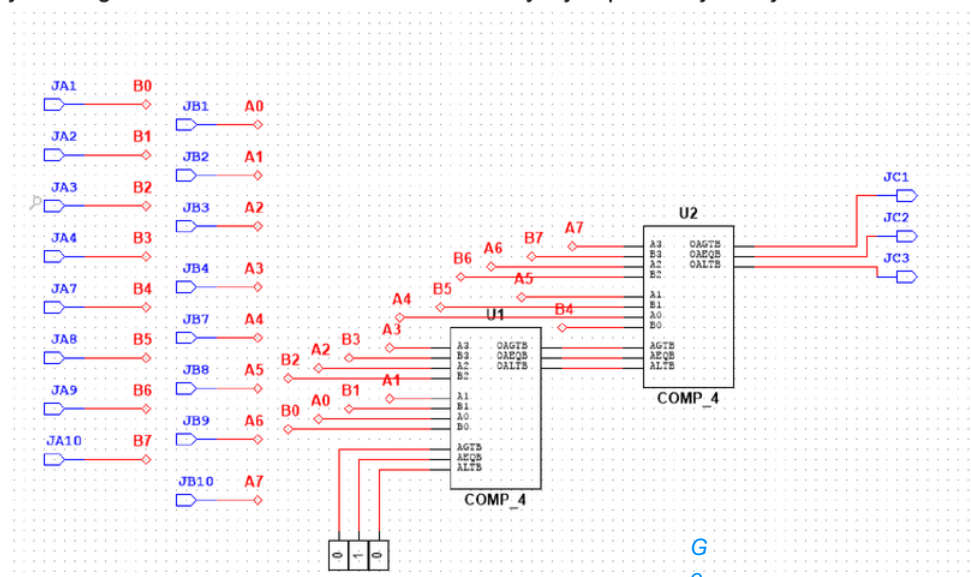


Figure 39: Modified multisim circuit for comparator

The results will be tested to the ELVIS board and FPGA and shown below in the screenshots, the connections are shown below.

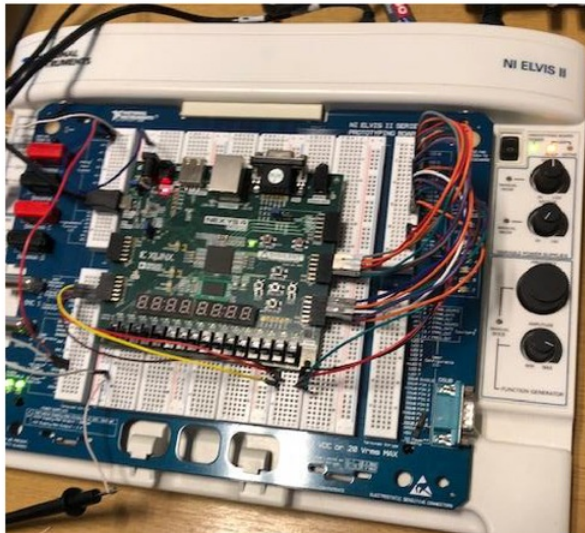


Figure 40: Practical ELVIS results

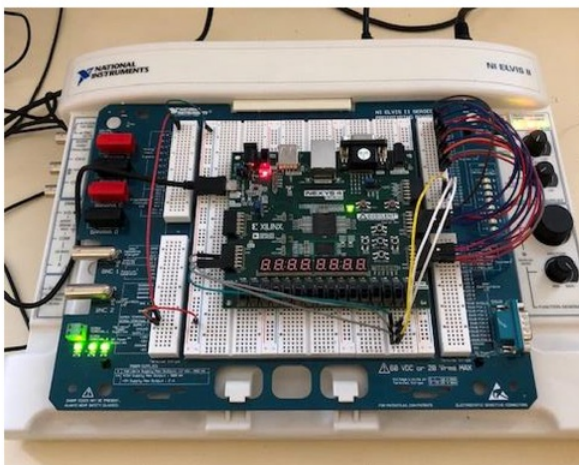


Figure 41: Practical ELVIS board operating

The practical deployment to the ELVIS board proved that all the channels were working correctly and the board worked when all the connections as above were connected and powered up.

6. Analysis of NI LabVIEW/FPGA results

This part of the assignment required the NI LabVIEW circuit designed above in part 5 to be tested with three values for the below, equal to and more than results expected. This was done by again showing the adaption to the multisim program to operate with the required software.

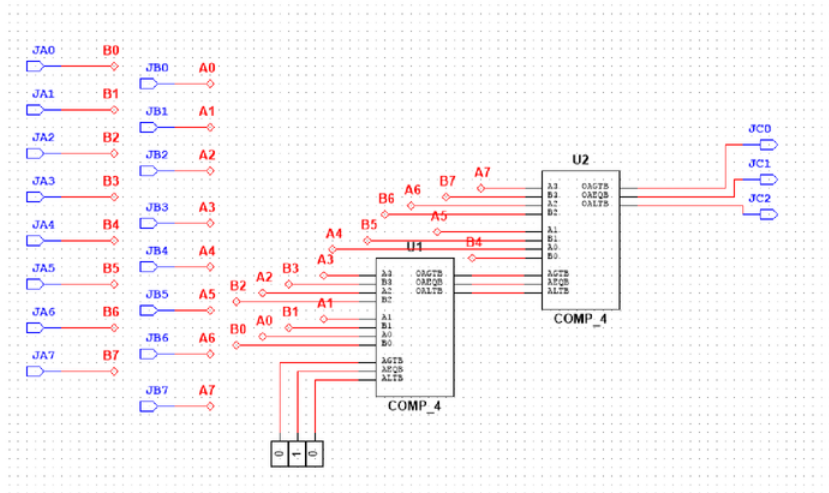
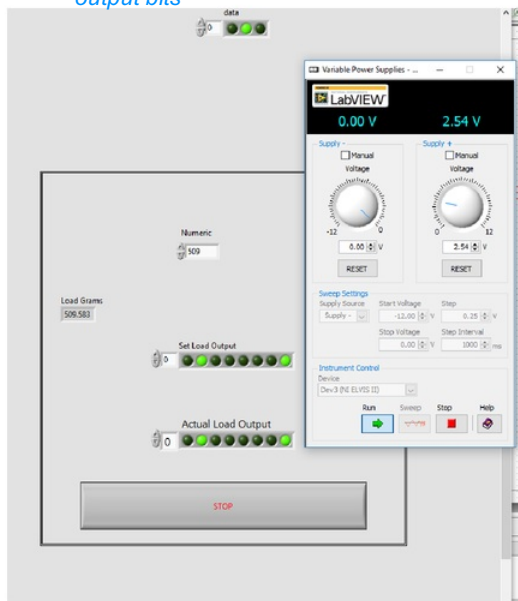


Figure 42: Multisim program modified

The first simulation was carried out for the equal to value, this was done with the use of a variable power supply instrument to input the varied power supply to mimic a varied load to simulate against the set load which will be inputted into the LabVIEW design as shown below in the three tests.

The first test shown below in figure 43 was for the equal to value, the set value of 500 grams was inputted and the voltage was varied to 2.54v which would give the 500gms output, as shown the program shows a middle LED illumination with the set load and actual load value being them same meaning the output is equal to.

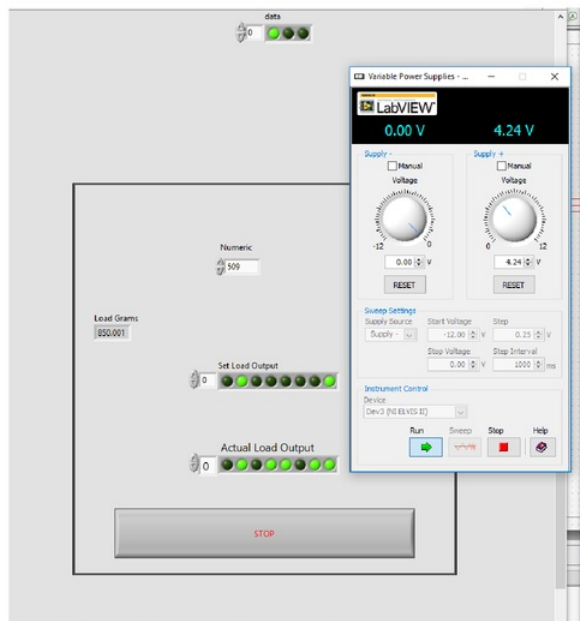
Would have been nice to have a legend on the 3 FPGA output bits



Good result analysed correctly

Figure 43: Equal to LabVIEW

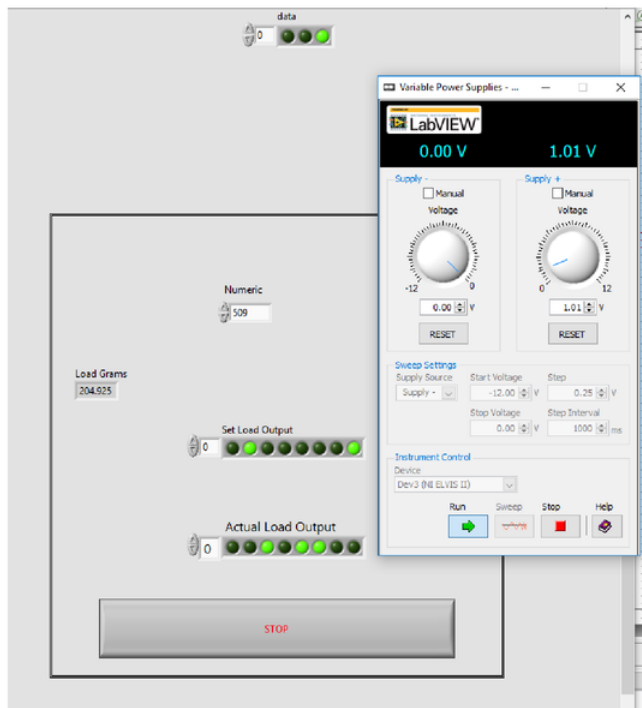
The second test below in figure 44 is looking at a more than value, the load value is set at 500gms again and the variable power supply was set to 4.24v or 800gms which would be a greater than value, the greater than LED shown as the far left is illuminated meaning the test was a success.



Good result analysed correctly

Figure 44: LabVIEW more than test

The last test was for the state of less than, this would again require the set value in grams to be set at 500 and a lower than variable voltage applied. The voltage applied was 1.01v which was equal to 204 grams which is under the set 500 grams, the far left LED was illuminated and proved the simulation was working as expected.



Good result analysed correctly

Figure 45: LabVIEW less than

These results proved as expected results that the program works correctly and they LabVIEW 'vi' is operating as it should.

7. Adapt design for new purpose

This part of the report requires the VI LabVIEW program built in task 5 to be adapted to output the load cell values measured in grams, over the full range of 0-5v along with comparison results to a data logging file format. Figure 46 below shows the new design which has been modified from the original design.

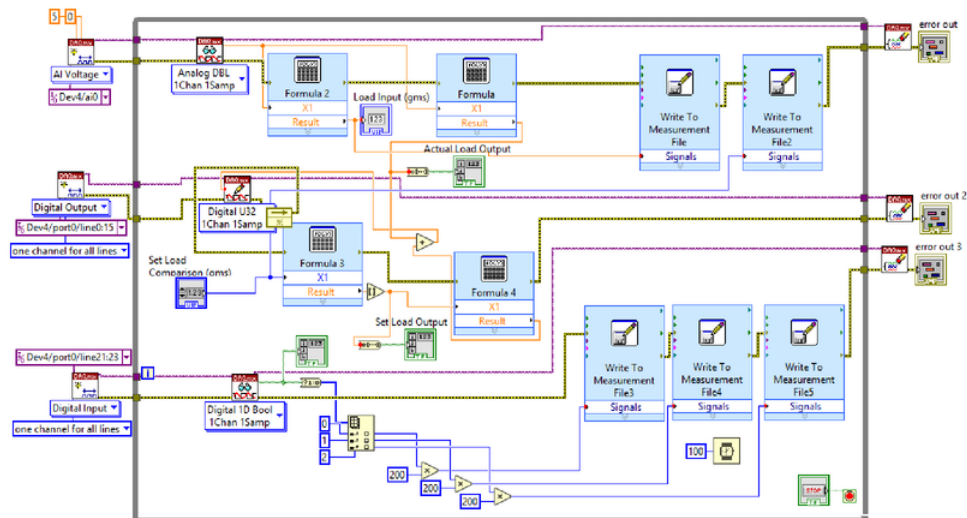


Figure 46: New VI design full range

The data that is being logged in this vi deign includes, the set load comparison, the load input, the load input less than set load, the load input equal to set load and the load input more than the set load. The new file has the same functions as the old file for the original icons, which can be seen above. The second line of icons function is to take the value of grams which is in a digital form, to separate the 0-1000 number and convert it into a 0-8-bit string which will reach 0-256 in value. The number is rounded up to the closest whole number to prevent it interfering with the other 0-8-bit string. The new parts are added to take the three input values which are found on the bottom line of the above program, and times each of them by 200. This is done so that the results can be seen on a graph, the three write to measurement icons added to the bottom right of the circuit give the program the ability to show the

values of less than, equal and more than onto a graph. The write to measures at the top of the 'vi' provide a write grams value which will fluctuate and a set load value.

Below in figure 47 shows the new program running and a set value of 300 and an input load value of 309 which would be less than the set value, the figure shows the value producing a greater than indication on the magnitude comparator result indication.

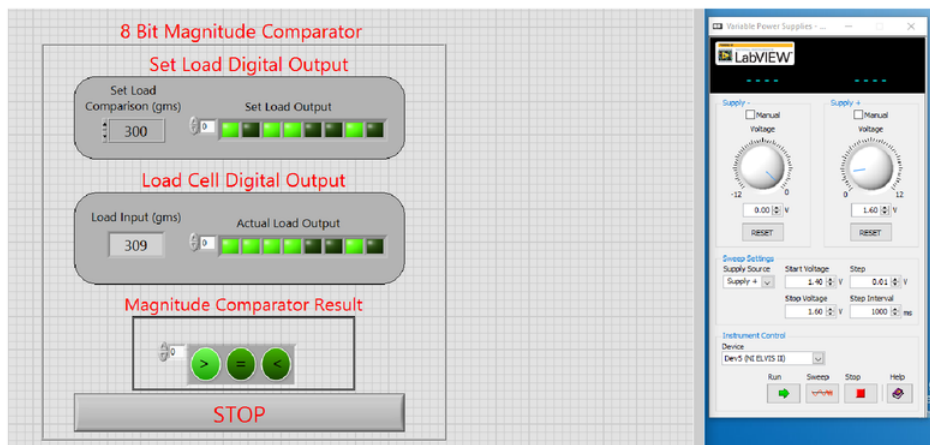


Figure 47: New vi simulation

New LabVIEW 'vi' explained to a reasonable level

8. Analysis of data Logging on EXEL

A graph was produced on Microsoft excel for the actual load over the range for a timer period for all the comparisons. The table was too large to add into this section of the report so it has been attached in the appendix section for reference. A graph was produced from the table results below to produce figure 48.

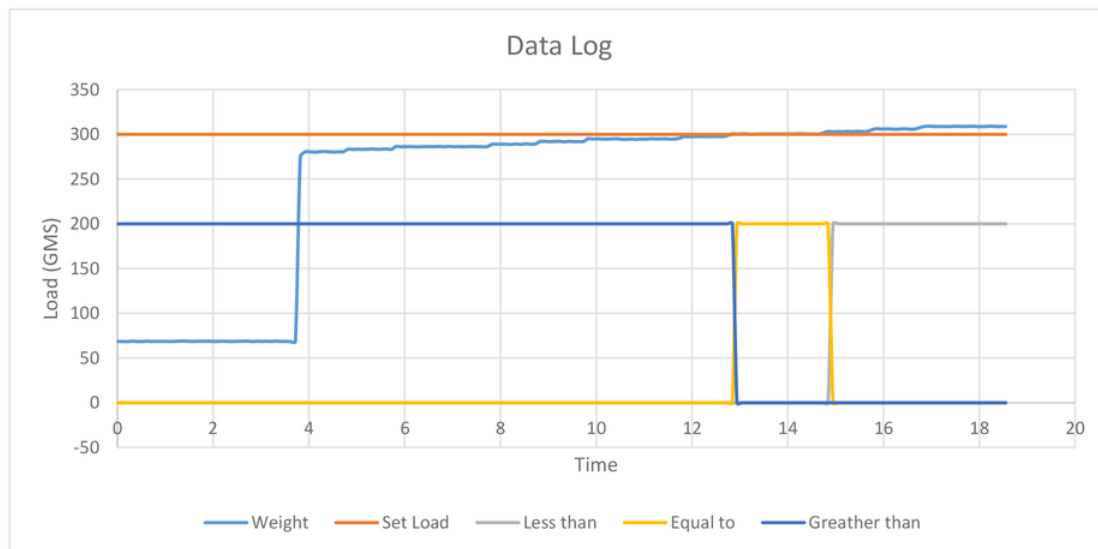


Figure 48: Graph for actual load over range

The graph shows the set load which is the red running line and is set to 500 grams, this is alongside the sky-blue colour which is representing the weight or the load, this load will increase as described above and does so in gradual steps of 5%. The dark blue line represents the greater than value, the yellow line is the equal to value and the grey line is the less than value. As the 'vi' has multiplied the values by 200, the on and off values would be 200 and 0. The lines below show the greater than line being at 200 until around 13 seconds when the two top lines meet which changed the yellow equal to line to 200 and then after 2 seconds sets the less than to equal 200 meaning the set load is less than the weight and vice versa for the start.

The graph proved that the values entered to the table were correct and the new adaption worked as expected with no errors.

Good explanation given

9. Conclusions

The assignment on a whole proved to be very helpful and a lot was learnt from carrying out the research and completing the design, simulations and testing. All results that were obtained were as expected and no difficulties or problems were found.

The research gave a good understanding of what task each data acquisition icon performed along with researching additional icons which could be added to future programs. The icons were listed in a readable layout and all the information was sourced directly from the help function inside LabVIEW and lecture teachings. The research then moved onto the digital magnitude convertors which gave a good understanding of how this equipment works, the comparators were used in the other sections of the report and were referred back to a number of times. This section helped a lot in building and analysing the programs used in the assignment. The next part of the research was the ADC section, this was a helpful section again by providing useful information to help with the analysis and program building. The last section looked at load cells, these load cells were used in the assignment so the research again built knowledge to build and analyse the programs. All sources used were creditable sources and are listed in the citation list.

The design section of the report is where most of the programs used are shown built with explanations on what they are doing along with analysis into their performance. The programs were built with the aid of the research and analysed with referring back to researched information.

The analysis section for the signal conditioning section gave an area to test the designs built and analysed further to what has been performed and what the results showed. The results gained from this section proved that the designs were working as they should and the results were good and as expected.

The practical build gave the opportunity to take the NI LabVIEW program and see if it operates with the ELVIS board and Nexys board correctly, as the section showed the practical was a success and all the ports and connections were correct. The analysis section of the NI program was again as the analysis above, an area to further explain the programs and comment on the results obtained. The NI program worked correctly and the LED indicators all shown the correct, less than, equal or more than values.

Adapting the NI program was another area of modifying the program and with the addition of some extra icons the program was able to output the actual load cell value in grams, all over the range and comparison values. The adaption proved a success and the results were used to build a table and graph to show an indication of what was happening.

Overall the assignment was a success, a lot was learnt from the research and the practical sessions carried out at college, with further adaptations the program could have more uses and with the skills gained in this assignment different types of

programmes could be built for different real-world situations. I feel I have explained the program to the best of my ability and with more practice and experience using the system the terminology and deployment could be improved.

Good conclusion given which included some reflection on what has been learned

10. Appendices including bibliography

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Good, varied set of works cited

Task 7 and 8 table used to produce the graph.

Voltage	Weight	Set Load	Less than	Equal to	Greater than
0	68.57283	300	0	0	200
0.208555	68.34741	300	0	0	200
0.308822	68.76606	300	0	0	200
0.409119	68.44402	300	0	0	200
0.509355	68.41181	300	0	0	200
0.609621	68.76606	300	0	0	200
0.709887	68.47622	300	0	0	200
0.809152	68.60504	300	0	0	200
0.910421	68.57283	300	0	0	200
1.01069	68.54063	300	0	0	200
1.110968	68.44402	300	0	0	200
1.21224	68.70165	300	0	0	200
1.313494	68.92707	300	0	0	200
1.410751	68.89487	300	0	0	200
1.511051	68.60504	300	0	0	200
1.611314	68.60504	300	0	0	200
1.71055	68.76606	300	0	0	200
1.810816	68.79826	300	0	0	200
1.912119	68.76606	300	0	0	200
2.011351	68.57283	300	0	0	200
2.112652	68.70165	300	0	0	200
2.211887	68.83046	300	0	0	200
2.313157	68.57283	300	0	0	200
2.411415	68.37961	300	0	0	200
2.511795	68.79826	300	0	0	200
2.61295	68.70165	300	0	0	200
2.714219	68.95928	300	0	0	200
2.81452	68.44402	300	0	0	200
2.915756	68.76606	300	0	0	200
3.015019	68.57283	300	0	0	200
3.115286	68.76606	300	0	0	200
3.216558	68.60504	300	0	0	200
3.314817	68.83046	300	0	0	200
3.416087	68.63724	300	0	0	200
3.516355	68.57283	300	0	0	200
3.616619	68.41181	300	0	0	200
3.717889	68.70165	300	0	0	200
3.818155	274.1949	300	0	0	200
3.917424	280.2814	300	0	0	200
4.018692	280.5391	300	0	0	200
4.117954	280.1526	300	0	0	200

4.22023	280.6679	300	0	0	200
4.318488	280.8933	300	0	0	200
4.418763	280.5713	300	0	0	200
4.520023	280.2814	300	0	0	200
4.618284	280.5391	300	0	0	200
4.718552	280.6679	300	0	0	200
4.818913	283.4052	300	0	0	200
4.919087	283.1476	300	0	0	200
5.018433	283.3086	300	0	0	200
5.119627	283.212	300	0	0	200
5.219885	283.4052	300	0	0	200
5.320154	283.6951	300	0	0	200
5.420427	283.2764	300	0	0	200
5.520686	283.3408	300	0	0	200
5.620952	283.7595	300	0	0	200
5.721219	283.2764	300	0	0	200
5.820483	286.4324	300	0	0	200
5.920749	286.1104	300	0	0	200
6.022018	286.3358	300	0	0	200
6.122289	286.3036	300	0	0	200
6.222553	286.046	300	0	0	200
6.325827	286.1748	300	0	0	200
6.42409	286.368	300	0	0	200
6.523354	286.3036	300	0	0	200
6.623677	286.368	300	0	0	200
6.724891	286.4646	300	0	0	200
6.826158	286.1104	300	0	0	200
6.924418	286.5934	300	0	0	200
7.029699	286.2392	300	0	0	200
7.12511	286.2714	300	0	0	200
7.225221	286.1748	300	0	0	200
7.324503	286.2714	300	0	0	200
7.42478	286.368	300	0	0	200
7.526019	286.207	300	0	0	200
7.624299	286.1104	300	0	0	200
7.726568	286.3358	300	0	0	200
7.824911	288.9765	300	0	0	200
7.926083	289.0409	300	0	0	200
8.025489	289.0409	300	0	0	200
8.126659	288.9765	300	0	0	200
8.226885	288.7511	300	0	0	200
8.327164	289.2664	300	0	0	200
8.427458	288.8477	300	0	0	200
8.528687	289.4274	300	0	0	200
8.628049	289.0087	300	0	0	200

8.730224	289.2986	300	0	0	200
8.826507	292.0037	300	0	0	200
8.927784	292.1647	300	0	0	200
9.029017	291.8427	300	0	0	200
9.128284	292.1647	300	0	0	200
9.22855	292.2291	300	0	0	200
9.328818	291.6173	300	0	0	200
9.429082	292.1647	300	0	0	200
9.52935	291.8749	300	0	0	200
9.629618	291.9393	300	0	0	200
9.731894	292.0359	300	0	0	200
9.829158	295.0631	300	0	0	200
9.929467	294.7733	300	0	0	200
10.02969	295.0309	300	0	0	200
10.12999	294.7411	300	0	0	200
10.23222	294.7089	300	0	0	200
10.33149	294.9021	300	0	0	200
10.43277	295.0631	300	0	0	200
10.53302	294.419	300	0	0	200
10.63228	294.4834	300	0	0	200
10.73455	294.6767	300	0	0	200
10.83282	294.3868	300	0	0	200
10.93409	294.7089	300	0	0	200
11.03335	294.6123	300	0	0	200
11.13462	294.9987	300	0	0	200
11.23589	294.9343	300	0	0	200
11.33616	294.9021	300	0	0	200
11.43843	295.0309	300	0	0	200
11.53569	294.6445	300	0	0	200
11.63597	294.7733	300	0	0	200
11.74026	295.6428	300	0	0	200
11.83548	297.7361	300	0	0	200
11.93876	297.2852	300	0	0	200
12.03903	297.5106	300	0	0	200
12.13829	297.575	300	0	0	200
12.23856	297.6072	300	0	0	200
12.33983	297.3174	300	0	0	200
12.43909	297.7038	300	0	0	200
12.53835	297.575	300	0	0	200
12.63862	297.6072	300	0	0	200
12.74089	298.7666	300	0	0	200
12.84216	300.4734	300	0	0	200
12.93842	300.2158	300	0	200	0
13.03871	300.6022	300	0	200	0
13.13897	300.5056	300	0	200	0

13.24022	300.1192	300	0	200	0
13.34049	300.3124	300	0	200	0
13.43975	300.3446	300	0	200	0
13.54002	300.5378	300	0	200	0
13.63928	300.3446	300	0	200	0
13.74158	300.5378	300	0	200	0
13.83982	300.3768	300	0	200	0
13.94111	300.5056	300	0	200	0
14.03935	300.3768	300	0	200	0
14.13961	300.409	300	0	200	0
14.23988	300.6666	300	0	200	0
14.34016	300.6022	300	0	200	0
14.44041	300.2802	300	0	200	0
14.54068	300.3768	300	0	200	0
14.64109	300.2158	300	0	200	0
14.74222	301.6005	300	0	200	0
14.84048	303.2108	300	0	200	0
14.94275	302.8565	300	200	0	0
15.04201	303.1786	300	200	0	0
15.14231	302.8887	300	200	0	0
15.24255	303.3074	300	200	0	0
15.34482	303.1141	300	200	0	0
15.44408	303.404	300	200	0	0
15.54335	303.1786	300	200	0	0
15.64362	303.1463	300	200	0	0
15.74388	304.9498	300	200	0	0
15.84416	306.2701	300	200	0	0
15.94341	305.9803	300	200	0	0
16.04371	306.1091	300	200	0	0
16.14396	305.9803	300	200	0	0
16.24823	305.7227	300	200	0	0
16.34348	305.9803	300	200	0	0
16.44374	306.2701	300	200	0	0
16.54401	305.7871	300	200	0	0
16.64331	305.9481	300	200	0	0
16.7446	307.4295	300	200	0	0
16.84481	308.7821	300	200	0	0
16.94611	309.1363	300	200	0	0
17.04535	308.8465	300	200	0	0
17.14561	308.7499	300	200	0	0
17.24689	308.8143	300	200	0	0
17.34915	308.7177	300	200	0	0
17.44741	308.9109	300	200	0	0
17.54868	309.0075	300	200	0	0
17.64896	308.8143	300	200	0	0

17.74921	308.8465	300	200	0	0
17.84848	309.0075	300	200	0	0
17.94875	308.7177	300	200	0	0
18.04905	308.6855	300	200	0	0
18.14828	308.8143	300	200	0	0
18.24855	309.1363	300	200	0	0
18.34984	308.7821	300	200	0	0
18.45008	308.8465	300	200	0	0
18.54938	308.8465	300	200	0	0

PSDE 5029 Assn 2

GRADEMARK REPORT

FINAL GRADE

GENERAL COMMENTS

61 / 100

Instructor

PAGE 1

PAGE 2

PAGE 3

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PAGE 5

PAGE 6

Text Comment. Very detailed introduction given

PAGE 7

PAGE 8

PAGE 9

PAGE 10

PAGE 11

PAGE 12

Text Comment. Very god detail shown in the use of the DAQmx icons within the assignment

PAGE 13

Text Comment. Good, general information given, but how does the comparator make a decision

PAGE 14

Text Comment. Basic research carried out on ADC's and their configuration

PAGE 15

Text Comment. The output voltage would be 2mV/excitation voltage applied

Text Comment. Good general detail but incorrect output voltage shown, this voltage (5V) would be correct after the signal conditioning unit

PAGE 16

Text Comment. Good result analysed correctly

PAGE 17

Text Comment. Good result analysed correctly

PAGE 18

Text Comment. Good result analysed correctly

Text Comment. 3 good results shown and analysed correctly but isn't this the design stage and not the analysis stage?

PAGE 19

PAGE 20

PAGE 21

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PAGE 24

Text Comment. Good schematic diagram shown but values of resistors chosen not explained.

Text Comment. You did not need to show as many screen shots and again this is the design section and not the analysis section

PAGE 25

Text Comment. Good graphical representation of the signal conditioned output showing 0-5V over the load range 0-1000gms

PAGE 26

PAGE 27

Text Comment. Good result analysed correctly

Text Comment. Good result analysed correctly

PAGE 28

Text Comment. Good result analysed correctly

PAGE 29

Text Comment. Good representation of the 8 bit ADC within LabVIEW

PAGE 30

Text Comment. Good design shown of the full LabVIEW 'vi' for the assignment

PAGE 31

Text Comment. The actual formulae are $(x1/5) * 100$ and $(x1/5) * 256$

Text Comment. Good design shown for FPGA download

PAGE 32

PAGE 33

PAGE 34

Text Comment. Would have been nice to have a legend on the 3 FPGA output bits

Text Comment. Good result analysed correctly

Text Comment. Good result analysed correctly

PAGE 35

Text Comment. Good result analysed correctly

PAGE 36

PAGE 37

Text Comment. New LabVIEW 'vi' explained to a reasonable level

PAGE 38

Text Comment. Good explanation given

PAGE 39

Text Comment. Good conclusion given which included some reflection on what has been learned

Text Comment. Good, varied set of works cited

GRADING FORM: CSG-RUBIC

NATHAN SMITH

61

RESEARCH-INFORMED LITERATURE



Analogue / Digital Converters: Basic research carried out on ADC's and their configuration (2/5)
Load Cells: Good general detail but incorrect output voltage shown this voltage would be correct after the signal conditioning unit (2/5) Digital Magnitude Comparators: Good, general information given, but how does the comparator make a decision? (2/5) NI DAQmx in LabVIEW: Very good detail shown in the use of the DAQmx icons within the assignment (4/5)

10

KNOWLEDGE AND UNDERSTANDING



Design of the signal conditioning circuit for LCKD-1Kg Load Cell: Good schematic diagram shown but values of resistors chosen not explained. (2/5)
Design of LabVIEW 'vi': Incorrect formulae shown in the design but good design shown and analysed satisfactorily. (5/10) Design of 4/8-bit Magnitude Comparator: 3 good results shown in MultiSim and analysed correctly but isn't this the design stage and not the analysis stage? Good design shown for FPGA download (6/10) Re-design to suit new applications: New LabVIEW 'vi' explained to a reasonable level (3/5)

16

ANALYSIS



Analysis of signal conditioning circuit: Good graphical representation of the signal conditioned output showing 0-5V over the load range 0-1000gms (4/5) Analysis of MultiSim Results: Good analysis of MultiSim results (3/5) Analysis of NI LabVIEW / FPGA results: Good screen shots shown from the LabVIEW front panel showing correct operation of 'less than', 'equal to' and 'greater than' the set value (7/10) Analysis of data logging files in EXCEL: Good explanation given (4/5)

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PRACTICAL APPLICATION AND DEP.



Build interface between LabVIEW and the FPGA board via the NI ELVIS 11 board: Good Pictorial evidence present in the final report and explained satisfactorily (6/10)

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SKILLS FOR PROFESSIONAL PRAC.

Deployment of appropriate media: Good use made



of screen shots and photographic evidence which helped explain design and analysis within the report (4/5) Report layout and readability: Report flow a bit confusing as the design and analysis sections sometimes overlapped (3/5) Appropriate conclusion: Good conclusion given which included some reflection on what has been learned (4/5)