

1809800

by Iwan CostelloDowns

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Name:	Iwan Downs
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1. Research

Combinational Logic Circuits

Combinational logic relies on the use of logic gates such as AND, NAND and NOT gates, therefore making them reliant on the input. No feedback is used with combinational circuitry.

They carry out operations like subtraction, addition or digital signal conversions from binary to BCD and vice versa. The output can be expressed in truth tables with logic gates and Boolean algebra. Most importantly they have no memory element.

Sequential Logic Circuits

The sequential circuit uses logic gates as well as the use of feedback acting as a memory element affecting the next output based on the previous input.

Sequential logic circuits form the fundament of most digital circuits. For example the finite state machine as used in this assignment. Asynchronous and synchronous sequential logic are the two types of sequential logic circuits.

In synchronous sequential logic circuits the output is formulated based on the input signal with the clock signal. A clock signal is given in the definite time interval. In asynchronous sequential logic circuits the output is generated whenever a change at the input terminal independent of the clock at any time response.

Combinational and Sequential Logic Circuit Comparison.

Specification	Combinational Circuit	Sequential Circuit
Output dependency.	Output depends on present input only.	Output depends on present and past input.
Speed.	Fast.	Slow.
Relative complexity of design in comparison to each other.	Simple.	Greater complexity.
Feedback.	Feedback not needed.	Feedback between input and output.
Time dependency.	Independent	Dependent.
Composition of design.	Logic gates.	Flip-flops.
Uses.	Used for arithmetic and Boolean operations.	Used for storing data.
State memory.	Cannot store any state.	Capability to store any state or to retain earlier state.
Triggering.	No clock present so they don't require triggering.	Clock dependent and need triggering.
Memory element.	No memory element.	Possess a memory element.
Examples.	Encoder, Decoder, Multiplexer, Demultiplexer	Flip-flops, Counters

(Electronics Tutorials, 2019)

Finite-state Machines

Finite-state machines (FSMs) are a device that can only be in one stage of their logic sequence at one time, these are known as a finite states.

An FSM changes states progressively in response to its signal input. An FSM can be simplified into a list of its potential states, the initial state, and the triggering conditions for each transition.

There are two types of FSM, Moore and Mealy.

FSMs of a Moore configuration comprise of states and their transitions. States can produce outputs, and the output is determined solely by the current state, not by any input. However, Mealy machines produce outputs only on transitions and not in states. This often results in state diagrams with fewer states because more logic can be put on transitions. Mealy designs can be adapted to work in Moore designs and vice versa.

Overall FSMs have a low processor overhead and an easy determination of reachability of a state. However, the implementation of huge systems using FSM is hard for managing without any idea of design and the orders of state conversions are inflexible. They are ideal for this assignment as we know exactly how the traffic lights will work.

(I-Programmer, 2018)

Application Specific Integrated Circuits

Application Specific Integrated Circuits (ASIC) are a unique controller chip which serves the single purpose for which it has been specifically designed for and cannot be reprogrammed or altered in any way to perform another function or execute another application it was not initially designed for. ASICs are manufactured to be used for a specific function which would direct how the chip is programmed in the first place considering its permanency. ASICs are abundant in modern electronics such as mobile phones, washing machines, television systems, and are found mostly in single purpose home electronics and handheld devices.

Field Programmable Gate Arrays

Field Programmable Gate Arrays (FPGA) are controller chips that can be programmed and altered to serve various functions simultaneously. The single chip is composed of thousands of units called logic blocks which are linked with programmable interconnects, these are the gate arrays. An FPGA is thus a programmable version of the ASIC controller chip. It has a general functionality that can be programmed to a specific design purpose. Having said that, due to its relative customisability it has several disadvantages such as higher internal delay, higher cost and limited analogue functionality.

(Swindon Silicon Systems, 2019)

Relative merits of FPGAs and ASICs

ASICs are generally less power hungry than FPGAs as they are only concerned with single or limited design purposes on a single chip. Because of the low power consumptions ASICs are normally found in battery powered operations and products. FPGA chips have a complex internal matrix which require a certain amount of comprehension whereas ASIC chips have very simple layouts, easy for reproduction and troubleshooting.

ASICs and FPGAs are normally inversely cost efficient, meaning that ASIC chips are initially expensive to produce but are normally produced in high quantities and sold in high number units offsetting start-up costs. Whereas FPGAs would be vastly inefficient to produce on a large scale due to their bespoke nature but ideal and cost effective for small scale projects and applications.

This means ASICs while they may have a high NRE cost which plays into the sustainability aspect of this technology which will be discussed in more detail now.

(AnySilicon, 2018)

Sustainable Development Using Electronics

Non-Recurring Engineering costs (NRE), refers to the one-time cost investment in the design and development of a system or device. This factor is exacerbated in ASICs due to the complex matrices that must be designed tested and manufactured but per unit they are cheap and mass-produced offsetting this cost. Whereas FPGAs act almost like blank slates and require far less NRE costs due to their intended functionality but would require far more investment overtime adding to the overall budget. Therefore, when it comes down to designs with little variance, such as the traffic light system that will be designed in this assignment, an ASIC chip would be ideal. Ideally the system should be designed and tested in an FSM setup and could then be reproduced en-masse using ASICs.

2.Designing a traffic light control system

5 Second Timer

A five second counter must be designed to function as the wait between the initial activation of the button after the pedestrian has pressed it. In Fig.1 the sequence for this timer can be seen. Using this sequence, the circuit in Fig.2 was designed and then tested in Fig.3. With the logic analyser graph, it can be observed that the timer counts successfully to 5, with this it can now be integrated into the larger circuit.

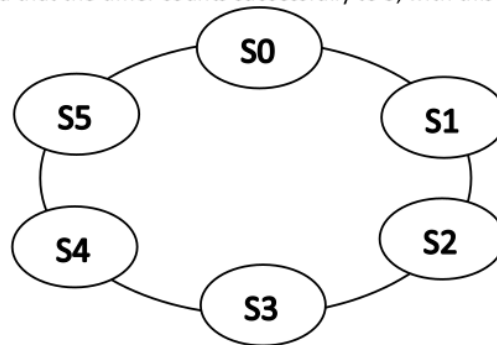


Fig.1 – 5 Sec Counter Sequence

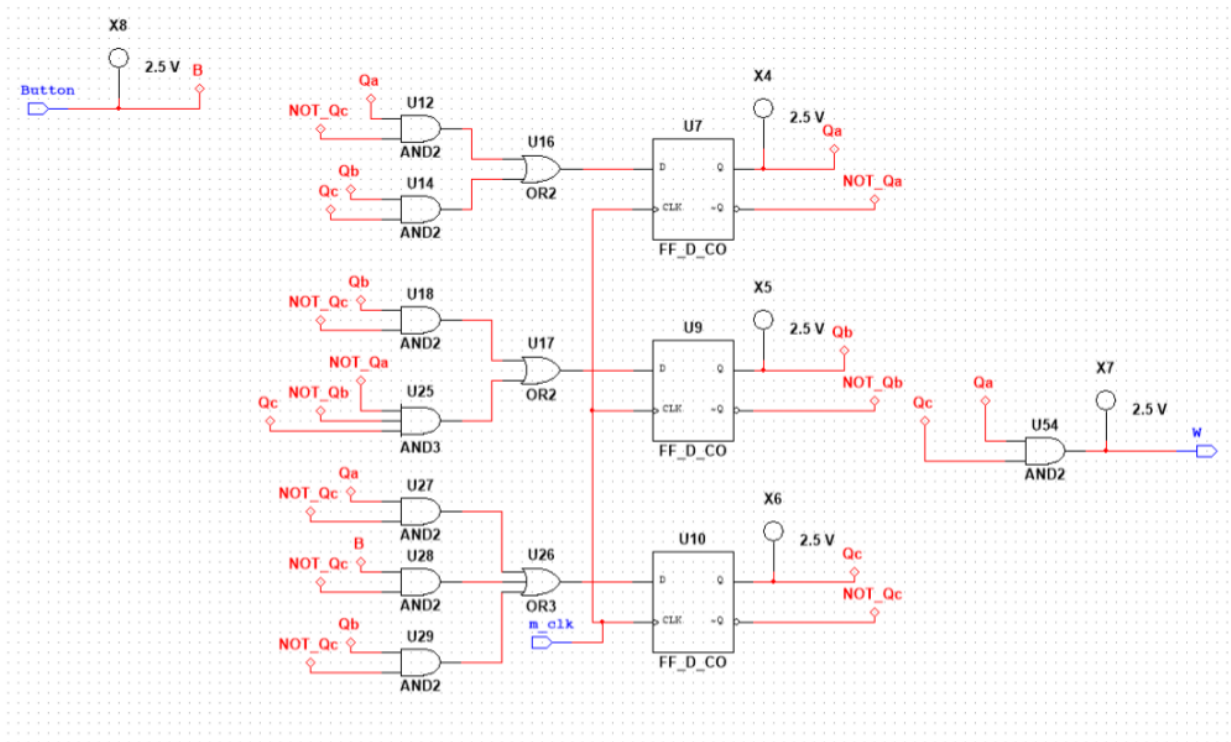


Fig.2 – 5 Sec Counter Circuit

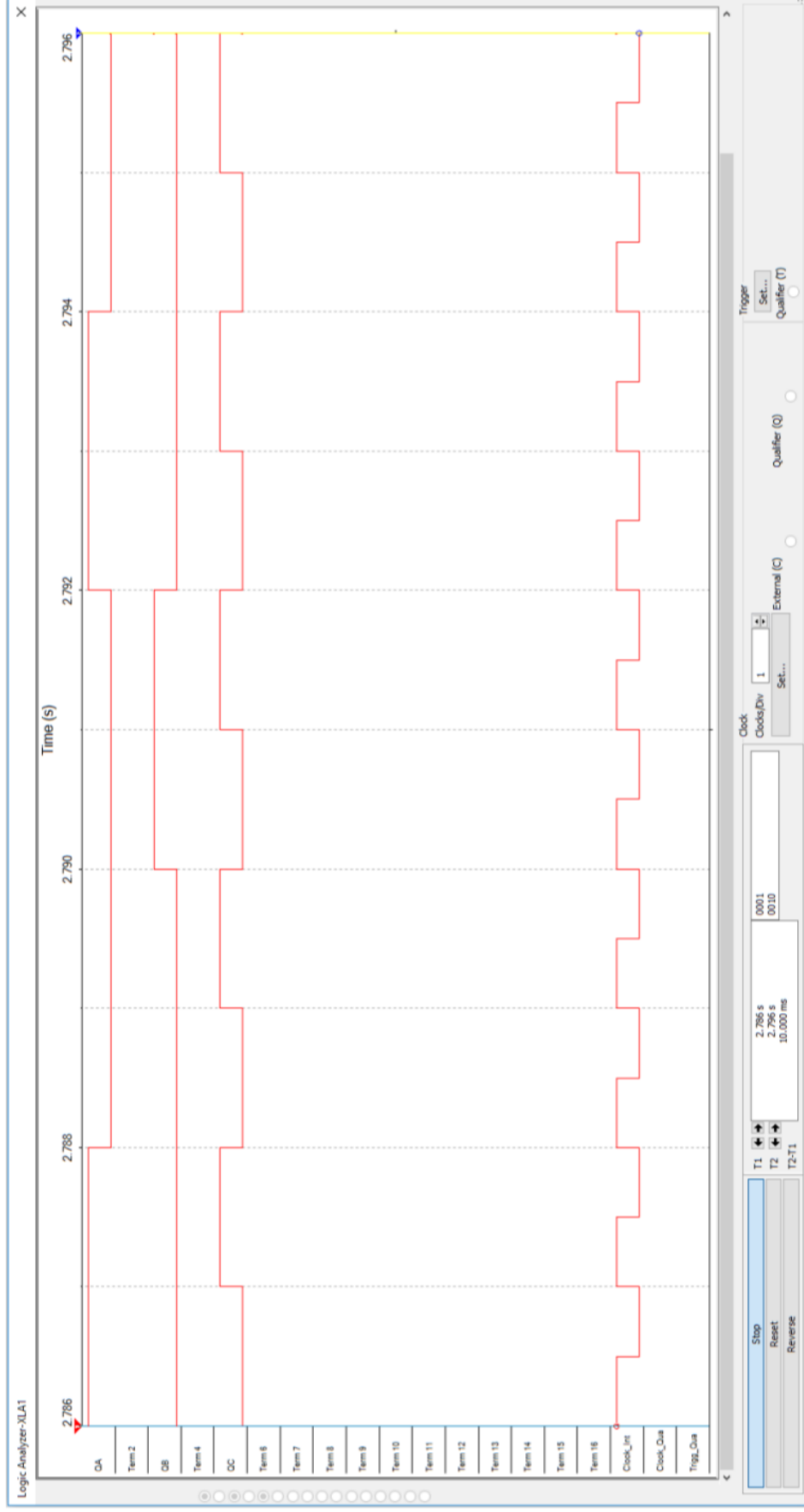


Fig.3 – 5 Sec Counter Circuit Test

15 Second Timer

As seen in Fig.4 the sequence for the 0-15 counter can be seen in full sequence. This counter will be the length of which the red lights stay active for, 15 seconds being ample for the pedestrian. With this sequence the truth table in Fig.5 can be created, then applying Karnaugh maps the tables can be simplified into input equations.

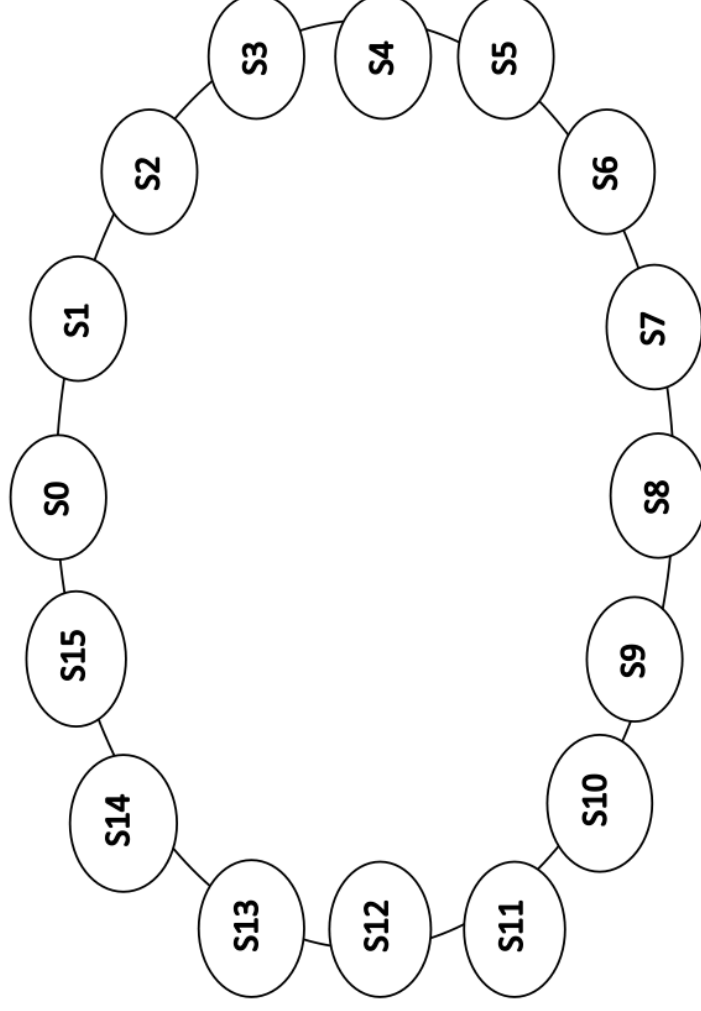


Fig.4 – 15 Sec Counter Sequence

R=0					R=1				
Qa+	0	1	11	10	Qa+	0	1	11	10
0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	1	0	0	1	0
11	1	1	1	1	11	1	1	0	1
10	1	1	1	1	10	1	1	1	1
Qb+	0	1	11	10	Qb+	0	1	11	10
0	0	0	0	0	0	0	0	1	0
1	1	1	1	1	1	1	1	0	1
11	1	1	1	1	11	0	0	1	0
10	0	0	0	0	10	1	1	0	1
Qc+	0	1	11	10	Qc+	0	1	11	10
0	0	0	1	1	0	0	1	0	1
1	0	0	1	1	1	0	1	0	1
11	0	0	1	1	11	0	1	0	1
10	0	0	1	1	10	0	1	0	1
Qd+	0	1	11	10	Qd+	0	1	11	10
0	0	1	1	0	0	1	0	0	1
1	0	1	1	0	1	1	0	0	1
11	0	1	1	0	11	1	0	0	1
10	0	1	1	0	10	1	0	0	1

State	R=0				R=1			
	Qa+	Qb+	Qc+	Qd+	Qa+	Qb+	Qc+	Qd+
0	0	0	0	0	0	0	0	0
1	0	0	0	0	1	0	0	1
2	0	0	0	1	0	0	0	1
3	0	0	0	1	0	0	1	0
4	0	0	1	0	0	0	1	0
5	0	1	0	1	0	1	0	1
6	0	1	1	0	0	0	1	1
7	0	1	1	1	0	1	0	0
8	1	0	0	0	1	0	0	0
9	1	0	0	0	1	1	0	1
10	1	0	0	1	0	1	0	1
11	1	0	0	1	1	1	1	0
12	1	1	1	0	1	1	1	0
13	1	1	1	0	1	1	1	1
14	1	1	1	1	1	1	1	1
15	1	1	1	1	1	0	0	0

$$Qa = A\bar{B} + A\bar{C} + A\bar{D} + \bar{A}BCD$$

$$Qb = B\bar{C} + B\bar{D} + \bar{B}CD$$

$$Qc = \bar{C}D + C\bar{D}$$

$$Qd = R\bar{D} + C\bar{D} + B\bar{D} + A\bar{D}$$

Fig.5 – 15 Sec Counter Truth Table/Karnaugh Maps

From Fig.5 the Multisim circuit can be created as seen in Fig.6. The circuit was tested using coloured probes and then thoroughly tested using the logic analyser in Fig.7. From the testing graph we can observe the counting stages from 0 to 15. Knowing that this counter also works as intended it can now be integrated with the RAG controller and the 5 second timer.

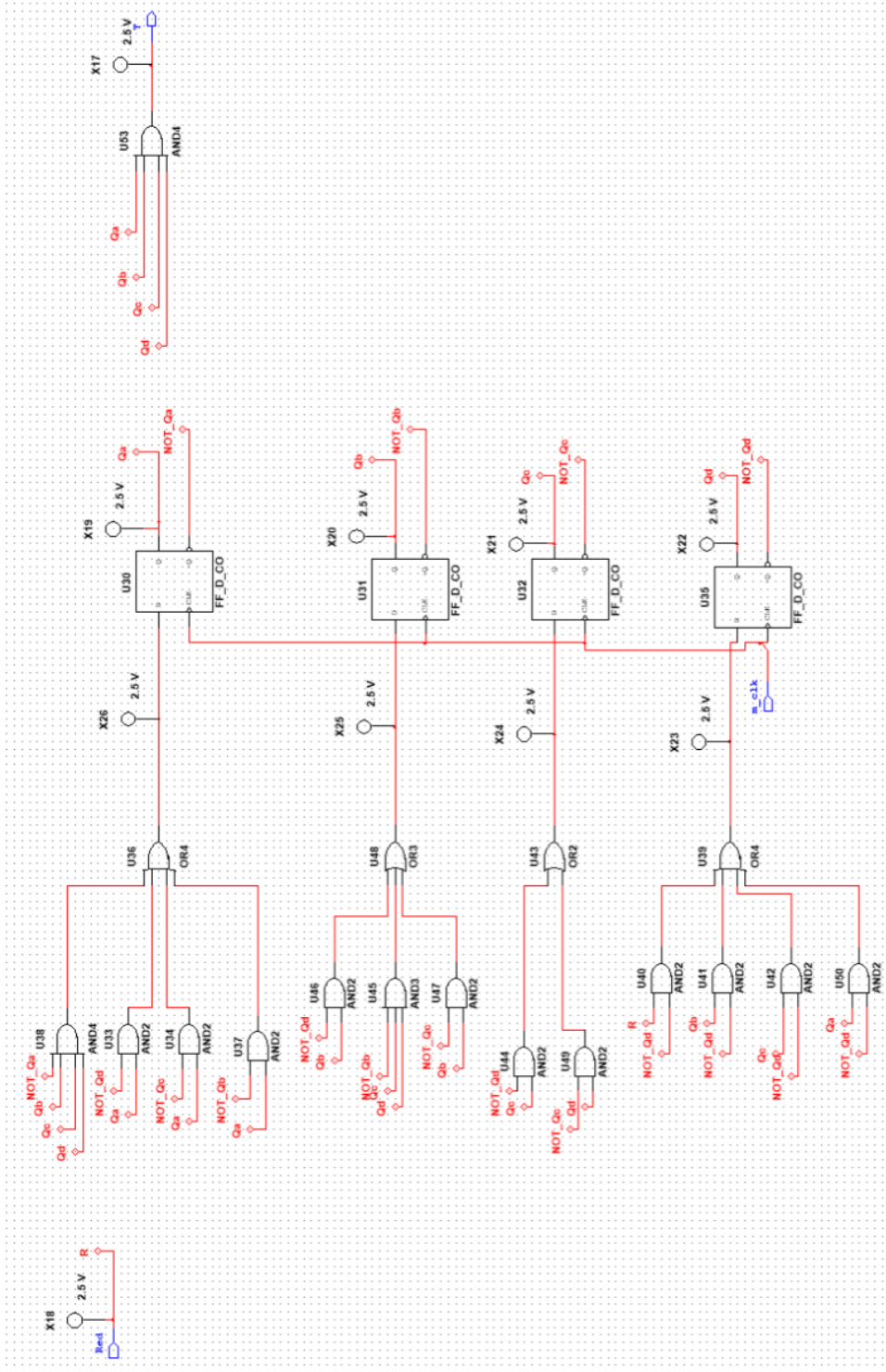


Fig.6 – 15 Sec Counter Circuit

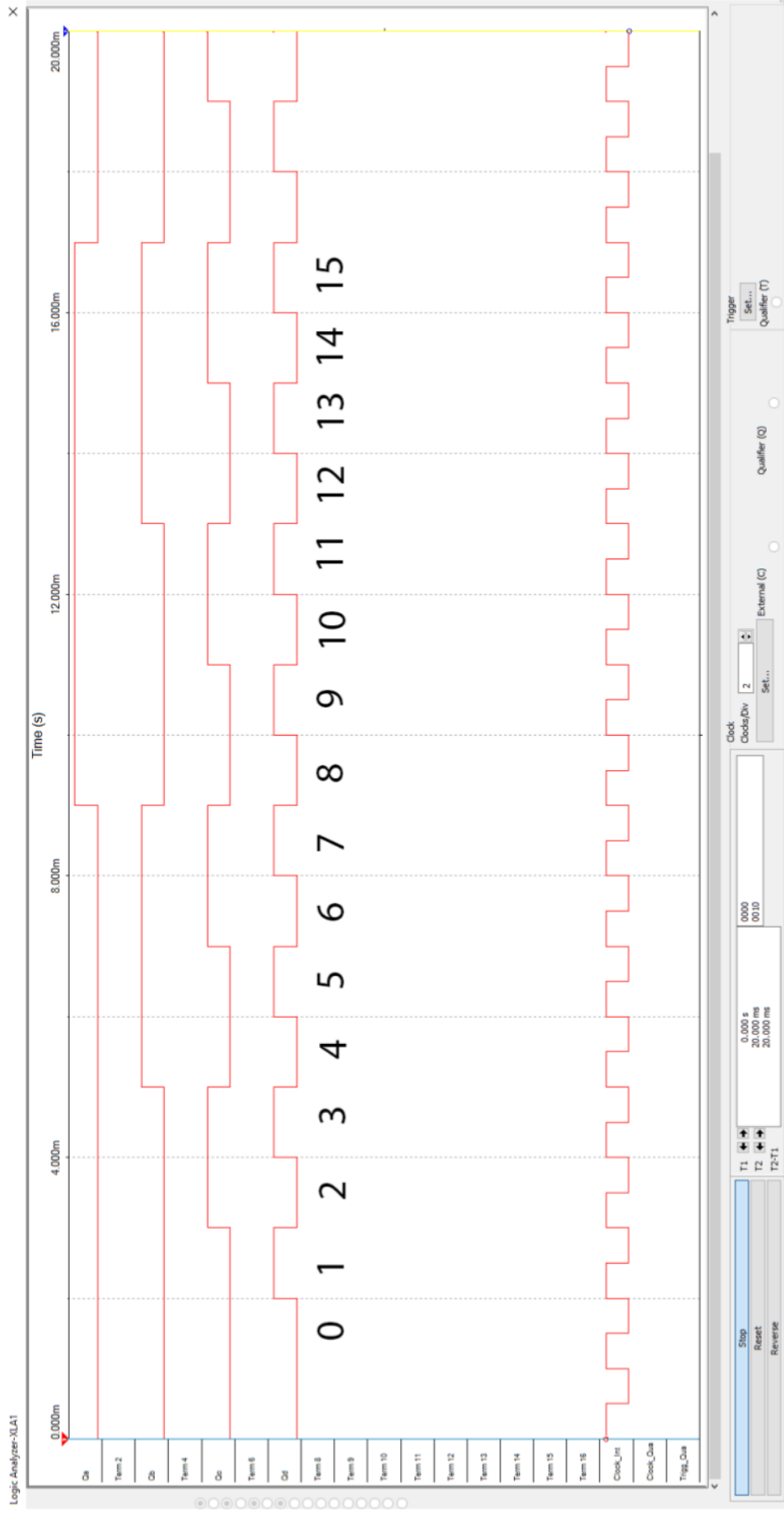


Fig.7 – 15 Sec Counter Circuit Test

RAG Controller

Finally, the RAG controller must be designed to allow the circuit to mesh bot circuits together to allow the lights to trigger in the correct order for the assigned amount of time. In Fig.8 the truth table for the different states before and after the button is pressed, then in Fig.9 the specific inputs fir the red amber and green light inputs can be seen which will turn on in sequence after the button is pressed. These Karnaugh maps can be used to make the RAG circuit as seen in Fig.10.

										NEXT									
NEXT					Current			W=0						W=1					
W=0		W=1			Qa	Qb	Qc	T=0			T=1			T=0			T=1		
State	T=0	T=1	T=0	T=1				Qa+	Qb+	Qc+	Qa+	Qb+	Qc+	Qa+	Qb+	Qc+	Qa+	Qb+	Qc+
S0	S0	S0	S1	S1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1
S1	S2	S2	S2	S2	0	0	1	0	1	0	0	1	0	0	1	0	0	1	0
S2	S3	S3	S3	S3	0	1	0	0	1	1	0	1	1	0	1	1	0	1	1
S3	S3	S4	S3	S4	0	1	1	0	1	1	1	0	0	0	1	1	1	0	0
S4	S5	S5	S5	S5	1	0	0	1	0	1	1	0	1	1	0	1	1	0	1
S5	S0	S0	S0	S0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
S6	X	X	X	X	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X
S7	X	X	X	X	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X

W=0					W=1				
T Qa/Qb Qc	0	1	11	10	T Qa/Qb Qc	0	1	11	10
0	0	0	0	0	0	0	0	0	0
1	1	0	x	x	1	1	0	x	x
11	1	0	x	x	11	1	0	x	x
10	0	0	1	0	10	0	0	1	0
T Qa/Qb Qc	0	1	11	10	T Qa/Qb Qc	0	1	11	10
0	0	1	1	1	0	0	1	1	1
1	0	0	x	x	1	0	0	x	x
11	0	0	x	x	11	0	0	x	x
10	0	1	0	1	10	0	1	0	1
T Qa/Qb Qc	0	1	11	10	T Qa/Qb Qc	0	1	11	10
0	0	0	1	1	0	1	0	1	1
1	1	0	x	x	1	1	0	x	x
11	1	0	x	x	11	1	0	x	x
10	0	0	0	1	10	1	0	0	1

$$Qa = A\bar{C} + TBC$$

$$Qb = B\bar{C} + \bar{T}B + \bar{A}\bar{B}C$$

$$Qc = A\bar{C} + \bar{T}B + B\bar{C} + W\bar{C}$$

Fig.8 – RAG Controller Input State Truth Table

State	Qa	Qb	Qc	R	A	G
S0	0	0	0	0	0	1
S1	0	0	1	0	1	0
S2	0	1	0	0	1	0
S3	0	1	1	1	0	0
S4	1	0	0	1	1	0
S5	1	0	1	1	1	0

Qa/Qb Qc	0	1	11	10
0	0	0	1	0
1	1	1	x	x
Qa/Qb Qc	0	1	11	10
0	0	1	0	1
1	1	1	x	x
Qa/Qb Qc	0	1	11	10
0	1	0	0	0
1	0	0	x	x

$$R = Qa + QbQc$$

$$A = Qa + \overline{Qb}Qc + Qb\overline{Qc}$$

$$G = \overline{Qa}\overline{Qb}\overline{Qc}$$

Fig.9 – RAG Controller Colour Input Truth Table

Traffic Lights Complete Circuit

Using the sub circuit functionality on Multisim, the 5 sec timer, 15 sec timer and the RAG controller have been simplified in the shorthand version seen in Fig.11. The B input acts as the pressed button activated by the pedestrian at the traffic light junction. After the button is pressed the first timer counts 5 seconds and the lights go from green to amber and then to red. The lights will remain on the red output for 15 seconds then the lights will change to red and amber on at the same time then to green resting until the button is pressed again. Looking at Fig.12, the logic analyser graph for this circuit can be seen, the input is kept as logic one and the full 20 second sequence can be seen graphically.

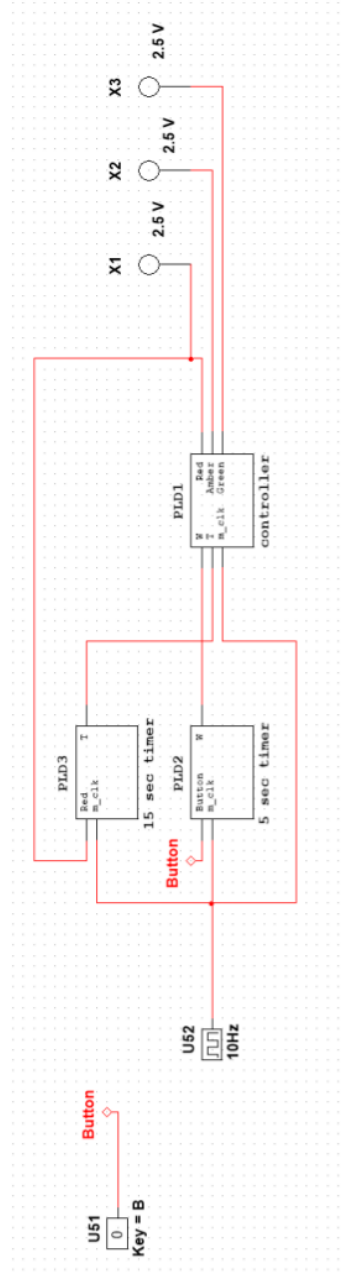


Fig.11 – Traffic Light Complete Circuit

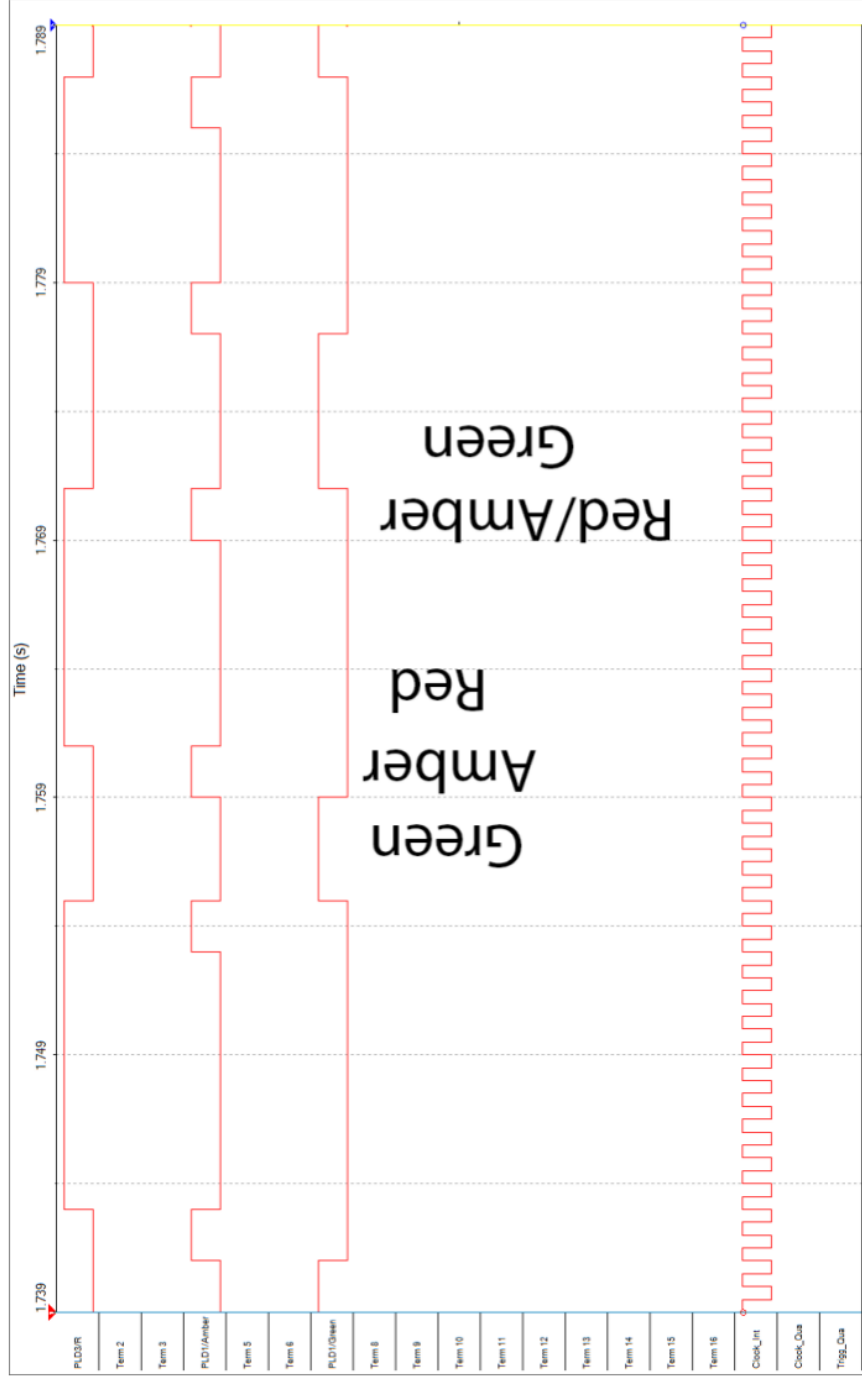


Fig.12 – Traffic Light Complete Circuit Test

3.Modifying and improving the design

To improve upon the efficiency of the circuit a pressure plate could be added to the input, to prevent troublesome pedestrians from pressing the button and starting the sequence without a need for the full sequence run. To achieve this a pressure plate input would have to added to the 5 second timer circuit. For example, the sequence could be programmed in such a way that when the button is pressed the pressure plate must also read as a logic high for the duration of the 5 second time delay until the 15 second sequence kicks in. Meaning for the sequence to be started the pedestrian must be on the crossing for the 5 seconds, however if the plate reads a logic low the sequence can then reset to stage 0.

4.Conclusion

In conclusion the designed and implemented solution successfully satisfied the outlined specification, in that the system successfully worked at all stages, this can be proven by the various tests carried out through the design implementation. Relating to the theoretical knowledge garnered from the research task as predicted using the chosen FSM solution worked adequately.

The improved design was not fully explored and explained, in the future this would be an ideal place to start improving the design, in its current state it is functional but not fully efficient, this tweak would increase the efficiency of the system.

Furthermore, as discussed in the research task the NRE cost for an initial system such as this would be high, especially if it was designed in detail on an ASIC chip. However, in terms of long term sustainability and overall cost drivers a system like this would be ideally mass produced on ASIC ships and installed on traffic light systems en-masse.

Citation List

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FINAL GRADE

GENERAL COMMENTS

Instructor

50/100

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GRADING FORM: CSG-RUBIC

IWAN COSTELLODOWNS**50****RESEARCH-INFORMED LITERATURE**



There was very good evidence of further reading and research from credible and reliable sources. Your interpretation and understanding of the additional research was good and demonstrated a very good underlying appreciation of the subject. Your references were appropriate to the task and applied with few errors or inconsistencies. Your reference list was of an appropriate length for this assignment.

7**KNOWLEDGE AND UNDERSTANDING**



The knowledge and understanding of the subject demonstrated by this assignment was reasonably detailed and mainly accurate. There were very few gaps in your knowledge of the basic concepts and your understanding of the higher level concepts was demonstrated to a limited degree - you could have

15

explained in more detail how the circuit evolved.
Further work – Your explanations need to be more detailed and written with a greater emphasis on critical evaluation rather than description.

ANALYSIS



Your analysis of the task was generally satisfactory, both in class and as shown in this assignment, however it did tend more towards descriptive rather than analytical. You have demonstrated some analytical skills and your approach to the task was logical. You wrote a short conclusion that demonstrated some skills in analysing quantitative and qualitative data, however this was generally basic in nature. Further work – in your conclusion, you should relate the results to the original specification and to accepted theory and provide a detailed critical analysis of this.

11

PRACTICAL APPLICATION AND DEP.



Your application of practical skills for this task was generally good. You used the resources available appropriately when designing the circuit and you used appropriate options for testing and evaluating the circuit performance. You managed to design an efficient circuit that functioned within the specification and achieved this by only asking for assistance when appropriate. Your results were comprehensive and allowed for a good conclusion to be attempted.

12

SKILLS FOR PROFESSIONAL PRAC.



Your written report was reasonably well presented in terms of content and layout and was mostly structured in a coherent way, however you should endeavour to use the available word count more effectively in future.

5