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Examination Answer Books

12 Pages

Complete, fold and seal
(see note 2 below)

SURNAME: GANNI

FORENAME(S): AMINA

Instructions to Candidates

1. Please give the information requested in the boxes below.
2. Enter your name in the space provided to the right, fold over and seal down (using the label provided) to hide your name.
3. The answers must be legibly written. The Examiners can either ignore illegible or have it typed and the expense of typing charged to the candidate.
4. Write your answers in ink.
5. Begin each answer on a fresh page. Do all rough work in the answer book and cross it through.
6. No part of this book is to be torn out; it must be handed in complete.
7. If more books than one are used, fasten them together using the tags available from the invigilator(s).
8. Every book must be handed in. In no circumstances may answer books, used or unused, be taken out of the examination venue.

1	Student Number	2319000
2	Title of Examination Paper	MICROS PERIPHERALS AND INTERFACES
3	Module Code	ACDA4004
4	Date and Time of Examination	08.01.25
5	Examination Venue	10307
6	Seat Number	—
7	Number of Answer Books handed in	

List the numbers of the questions you have attempted	Office Use
1	6
2	2
3	1 1/2
4	2
5	10
6	2
	23 1/2
	+2
Total	47 1/2

6.
2
1 1/2
2
10
2
23 1/2

1

a. RETURN - End of Subroutine, goes back to the top

b. SLEEP - cause a time delay

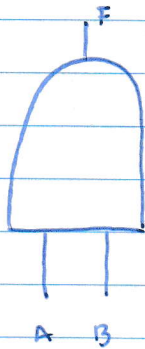
c. ADDLW - Add literal to W, add a literal value to W register.

d. BCF F, b - Bit clear file, sets the specific file to zero then sets the value.

e. DECF - decrement to file, decrement 1 from file

2. Schmitt trigger or a resistor-capacitor circuit acting as a low pass filter

3.

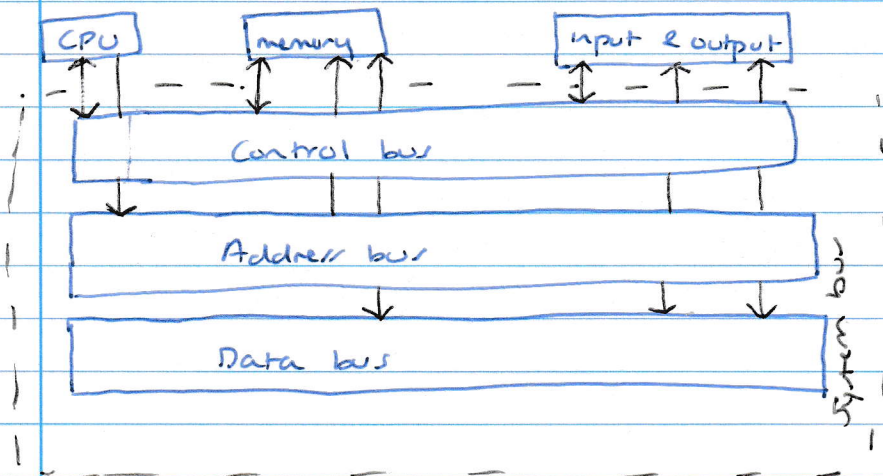


$$F = A \cdot B$$

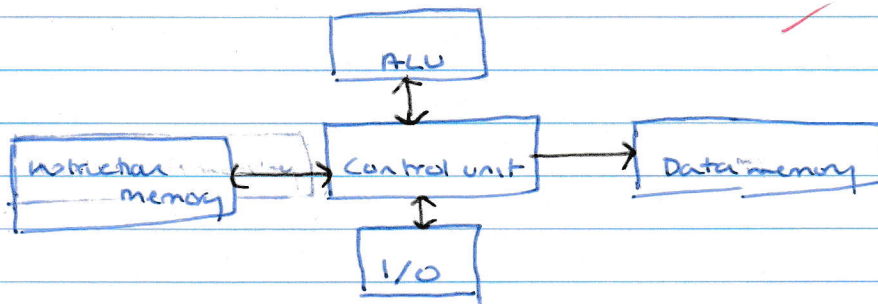
Truth table

A	B	F
0	0	0
1	0	0
0	1	0
1	1	1

5. Von Neumann



Harvard



Von Neumann architecture uses a more each design approach & is easier to implement due to its more simple nature of carrying out one instruction per clock cycle, and it shares the data bus & address bus. Due to ~~the~~ this simpler design it is cheaper & more cost effective compared to the Harvard architecture. of using However, the advantage the Harvard architecture over the von Neumann proves handy for more complicated systems such as embedded systems whereby multiple instructions are carried out per clock cycle thus making it more efficient in more instances.

Simple

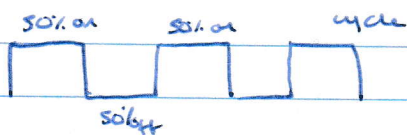
6.

DAC

Pulse width modulation is a technique whereby the digital ^{duration} ~~data~~ (width) of a digital pulse is manipulated. This is done by either frequency ^{switching} ~~switching~~ or duty cycle. ✓

Frequency switching is dependent on the load of device. Whereas on-off duty cycle depends on the duration of on & off cycle.

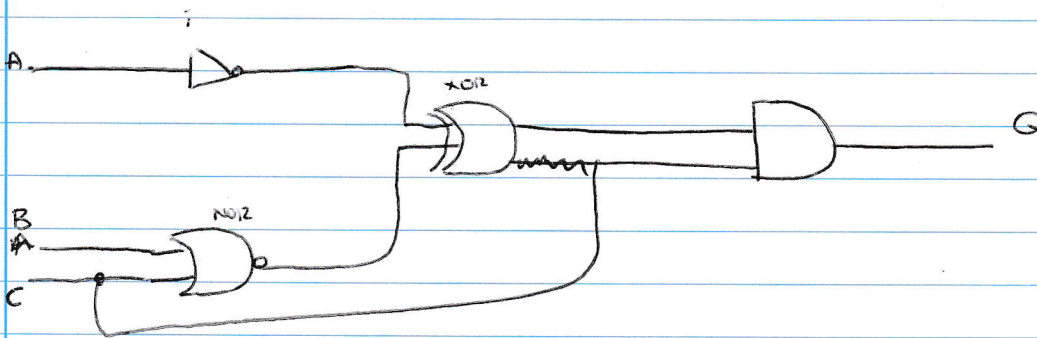
time-ramp



By using a rise delay ^{using} ~~using~~ on the clock to set the input for a certain amount of time

The digital analogue converter reads the voltage input, and the comparator compares the voltage with the V_{REF} . [×] or the clock is set bit by bit depending on the voltage input; this is set to either 0 or 1, if the V_{in} is higher than V_{REF} or 0 if it's lower. This causes an on & off cycle caused by the resetting of the clock.

4.



Inputs

A	B	C	D NOT A	E NOR B/C	F XOR D/E	Q and F & C
0	0	0	1	1	0	0
0	1	0	1	0	1	0
0	0	1	1	0	1	1
1	0	0	0	1	1	0
0	1	1	1	0	1	1
1	1	0	0	1	1	0
1	0	1	0	0	0	0
1	1	1	0	0	0	1

NOR

Truth table

A	B	F
0	0	1
0	1	0
1	0	0
1	1	1

OR

Truth table

A	B	F
0	0	0
0	1	1
1	0	1
1	1	0

XOR

Truth table

A	B	F
0	0	0
1	0	1
0	1	1
1	1	0

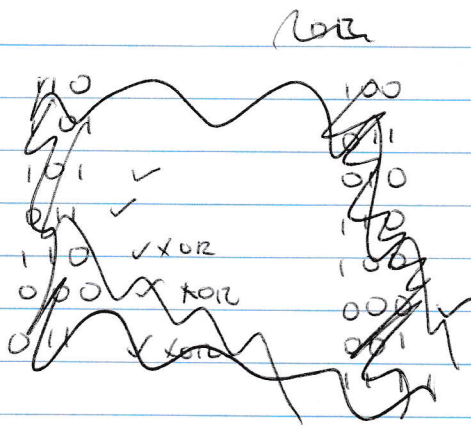
Inputs

A	B	C	D NOT A	E NOR B/C	F XOR D/E	Q and F & C
0	0	0	1	1	0	0
0	0	1	1	0	1	1
0	1	0	1	0	1	0
1	0	0	0	1	1	0
0	1	1	1	0	0	0
1	0	1	0	0	0	0
1	1	0	0	0	0	1
1	1	1	0	0	1	1

2 / 2

b.

XNOR XOR



2.

By adding a resistor-capacitor as a low-pass filter & then implementing a schmitt trigger