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Electrical and Electronic Principles

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Different types of transistor amplifiers

There are two main types of transistor amplifiers. They are bipolar junction transistors (BJT), and field effect transistors (FET). Both transistors are capable of voltage, current and power gain. Although they both have three terminals, they are not identified using the same names. The BJT will have a base, collector and emitter, whereas a FET will have source, drain and gate terminals. According to (Garg, et al., 2008, p. 394) the main differences between the BJT and FET transistors are that “the former is a current-controlled device and the latter is a voltage-controlled device.”

Bipolar Junction Transistors

Both transistors come in different configurations. The BJT transistors can be used as an NPN variant or PNP variant. These are semi-conductor devices, usually formed using silicon or germanium. The difference between the NPN and PNP is the formation of the junctions. An NPN transistor will have a surplus of electrons and a PNP transistor will have a surplus of ‘holes.’ As shown below, (Fig 1.) the NPN transistor will have a P-type semi-conductor between two N-type semi-conductors. The PNP transistor has an N-type semi-conductor between two P-type semi-conductors. The configuration of the transistors is achieved by doping. An NPN transistor “comprises two semiconductor junctions that share a thin p-doped anode region” (Aluf, 2017, p. 775), whereas a PNP transistor “comprises two semiconductor junctions that share a thin n-doped cathode region.” (Aluf, 2017, p. 775)

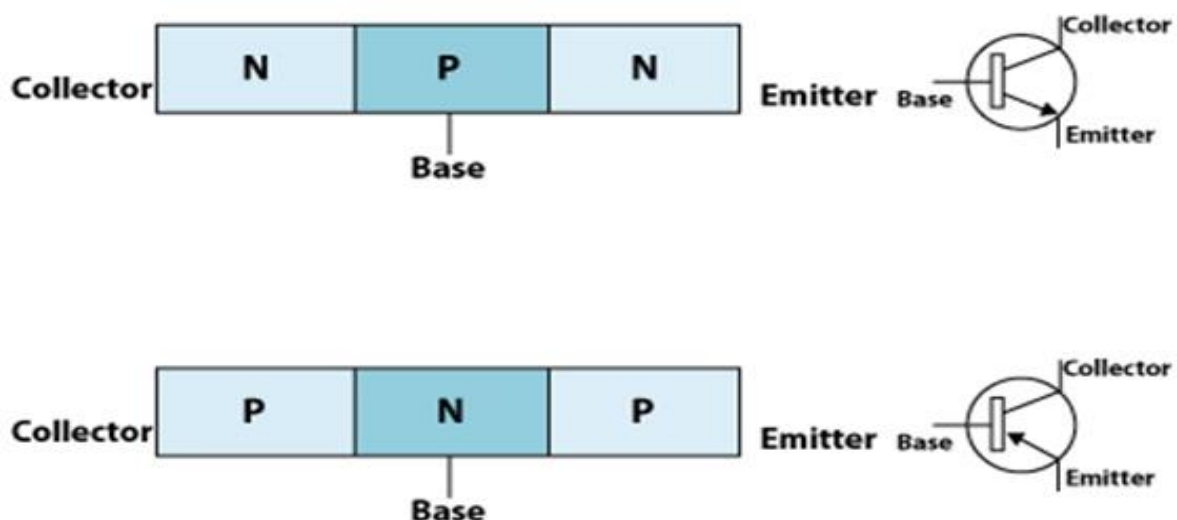


Fig 1. Difference between NPN and PNP junctions (Elprocus, 2020)

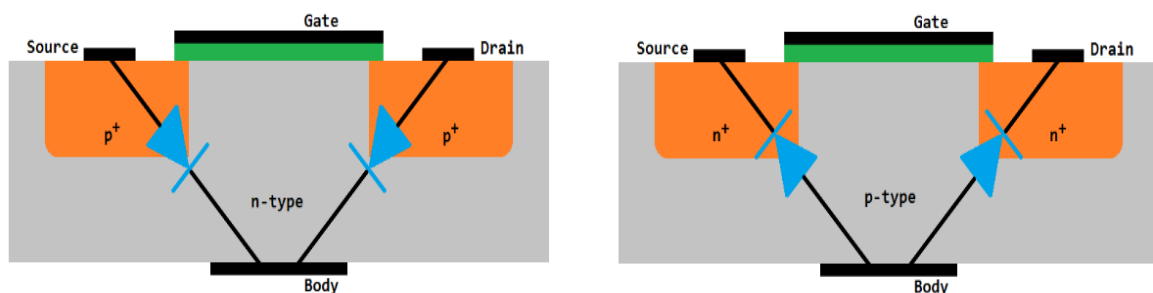
They can be put into a circuit in three different configurations. Common base, common emitter and common collector. The gain of current, voltage and power will vary depending which way you put them in to the circuit. Below is a table displaying the gains.

Configuration	Voltage gain	Current gain	Power gain
Common emitter	Medium	Medium	Very High
Common base	High	Low	Low
Common collector	Low	High	Medium

Field Effect Transistors

FET transistors also come in two main configurations. They are P-FET and N-FET. As mentioned, FET transistors also have 3 terminals; Gate, source and drain. The transistor is formed through a uni junction as opposed to the bipolar junction of the BJT transistors, and is a voltage controlled device not a current controlled device. FET's have a lower noise output, which according to (Schuler, 2019, p. 198) "makes them useful as pre amplifiers when noise must be very low because of high gain in the following stages." Whether the transistor is N-FET or P-FET is determined by the material that connects the source channel to the drain. As (Cox, 2002) states, when the "channel is made of P-type material, the device is a P-channel JFET." This is then the exact opposite for the N-FET types, as shown in Fig 2 below.

Fig 2. Difference between P-FET and N-FET transistors (Schmidt, 2018)



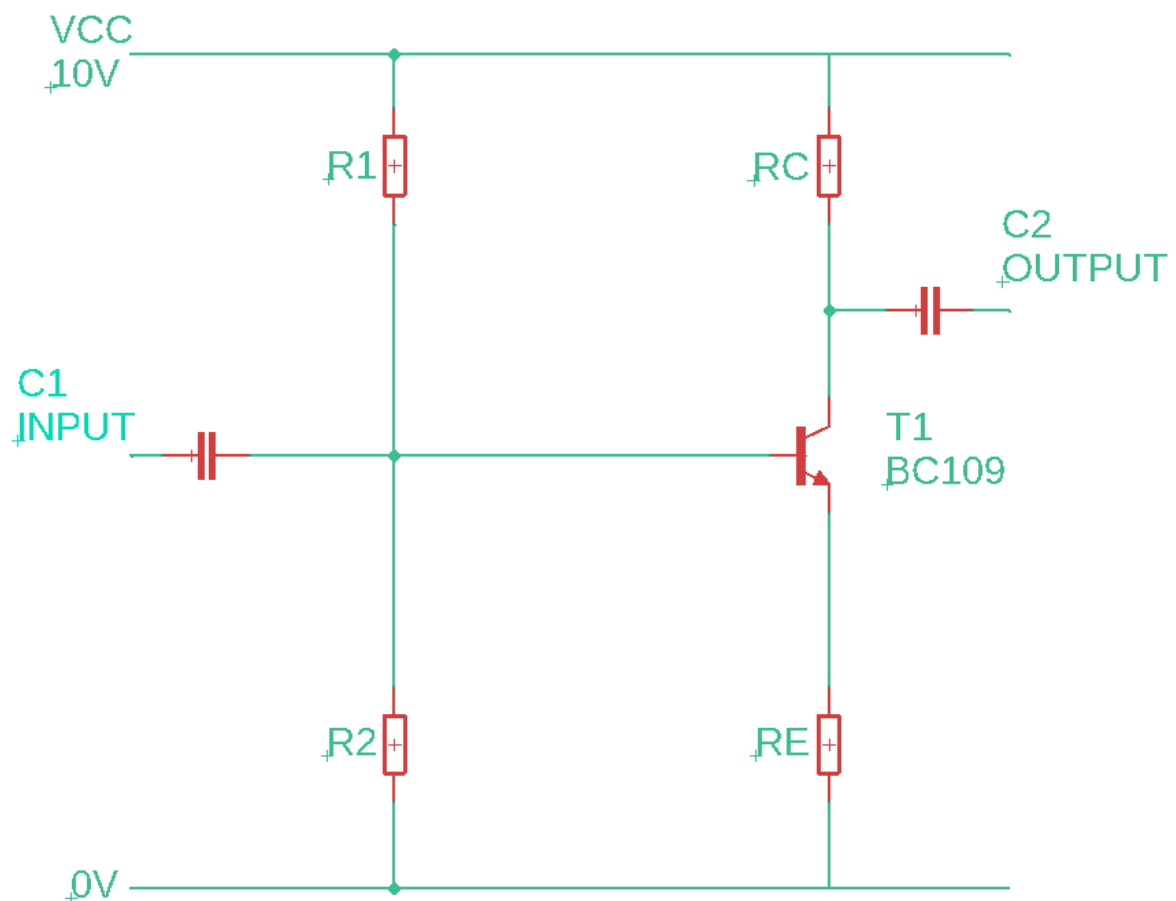
Like the BJT transistor, the configuration of the way the transistor is put into circuit will affect the current, voltage and power gains. The configurations available are common source, common gate and common drain. The gains are indicated in the table below.

Configuration	Voltage gain	Current gain	Power gain
Common source	Medium	Very High	Very High
Common drain	Unity	Very High	Very High
Common gate	High	Unity	High

Unity simply means that the input and output signals are in phase.

Circuit design

As part of the assignment we were given pre-set values for VCC and gain, and asked to show all the workings for the below circuit. The values I were give were; VCC – 10, and Gain of 10.



We assume that the voltage at RC is approximately half of the VCC. This will give us 5V at RC which we will call VC. We also can assume that IC is 2mA. I have chosen this value as 2mA is the operating current at IC to produce a minimum gain (hFE) of 200 in the transistor according to our datasheet (MultiComp, 2006). Now that we know the values of VC and IC, we can calculate the value of RC using Ohms law.

Calculations

$$RC = VC/IC, \quad RC = 5V/2mA, \quad RC = 2.5K\Omega$$

For RE, we are going to divide RC by the Gain. So, $RE = 2.5K\Omega/10$, $RE = 250\Omega$.

This is not the true value, however. To find the true value of RE, we need to use the formula $Gain = \frac{RC}{(RE+Re)}$, Where RC is $2.5K\Omega$, RE is 250Ω and Re is 12.5Ω .

We know Re is 12.5Ω as we get this from the internal voltage drop of the transistor (25mv), divided by the current at the collector (2mA). From this we can deduce that the true gain of the circuit is approximately 9.43.

From this we can rearrange the formula to show the real value for RE. This is shown below: $RE = \frac{RC}{Gain} - Re$. $RE = \frac{2500}{10} - 12.5$ $RE = 235\Omega$

The voltage at the emitter (VE) is $\frac{VC}{Gain}$, $\frac{5V}{10}$ so, VE is 0.5v

The current at the emitter (IE) is approximately the same as IC, so 2mA.

The current at the base of the transistor (Ib) is $\frac{IC}{hFE}$, $\frac{2mA}{200} = 10\mu A$.

The voltage at the base of the transistor (Vb) is $VE + 0.7v = 1.2v$ We use the value 0.7v as this is minimum operating voltage of the transistor (datasheet).

The current at R1 (IR1) is approximately 11 times bigger than Ib. So, $11 \times 10\mu A = 110\mu A$

The current at R2 (IR2) is approximately 10 times bigger than Ib. So, $10 \times 10\mu A = 100\mu A$

The voltage at R1 (VR1) is $VCC - Vb$. So, $VR1 = 8.8v$

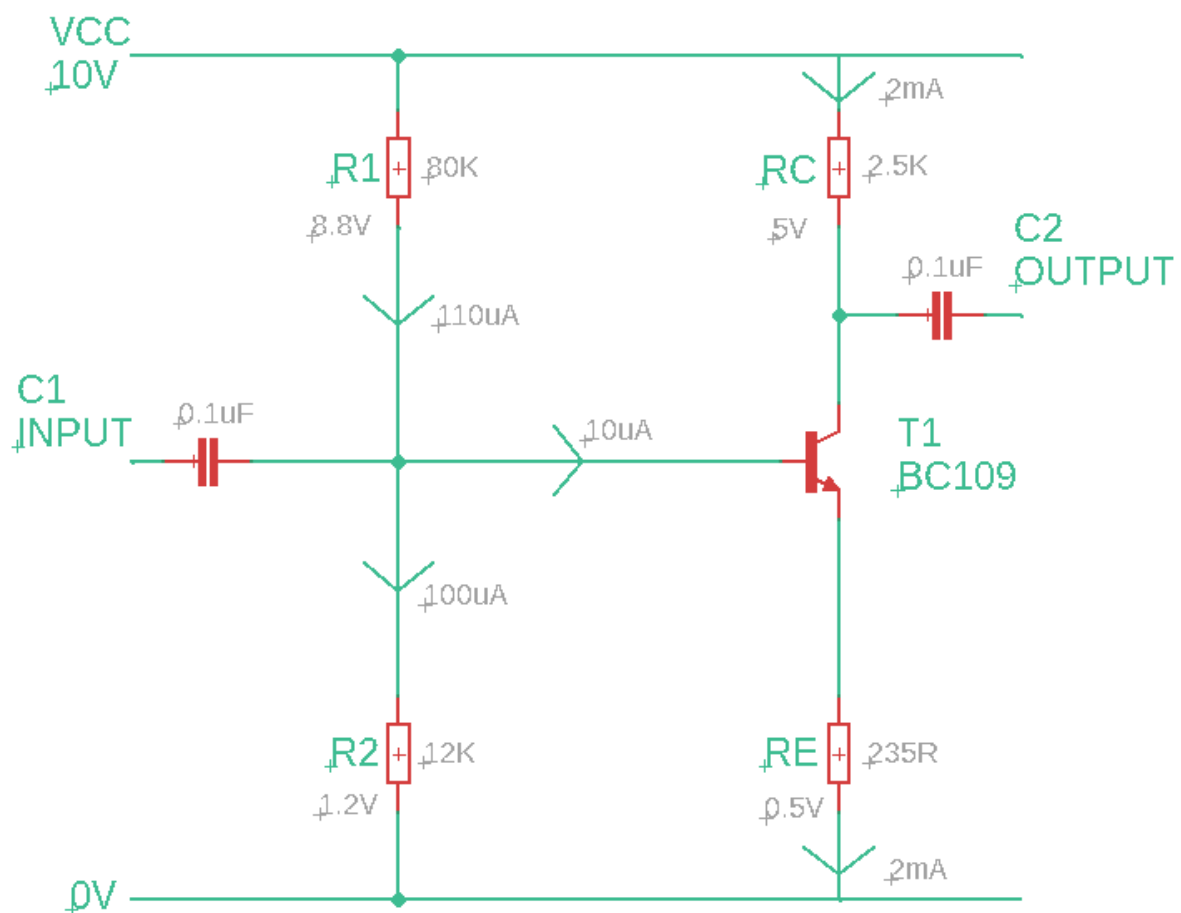
The voltage at R2 (VR2) is equal to Vb, so 1.2v.

The value of R1 is $\frac{VR1}{IR1} = 80K\Omega$

The value of R2 is $\frac{VR2}{IR2} = 12K\Omega$

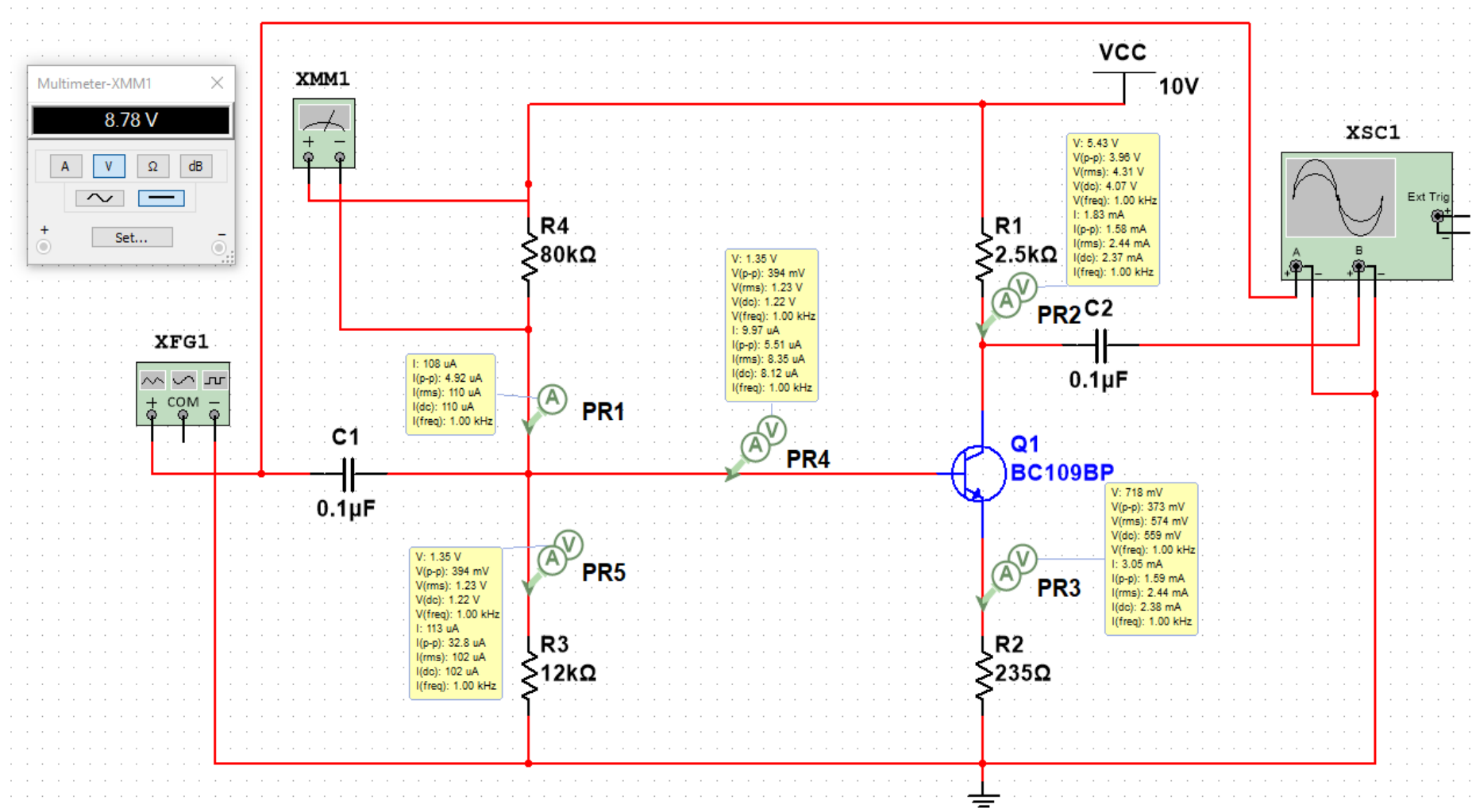
We can assume the values of C1 and C2 to be 0.1μF.

Below is the finished circuit with all declared values and assumptions.



Multisim Build

Below is the finished circuit simulating in Multisim



Below are closer screenshots of the probes and the multimeter used in the simulation to determine the voltage and current readings at each point.

PR1

I: 108 μ A
I(p-p): 4.92 μ A
I(rms): 110 μ A
I(dc): 110 μ A
I(freq): 1.00 kHz

PR2

V: 5.43 V
V(p-p): 3.96 V
V(rms): 4.31 V
V(dc): 4.07 V
V(freq): 1.00 kHz
I: 1.83 mA
I(p-p): 1.58 mA
I(rms): 2.44 mA
I(dc): 2.37 mA
I(freq): 1.00 kHz

PR3

V: 718 mV
V(p-p): 373 mV
V(rms): 574 mV
V(dc): 559 mV
V(freq): 1.00 kHz
I: 3.05 mA
I(p-p): 1.59 mA
I(rms): 2.44 mA
I(dc): 2.38 mA
I(freq): 1.00 kHz

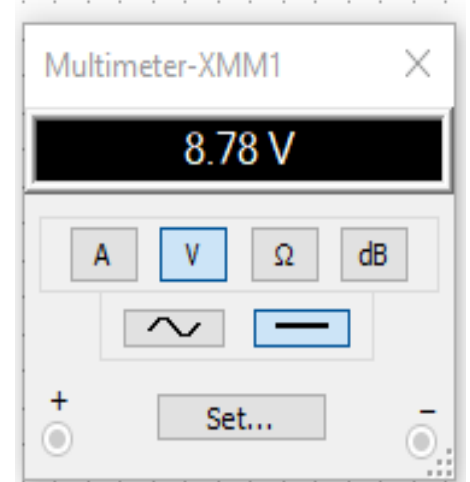
PR4

V: 1.35 V
V(p-p): 394 mV
V(rms): 1.23 V
V(dc): 1.22 V
V(freq): 1.00 kHz
I: 9.97 μ A
I(p-p): 5.51 μ A
I(rms): 8.35 μ A
I(dc): 8.12 μ A
I(freq): 1.00 kHz

PR5

V: 1.35 V
V(p-p): 394 mV
V(rms): 1.23 V
V(dc): 1.22 V
V(freq): 1.00 kHz
I: 113 μ A
I(p-p): 32.8 μ A
I(rms): 102 μ A
I(dc): 102 μ A
I(freq): 1.00 kHz

XMM1



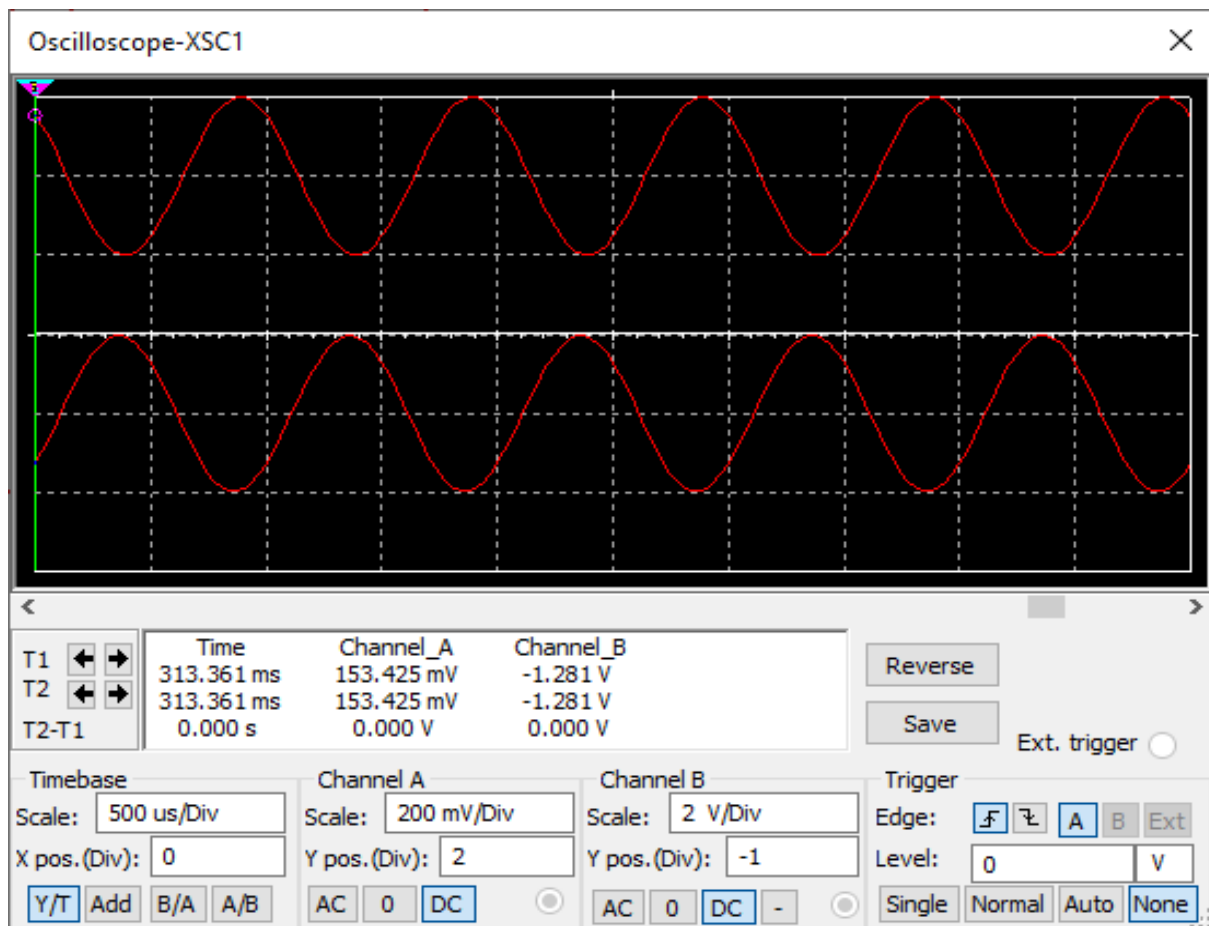
Comparisons and analysis

The comparisons are very similar between the circuit I have designed and the circuit I have simulated in multisim. Below is a comparison table deduced from the two circuits.

Measured Point	Designed circuit expected measurement	Multisim circuit measurement
IC	2mA	2.37mA
VC	5V	4.07V
IE	2mA	2.37mA
VE	500mV	559mV
Ib	10 μ A	8.12 μ A
IR1	110 μ A	110 μ A
VR1	8.8V	8.78V
IR2	100 μ A	102 μ A
VR2	1.2V	1.22V

There are very slight differences. This could be due to the fact that to start the calculations for the expected design, we had to assume the current IC and the voltage VC, therefore having a knock-on effect. However, from looking at the table the measurements are very close.

We can also see from the screenshot on the next page of the oscilloscope used in multisim (XSC1) that we have achieved the overall gain of 10 that we were aiming for.



We can clearly analyse from the screenshot, that the top waveform measured at the input is 400mV peak to peak, and the second waveform measured at the output is 4V peak to peak. This is an exact gain of 10. We can also distinguish that the output waveform is 180 degree out of phase compared to the input.

Input and output impedance

The task brief says that at the output of our amplifier, a piece of audio equipment will be connected with an impedance of 600Ω . Normally we would impedance match this to R_C , but for the purpose of this calculation we will keep R_C at $2.5K\Omega$. To prove our output impedance is correct at $2.5K\Omega$, we have to use the following formula to find the h_{ie} .

$$h_{ie} = \frac{h_{FE}}{40I_{CQ}} = \frac{200 \text{ assumed}}{40 \times 2\text{mA}} = \frac{200}{0.08} = 2.5K\Omega$$

where, h_{FE} is the gain of the transistor, and $40I_{CQ}$ is a constant multiple of the current at the collector

Now that we have proved that h_{ie} matches the output impedance, we can calculate the input impedance using the formula below.

$$\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_C} = \frac{1}{80K\Omega} + \frac{1}{12K\Omega} + \frac{1}{2.5K\Omega} = 2.02K\Omega$$

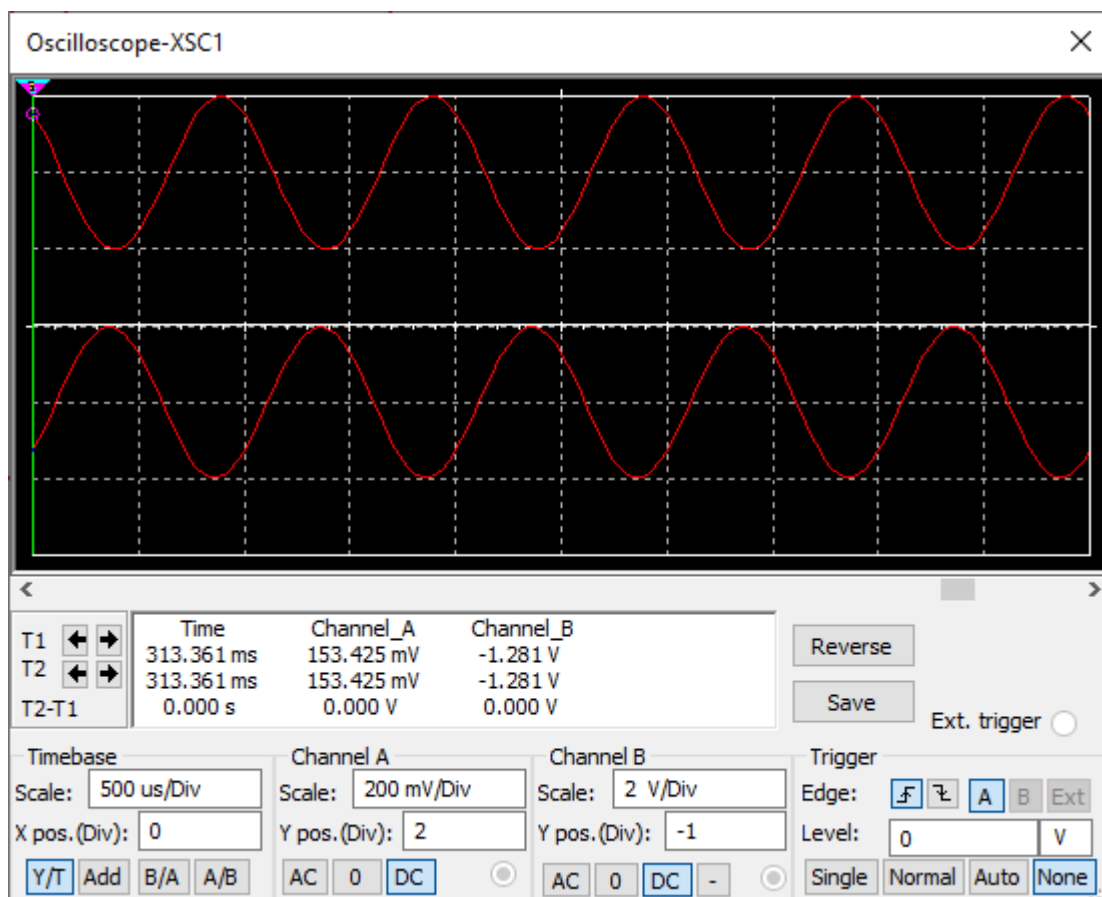
So, input impedance is $2.02K\Omega$ and the output impedance was confirmed at $2.5K\Omega$

Capacitors and their effect on gain

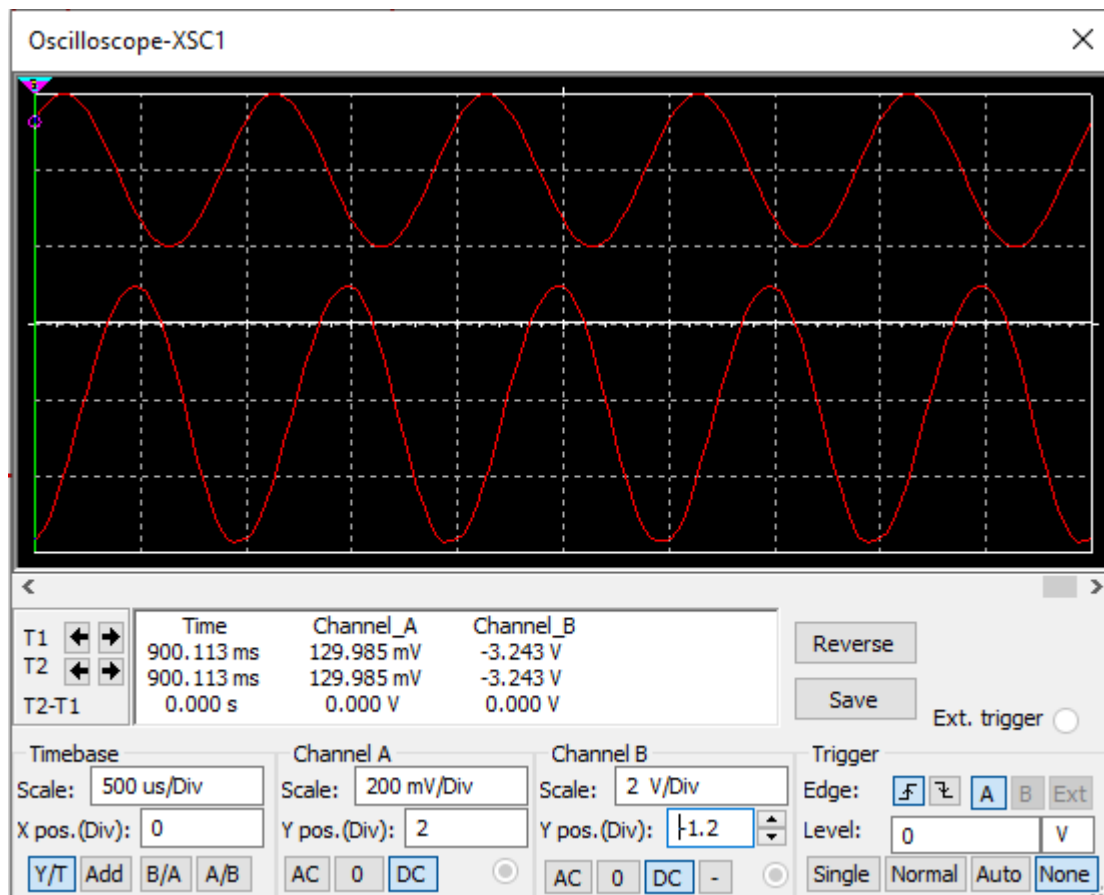
There are several ways in which we can affect the gain in the circuit. One of them is by adding a capacitor across the emitter resistor. Once you put the capacitor in parallel with the emitter resistor, the AC signal bypasses the resistor, hence the capacitor has the name 'bypass capacitor.'

According to (Elprocus, 2019), "A bypass capacitor basically bypasses AC noise that may be on a DC signal, filtering out of AC so that a clean, pure DC signal goes through without several AC ripples." So, when the bypass capacitor is connected in parallel with the emitter resistor, the voltage gain of the transistor increases.

For example, the two screenshots below are readings from the single stage amplifier I designed earlier. The first photo shows the gain without the capacitor which was the gain of 10 we were seeking as part of the brief.



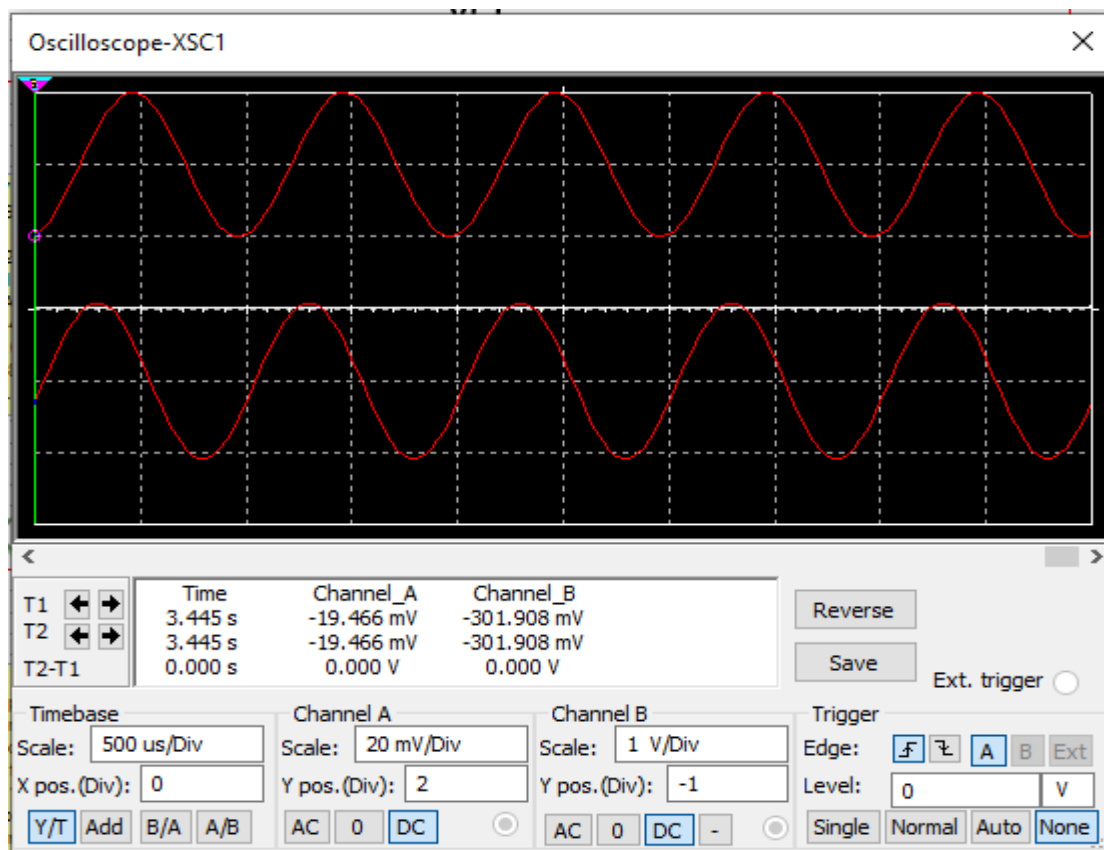
The second screen shot below shows the effect of adding a 1uF capacitor in parallel with the emitter resistor.



As you can see from the reading, the input stays the same at 400mV peak to peak, however the output has increased significantly from 4V peak to peak, to approximately 6.5V peak to peak. This means that the capacitor has increased the gain from 10, to 16.25.

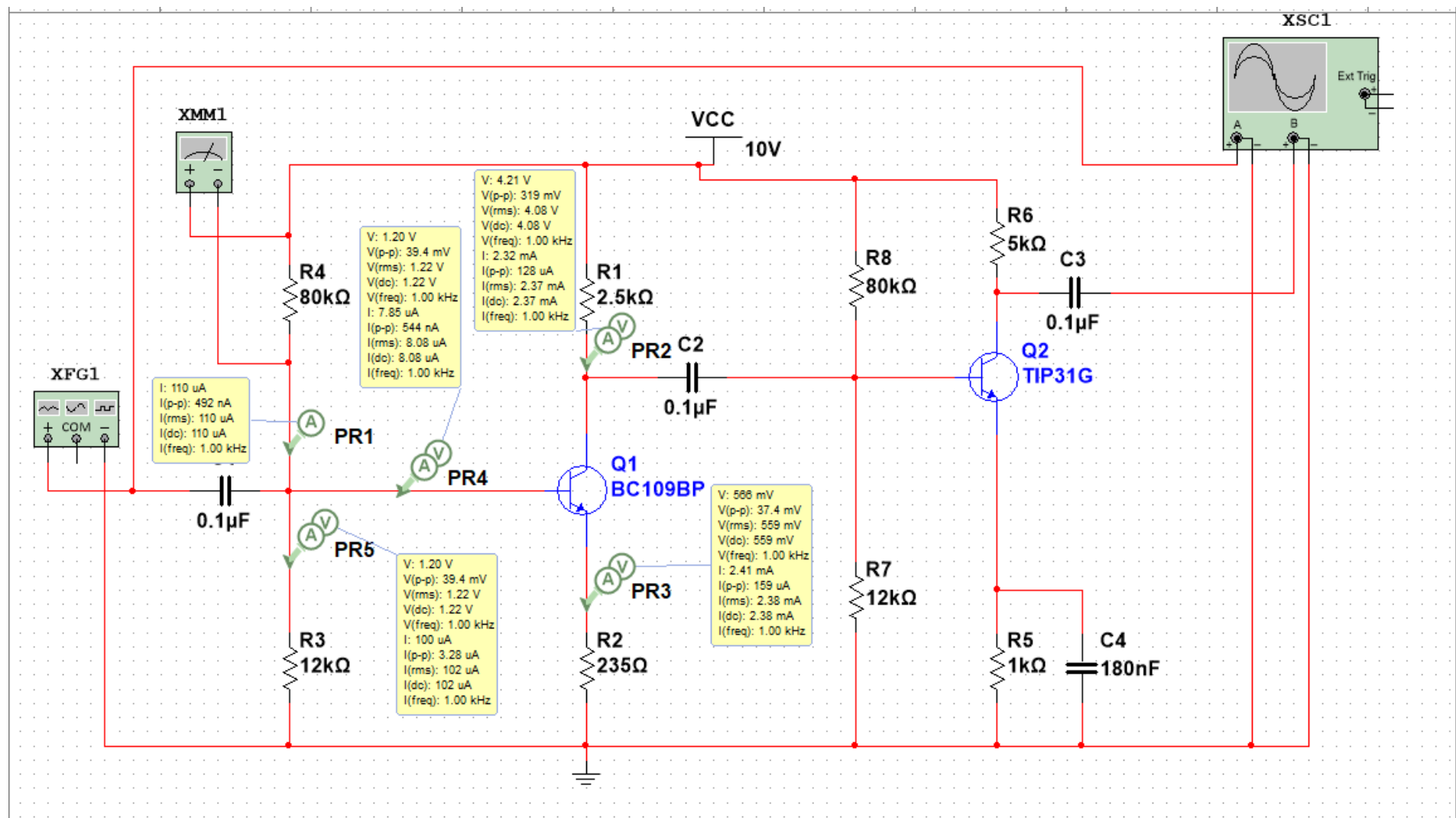
2 stage amplifier – Multisim

The final part of Task 1 asks us to design a 2 stage amplifier in Multisim, such that the overall gain is 50. Below is a screenshot from the oscilloscope in Multisim showing that we have achieved that.



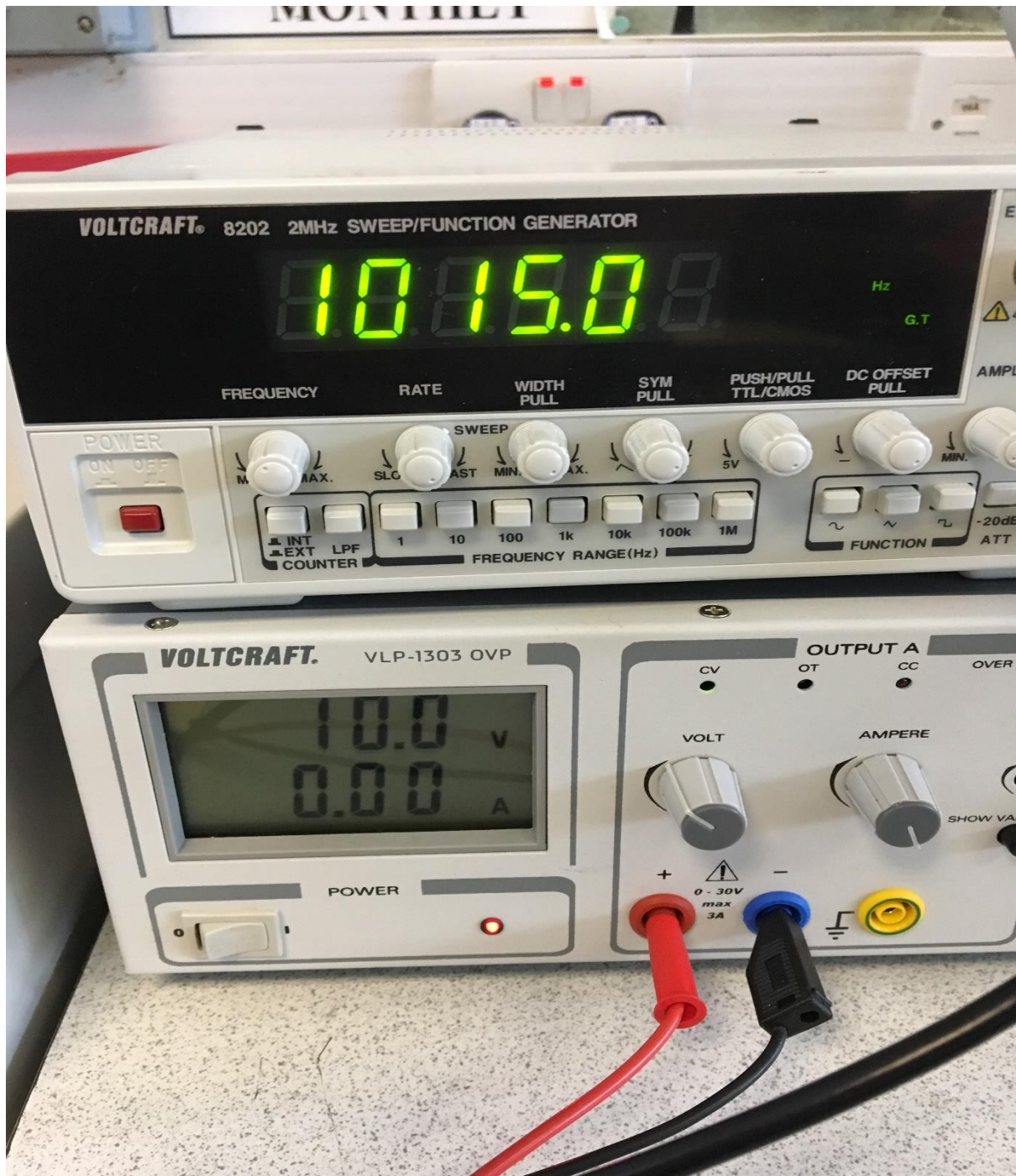
As we can see the first waveform recorded at the input shows a signal of 40mV peak to peak. The second waveform which was measured at the output, shows a waveform with a signal measuring 2V peak to peak. This is a gain of exactly 50.

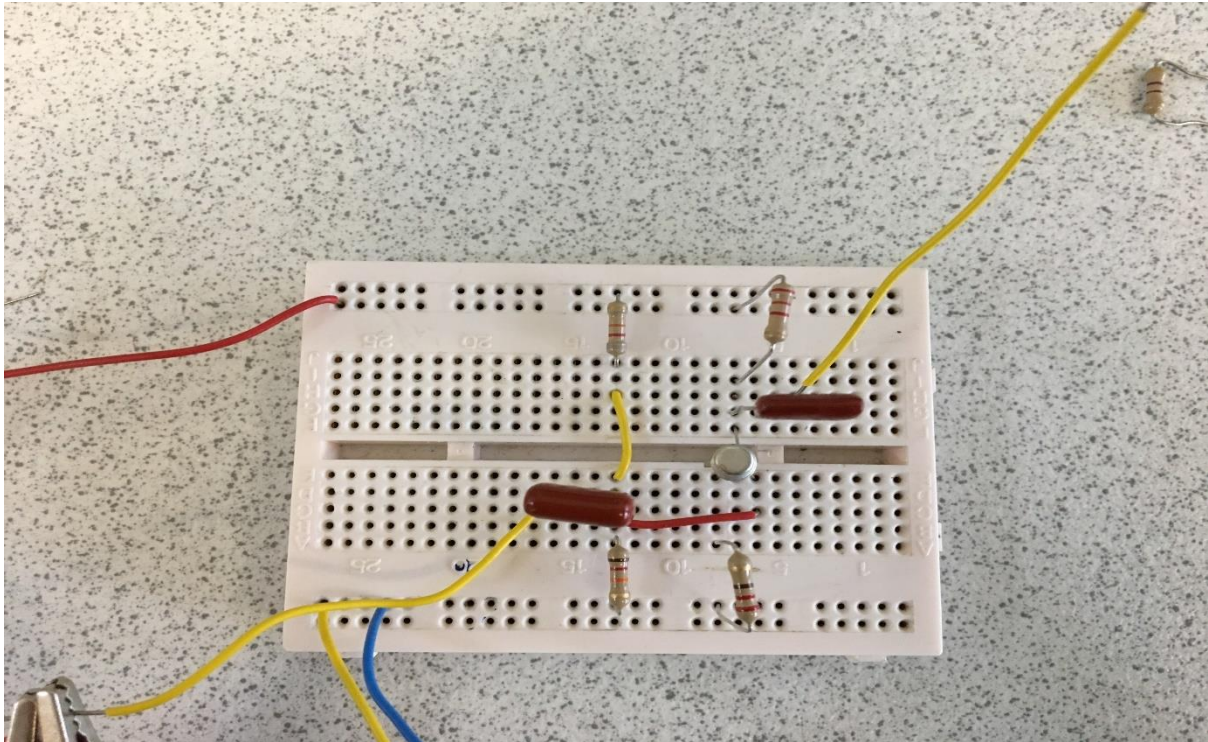
To design the circuit to do this I took my initial single stage amplifier with a gain of 10. This meant that to achieve a gain of 50 my second stage had to achieve a secondary amplification of 5. Therefore, I duplicated my first stage and changed the values of RC and RE to 5K Ω and 1K Ω respectively. This means that because RC is 5 times bigger than RE, we will achieve a gain of 5, ultimately achieving a 2 stage amplifier with a gain of 50. The circuit can be shown on the next page.



Task 2 – Construction of designed circuit

Task 2 asks us to physically build the designed circuit and compare the results. Below is the constructed circuit on breadboard, the power supply and function generator with the indicated values.



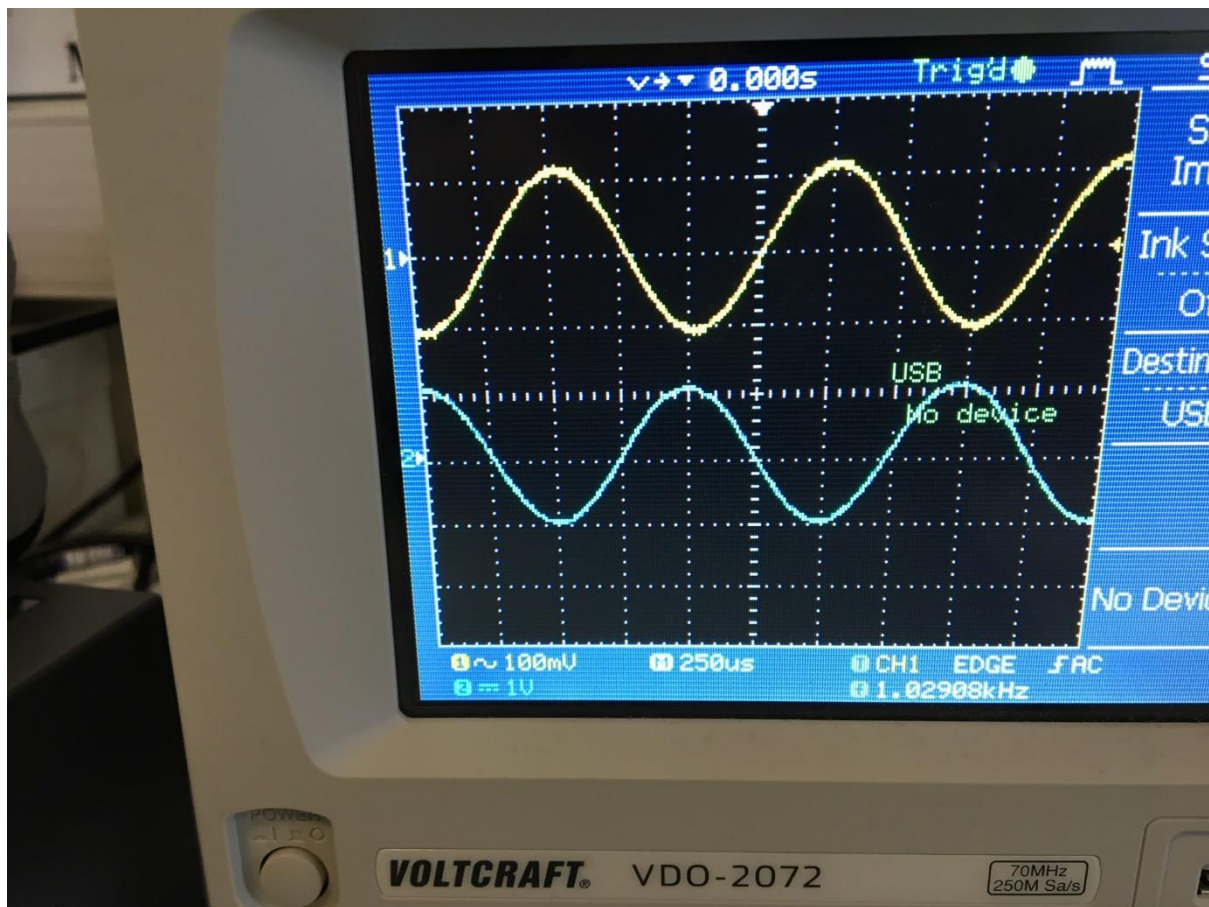


The function generator indicates that we injected a 1KHz sinewave into the circuit. The power supply shows that we powered the circuit using 10V as requested. The final photo shows the circuit constructed on a breadboard. Below is a table showing what value components we chose in our design, and what components we used for the build.

Designator	Design Value	Constructed Value
R1	80K Ω	82K Ω
R2	12K Ω	12K Ω
RC	2.5K Ω	2.2K Ω
RE	235 Ω	220 Ω
C1	0.1 μ F	0.1 μ F
C2	0.1 μ F	0.1 μ F
T1	BC109	BC109

As you can see with the resistors, there are slight variations in the values. This is because resistors are only manufactured in certain values. If we wanted to be 100% accurate and match the exact values of the resistors, we could use decade boxes, but for the purpose of this experiment, we have used the closest valued resistors.

The last piece of equipment shown below is an oscilloscope which we used to measure the difference in the waveforms at the input and the output.



The yellow waveform on top, is the input. This waveform is 200mV peak to peak. The blue waveform on the bottom is measured at the output. This waveform is 2V peak to peak. This is a gain of exactly 10, which is the same as our designed circuit. The waveform is also 180 degrees out of phase, same as our designed circuit.

We haven't really seen a difference between our simulated circuit and the one we have constructed. The main thing that would have caused any differences would have been the values of the resistors as they are not identical. Also, the resistors we were using had a gold tolerance band, which means that the value of the resistor can be +/- the indicated value.

This circuit was also demonstrated fully working to my lecturer.

BC109 Series

Low Power Bipolar Transistors

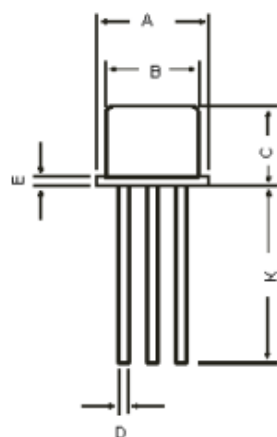
multicomp



Feature:

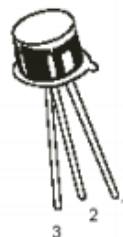
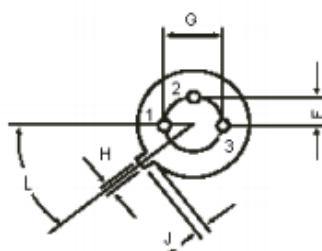
- NPN Silicon Planar Epitaxial Transistors.

TO-18 Metal Can Package



Dimensions	Minimum	Maximum
A	5.24	5.84
B	4.52	4.97
C	4.31	5.33
D	0.40	0.53
E	-	0.76
F	-	1.27
G	-	2.97
H	0.91	1.17
J	0.71	1.21
K	12.70	-
L	45°	

Dimensions : Millimetres



Pin Configuration:

1. Emitter
2. Base
3. Collector

multicomp

BC109 Series

Low Power Bipolar Transistors



Absolute Maximum Ratings

Description	Symbol	BC109	Unit
Collector-Emitter Voltage	V_{CEO}	25	V
Collector-Base Voltage	V_{CBO}	30	
Emitter-Base Voltage	V_{EBO}	5.0	
Collector Current Continuous	I_C	0.2	A
Power Dissipation at $T_a = 25^\circ\text{C}$ Derate above 25°C	P_D	0.6 2.28	W mW/ $^\circ\text{C}$
Power Dissipation at $T_C = 25^\circ\text{C}$ Derate above 25°C		1.0 6.67	
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	$^\circ\text{C}$
Thermal Resistance			
Junction to Case	$R_{th(j-c)}$	175	$^\circ\text{C/W}$

Electrical Characteristics ($T_a = 25^\circ\text{C}$ unless otherwise specified)

Description	Symbol	Test Condition	Minimum	Maximum	Unit
Collector-Emitter Voltage	V_{CEO}	$I_C = 2\text{mA}, I_B = 0$	25	-	V
Emitter Base Voltage	V_{EBO}	$I_E = 10\mu\text{A}, I_C = 0$	5.0	-	
Collector Cut off Current	I_{CBO}	$V_{CB} = 25\text{V}, I_E = 0$	-	15	nA
		$T_{amb} = 125^\circ\text{C}$ $V_{CB} = 25\text{V}, I_E = 0$	-	4.0	μA
DC Current	h_{FE}	$I_C = 10\mu\text{A}, V_{CE} = 5\text{V}$ B Group	40	-	-
		C Group	100	-	
		$I_C = 2\text{mA}, V_{CE} = 5\text{V}$ B Group	200	800	
		C Group	200 420	450 800	
Base Emitter Saturation Voltage	$V_{BE(Sat)}$	$I_C = 10\text{mA}, I_B = 0.5\text{mA}$	-	0.83 1.05	V
Collector Emitter Saturation Voltage	$V_{CE(Sat)}$	$I_C = 100\text{mA}, I_B = 5\text{mA}$	-	0.25 0.60	
Base Emitter On Voltage	$V_{BE(on)}$	$I_C = 2\text{mA}, V_{CE} = 5\text{V}$ $I_C = 10\text{mA}, V_{CE} = 5\text{V}$	0.55 -	0.70 0.77	



BC109 Series

Low Power Bipolar Transistors



Electrical Characteristics ($T_a = 25^\circ\text{C}$ unless otherwise specified)

Description	Symbol	Test Condition	Minimum	Maximum	Unit
Collector Knee Voltage	$V_{CE(K)}$	$I_C = 10\text{mA}$, $I_B = \text{The value for which } I_C = 11\text{mA} \text{ at } V_{CE} = 1\text{V}$	-	0.60	V
Transition Frequency	f_t	$V_{CE} = 5\text{V}$, $I_C = 10\text{mA}$, $f = 100\text{MHz}$	150	-	MHz
Noise Figure	NF	$V_{CE} = 5\text{V}$, $I_C = 0.2\text{mA}$ $R_g = 2\text{k}\Omega$ $F = 30\text{Hz to } 15\text{KHz}$ $F = 1\text{kHz}, B = 200\text{Hz}$	-	4.0 4.0	dB dB
Output Capacitance	C_{obo}	$V_{CB} = 10\text{V}$, $f = 1\text{MHz}$	-	4.5	pF
Small Signal Current Gain	h_{fe}	ALL $f = 1\text{kHz}$ $I_C = 2\text{mA}$, $V_{CE} = 5\text{V}$ B Group C Group	240 240 450	900 500 900	-
Input Impedance	h_{ie}	$I_C = 2\text{mA}$, $V_{CE} = 5\text{V}$ B Group C Group	3.2 6.0	8.5 15	$\text{K}\Omega$ $\text{K}\Omega$
Output Admittance	h_{oe}	$I_C = 2\text{mA}$, $V_{CE} = 5\text{V}$ B Group C Group	-	60 110	$\mu\Omega$

Part Number Table

Package	Part Number
TO-18	BC109
	BC109B
	BC109C



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Word count excluding reference list, 2073 word