



12 Tudalen

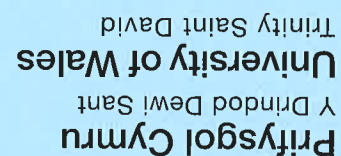
1. Rhowch yr holl wybodaeth y gofynnir amdani yn y blychau isod.
2. Rhowch eich enw yn y lle a ddarparwyd ar y dde, plygwch ef a'i selio i lawr (gan ddefnyddio'r label a ddarparwyd) i guddio'ch enw.
3. Rhaid i'r atebion fod mewn llawysgrifen ddarllenadwy. Gall yr Arholwyr naill ai anwybyddu sgrïpt annarllenadwy, neu drefnu iddi gael ei theipio a chael yr ymgeisydd i dalu.
4. Ysgrifennwch eich atebion mewn inc.
5. Dechreuwch bob ateb ar dudalen newydd. Gwnewch unrhyw fras nodiadau yn y llyfr atebion a thynnu llinell drwyddynt.
6. Ni ddylid rhwygo unrhyw ran o'r llyfr hwn; rhaid ei gyflwyno yn gyfan.
7. Os defnyddir mwy nag un llyfr, rhwymwch hwy gyda'i gilydd gan ddefnyddio'r tagiau sydd ar gael oddi wrth y gwyliwr/gwylwyr.
8. Rhaid dychwelyd pob llyfr. Ni chaniateir mynd â llyfrau atebion, wedi eu defnyddio neu heb eu defnyddio, allan o'r lleoliad arholi o dan unrhyw amgylchiadau.

1	Rhif Myfyriwr	
2	Teitl y Papur Arholiad	
3	Cod y Modwl	
4	Dyddiad ac Amser yr Archoliad	
5	Lleoliad yr Arholiad	
6	Rhif Sedd	
7	Nifer y Llyfrau Atebion a gyflwynwyd	

Llenwch, plygwch a seliwch (gweler nodyn 2 isod)

CYFENW: _____

ENW(AU) CYNTAF: _____

[illegible]

Instructions to Candidates

1. Please give the information requested in the boxes below.

2. Enter your name in the space provided to the right, fold over and seal down (using the label provided) to hide your name.

3. The answers must be legible and not be charged to the candidate.

4. Write your answers in ink.

5. Begin each answer on a fresh page. Do all rough work in the answer book and cross it through.

6. No part of this book is to be torn out; it must be handed in complete.

7. If more books than one are used, fasten them together using the tags available from the invigilator(s).

8. Every book must be handed in. In no circumstances may answer books, used or unused, be taken out of the examination venue.

1	Student Number	
2	Title of Examination Paper	Computer Architecture
3	Module Code	ACCA4022
4	Date and Time of Examination	5/12/2022
5	Examination Venue	
6	Seat Number	
7	Number of Answer Books handed in	

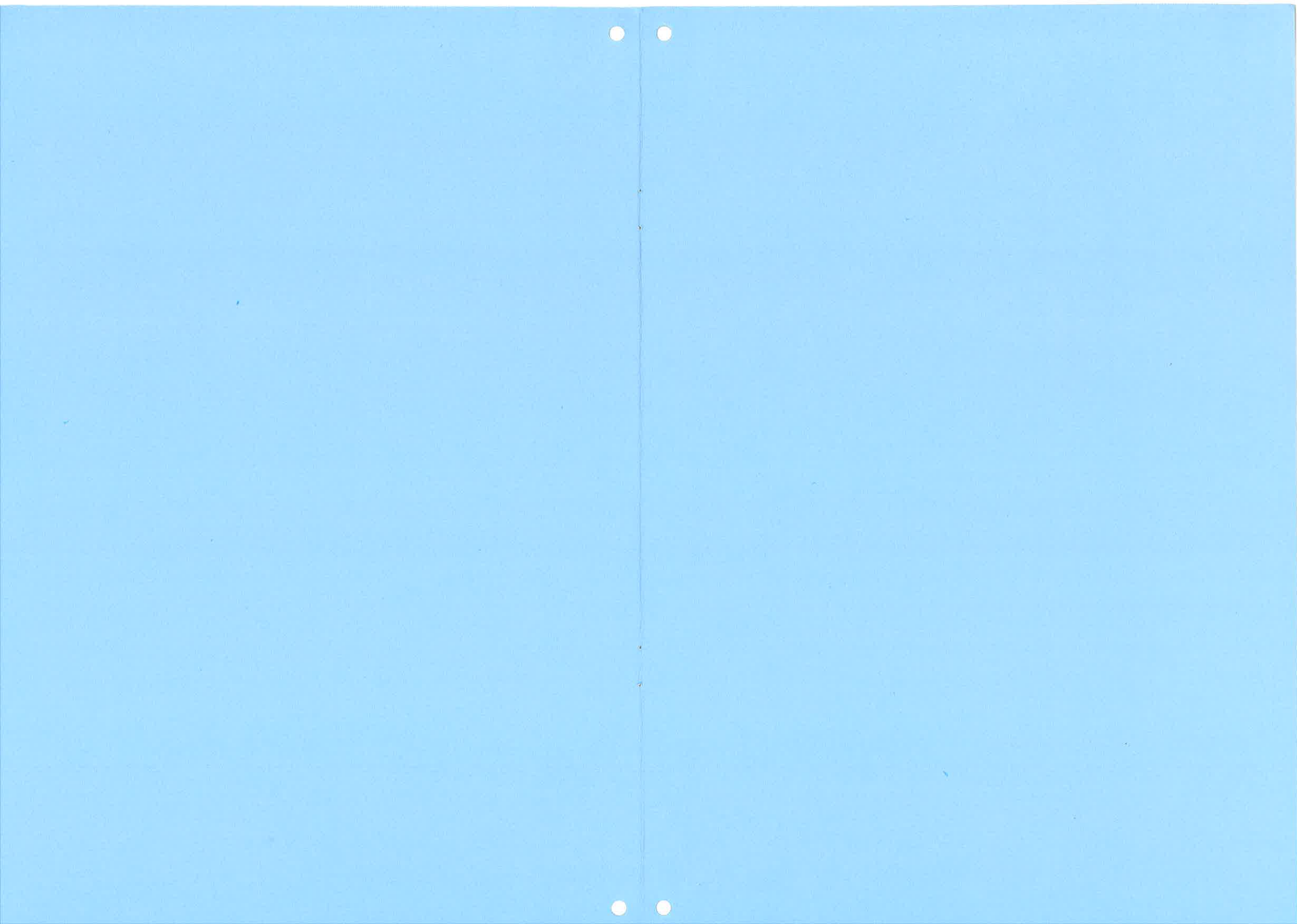
(Gweler yr ochr arall am y fersiwn Cymraeg)

[illegible]

Complete, fold and seal
(see note 2 below)

SURNAME: Abanasi

FORENAME(S): Gheorghe Loca



Question No.

Examiner Only

Question No.

T 4012290

263

$$x = 256 - 263$$

$$\xi = h - 1$$

$$3 - 2 = 1$$

$$0 = 1 - 1$$

to Octal

3 5 1 3 2

Answer: 35132

3 5 1 3 0

Question 5

RAID (Redundant Array of Independent Disks) is a technology that combines multiple disk drives into a single logical unit and offers increase in storage (reliability) performance, ~~performance~~ and performance improvement. There are also 5 different levels such as: Striping, Mirroring, Striping with parity, Raid 10 and Striping with dual parity.

b

a.

Question 7

Differences between Harvard and Neuman architecture :

1. Memory organisation
2. Instruction and data fetching
3. Instruction and data transfer
4. Program and data memory access
5. Complexity and cost.

IV.

(1010011011)

$$(A6B8)_{16} = 1010011011001_2 \Rightarrow 42819_{10}$$

V

~~If when you have 4 bits of (storage) storing numbers, you can represent a total of 16 different values. This is because each bit have two possible states.~~

When you have 4 bits of storing numbers, you can represent a total of 16 different values. This is because each bit have two possible states (0 or 1) and by raising 2 to the power of 4 you account for all the possible combinations of these four bits.

Question 2

1. Mouse - Input
2. Monitor - Output
3. RAM - Storage
4. Ethernet Port - Communication
5. Microphone - Input
6. Flash Drive - Storage
7. Modem - Communication
8. Game pad - Input

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Question 6

There are three types of buses:

- Data bus - sends and exchange signals between the CPU and memory and also CPU and I/O and holds the data in the specified locations.
- Address bus - is a signal line that specifies the locations of the memory. When exchanging data it has to be specified the take off destination of the data or the (data) storage destination of the data
- Control bus - signal line that specifies whether to read or (write) write to the location specified by the address bus. The memory I/O specified on the Address bus receive the data which is sent to the data bus when instructed (written) by the control bus.

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