

Examination Answer Books

12 Pages

Instructions to Candidates

1. Please give the information requested in the boxes below.
2. Enter your name in the space provided to the right, fold over and seal down (using the label provided) to hide your name.
3. The answers must be legibly written. The Examiners can either ignore illegible script or have it typed and the expense of typing charged to the candidate.
4. Write your answers in ink.
5. Begin each answer on a fresh page. Do all rough work in the answer book and cross it through.
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8. **Every book must be handed in. In no circumstances may answer books, used or unused, be taken out of the examination venue.**

1	Student Number	1503008/1
2	Title of Examination Paper	ELECTRONIC DESIGN
3	Module Code	SGEE 6000
4	Date and Time of Examination	03/05/19 09:30
5	Examination Venue	G24
6	Seat Number	1
7	Number of Answer Books handed in	1

(Gweler yr ochr arall am y fersiwn Cymraeg)

Complete, fold and seal
(see note 2 below)

SURNAME: DYER

FORENAME(S): EMVR WYN

[illegible]

38%

(See the other side for English version)

7	Nifer y Llyfrau Alebion a gyflwynwyd	
6	Rhif Sedd	
5	Lleoliad yr Arholiad	
4	Dyddiad ac Amser yr Arholiad	
3	Cod y Modwl	
2	Teitl y Papur Arholiad	
1	Rhif Myfyrwr	

Rhestrwch ffurf cwsylliau a ymgeisydd	Cyfanswm
Ae Dilbenion y Swyddfa	

- guddio'ch anw.
1. Rhaid i'r atebion fod mewn llawysgriften ddarlennadwy. Gall yr Arholwyr naill ai anwybyddu sgrïpt annarllennadwy, neu drefnu iddi gael ei theipio a chael yr ymgaisydd i dalu.
 2. Ysgrifennwch eich atebion mewn inc.
 3. Dechreuwch bob ateb ar dudalen newydd. Gwnewch unrhyw fras nodiadau yn y llyfr atebion a thynnu llinell drwyddynt.
 4. Ni ddylid rhwygo unrhyw ran o'r llyfr. hwn; rhaid ei gyflwyno yn gyfan.
 5. Os defnyddir mwy nag un llyfr, rhwyngwch hwy gyda'i gilydd gan ddefnyddio'r tagiau sydd ar gael oddi wrth y gwyllwyr/gwylwyr.
 6. Rhaid dychwelyd pob llyfr. Ni chaniateir mynd â llyfrau atebion, wedi eu defnyddio neu heb eu defnyddio, allan o'r lleoliad arholi o dan unrhyw amgylchadau.

1. Rhwch yr holl wybodaeth y gofynnir amdani yn y blychau isod.
2. Rhwch eich enw yn y lle a ddarparwyd ar y dde, plynwch et a'i seilio i lawr (gan ddefnyddio'r label a ddarparwyd) i guddio'ch enw.

Cyfarwyddiadau i Ymgeiswyr

12 Tüdalen

Llyfr Atebion Arholiadau

Llenwch, plygwch a seliwch
(gweler nodyn 2 isod)

CYFENW:

ENW(AU) CYNTAF:

A1 Find $R_{s(max)}$

$$I_{L(max)} = \frac{2.5}{1000} = 2.5 \text{ mA}$$

$$R_{s(max)} = \frac{10 - 2.5}{(2.5 \times 10^{-3}) + (1.2 \times 10^{-3})} = 2.03 \text{ K}\Omega$$

A2. In the event of an unexpected increase of output voltage, the voltage across R_2 also increases, which as a result increases the amount of V_F fed to the base of Q_1 , causing voltage to drop across R_3 , resulting in reduced voltage applied to the base of Q_2 , dropping the overall V_{out} .

A3. A ~~switch~~ SMPS operates on a high frequency square-wave which is manipulated through Pulse Width Modulation to lower the DC output.

As a high frequency means of transformation is used, the components used in the design of the SMPS are ~~are~~ smaller and cheaper than components used in line transformation.

Voltage Regulation in a SMPS is done through the adjustment of the Mark-to-Space ratio where the Square-wave output is compared to the reference voltage.

A4.i. $P_D = 500 \text{ mW}$
 $T_J = 100^\circ\text{C}$

$$T_{A(\text{desired})} = 22^\circ\text{C}$$

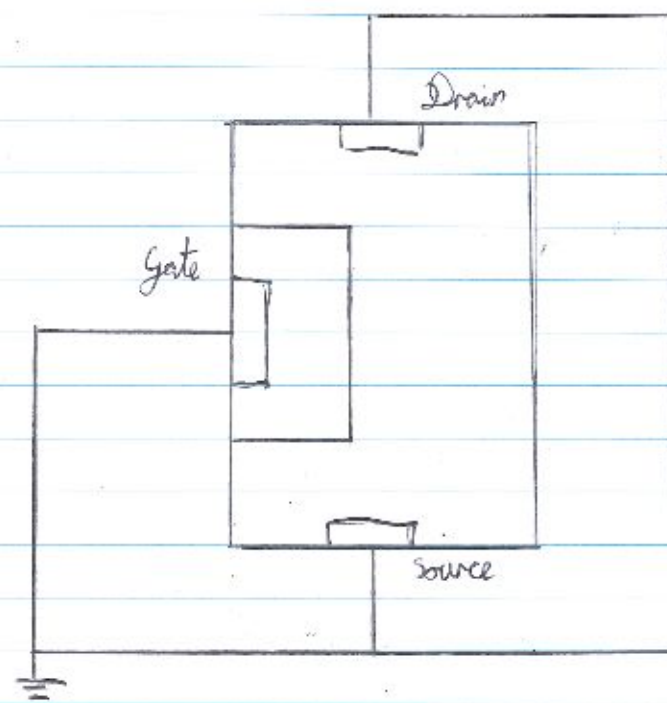
$$\theta_{JA} = 180^\circ\text{C/W}$$

$$T_A = 100 - (500 \times 10^{-3}) \times 180 = 10^\circ\text{C}$$

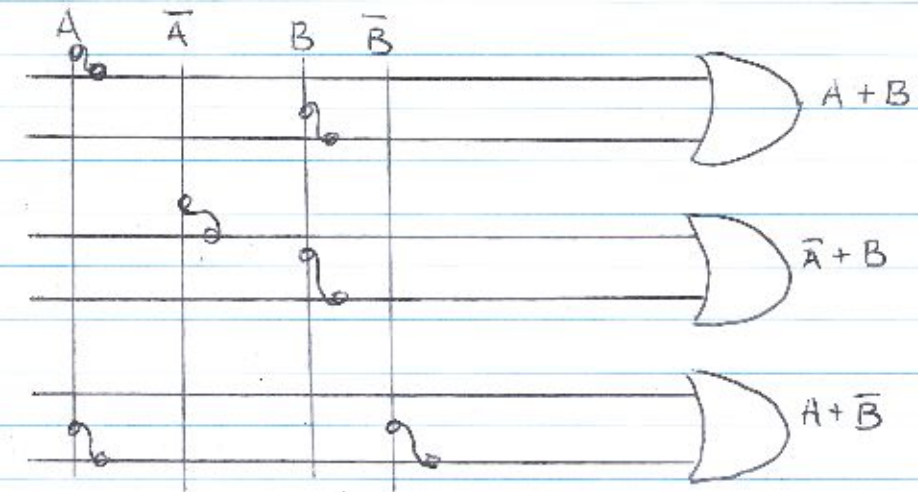
As the regulator runs cooler at 10°C , than ambient room temperature, a heat-sink is not required.

ii $\theta_{SA} = \frac{T_J - T_A}{P_D} - \theta_{CS} - \theta_{SC} = \frac{100 - 22}{5} - 1.6 - 2.5 = 11.5$

A5.



A7



①

③

21

04

Bl a:

i. Find the Breakdown Voltage

$$V_{in} = 15V$$

$$\beta = 50$$

$$V_{BE} = 0.6V$$

$$I_{Z(min)} = 5.6mA$$

$$I_C = 1.2A$$

$$I_B = \frac{I_C}{\beta} = \frac{1.2}{50} = 24mA$$

b As voltage increases across R_4 , the applied voltage to the base of Q_3 , which in turn causes voltage to drop across on the base of Q_2 , reducing the current flow through Q_2

c

$$P_D = 5W$$

$$T_A = 60^\circ C$$

$$T_J = 130^\circ C$$

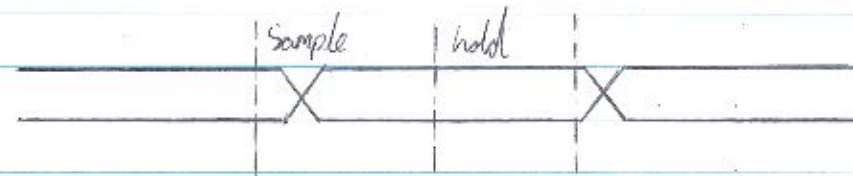
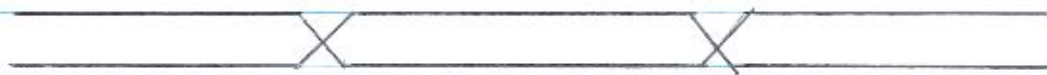
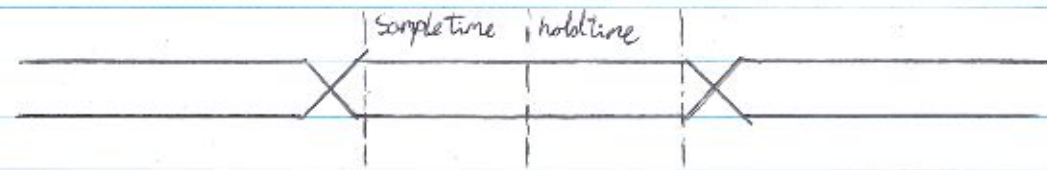
$$\theta_{JC} = 2.5^\circ C/W$$

$$\theta_{CS} = 1.6^\circ C/W$$

B2 a. A JFET is made up of only one carrier material where the cathode has electrons and anode has holes.
The gate of the JFET is not current driven

$$b. V_{GS} = V_{GS(OFF)} \left[1 - \sqrt{\frac{I_D}{I_{DSS}}} \right] = -4.5 \left[1 - \sqrt{\frac{8 \times 10^{-3}}{12 \times 10^{-3}}} \right] = -825.77 \text{ mV}$$

c.



If a signal changes state after the sample point, the signal state could be in either state after the hold.

$$d. \tau = 0.2 \text{ ns}$$

$$T_0 = 9.6 \times 10^{-18} \text{ s}$$

$$t_{su} = 1 \text{ ns}$$

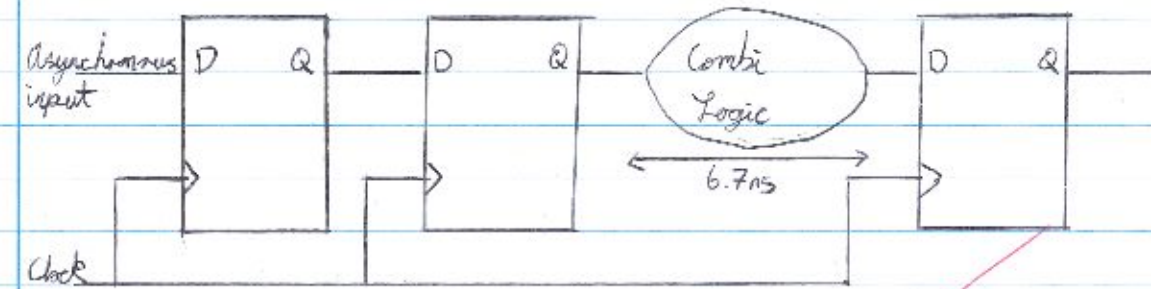
$$i. t_r = t_{proc} + t_{su} = 6.7 \times 10^{-9} + 1 \times 10^{-9} = 7.7 \text{ ns}$$

$$MTBF = \frac{e^{\frac{7.7 \times 10^{-9}}{0.2 \times 10^{-9}}}}{(9.6 \times 10^{-18}) \times (20 \times 10^6) \times (2 \times 10^6)} = 1.368 \times 10^{20} \text{ Hz}$$

$$ii. MTBF = \frac{e^{\frac{7.7 \times 10^{-9}}{0.2 \times 10^{-9}}}}{(9.6 \times 10^{-18}) \times (80 \times 10^6) \times (2 \times 10^6)} = 34.194 \times 10^{18} \text{ Hz}$$

the MTBF in this recalculated state with a clock frequency of 80MHz, the MTBF is smaller

iii. An additional flip flop may be incorporated into the design.

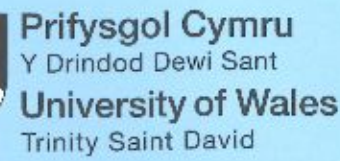


$$MTBF = \left\{ \frac{e^{\frac{t_r}{T}}}{T_0 \times f \times a} \right\} + K \left\{ \frac{e^{\frac{t_r}{T}}}{T_0 \times f} \right\}$$

$$MTBF = \left\{ \frac{e^{\frac{7.7 \times 10^{-9}}{0.2 \times 10^{-9}}}}{(9.6 \times 10^{-18}) \times (80 \times 10^6) \times (2 \times 10^6)} \right\} + 1 \times \left\{ \frac{e^{\frac{7.7 \times 10^{-9}}{0.2 \times 10^{-9}}}}{(9.6 \times 10^{-18}) \times (80 \times 10^6)} \right\}$$

$$= 68.387 \times 10^{24} \text{ Hz}$$

14/30



12 Pages

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2	Title of Examination Paper	ELECTRONIC DESIGN
3	Module Code	SGEE 6000
4	Date and Time of Examination	3/5/2019 4:30
5	Examination Venue	COLEG SIR CAR 624
6	Seat Number	2
7	Number of Answer Books handed in	

(Gweler yr ochr arall am y fersiwn Cymraeg)

FORENAME(S): DAVID SAMUEL

List the numbers of the questions you have attempted	Office Use
A	28
B1	30
B2	22
Total	80%

80%

Nifer y Llyfrau Atebion
a gyflwynwyd

7	Nifer y Llyfrau Atebion a gyflwynwyd
6	Rhif Sedd
5	Lleoliad yr Arholiad
4	Dyddiad ac Amser yr Arholiad
3	Cod y Modwl
2	Tittl y Papur Arholiad
1	Rhif Myfyrwr

[illegible]

1. Rhaid i'r atebion fod mewn llawysgriflen ddarlennadwy. Gall yr Arholwyr naill ai anwybyddu sgrïpt annarlennadwy, neu drefnu iddi gael ei thafio a chael yr ymgeisydd i dalu.
2. Ysgrifennwch eich atebion mewn inc.
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1. Rhwch yr holl wybodaeth y gofynnir amdani yn y blychau isod.
2. Rhwch eich enw yn y lle a ddarparwyd ar y dde, pwygch et a'i seilio i lawr (gan ddefnyddio'r label a ddarparwyd) i guddio'ch enw.

Cyfarwyddiadau i Ymgeiswyr

12 Tudalen

Llyfr Atebion Arholiadau



Prifysgol Cymru
Y Drindod Dewi Sant
University of Wales
Trinity Saint David

Llenwch, plygwrch a seliwrch
(gweler nodyn 2 isod)

CYFENN:

ENW(AU) CYNTAF:

$$A1. I_{L(max)} = \frac{V_z}{R_{L(min)}} = \frac{2.5}{1K} = 2.5mA \quad \checkmark$$

$$R_{s(max)} = \frac{V_{in} - V_z}{I_{L(max)} + I_{z(min)}} = \frac{10 - 2.5}{2.5mA + 1.2mA} = 5769.231\Omega \quad \checkmark$$

A2. An unregulated DC voltage or rectified AC voltage is used as a source. To regulate the voltage on the output, a voltage feedback is used. If the output voltage were to increase above the regulated amount, the voltage across R_2 would also increase as it is part of the output circuit. This in turn increases the feedback voltage V_F . V_F is connected to the base of Q_1 which when increased produces a higher current on the collector of Q_1 . This current mostly flows through R_3 , which reduces the voltage on the base of Q_2 . This reduction on V_{BQ2} causes less voltage on the output, which offsets the initial increase and therefore maintaining a constant, regulated voltage. If the output voltage were to decrease, the opposite would occur where: V_{R2} decreases $\rightarrow V_F$ decreases $\rightarrow I_{CQ1}$ decreases $\rightarrow I_{R3}$ decreases $\rightarrow V_{BQ2}$ ~~decreases~~ increases $\rightarrow$ increased output voltage to offset initial decrease and maintain constant regulated voltage. $\checkmark$

A3. A high frequency square wave is used to drive electronic power circuit. SMPSs are used to convert DC supply, to high frequency, high current AC, then back to regulated DC through various means.

This double conversion is used as converting back to DC from AC at high frequencies requires much smaller and therefore cheaper and more space economic components such as transformers, inductors and capacitors in comparison to those that would be required if the conversion took place at line frequency.

The AC waveform generated is a high frequency square wave that can be used to drive pwn to regulate the output voltage. This method of regulation is much more efficient than linear regulated power supplies.

The combination of the high frequency square wave and switches is often used in inverters to convert DC supplies such as batteries and solar panels to mains potential AC.

To regulate voltage the mark to space ratio of the AC waveform is

changed. This is done by taking a feedback voltage from the output and comparing it to a stable reference voltage. This then controls the mark to space ratio of the square wave which drives the pump. This changes the duty cycle of the output voltage to increase/decrease it to its desired regulated value. This also stops over voltage/current and protects the circuit.

A4. $P_d = 500mW$ $T_j = 100^\circ C$ $\theta_{JA} = 180^\circ C/W$ $\theta_{CS} = 1.6^\circ C/W$ $\theta_{JC} = 2.5^\circ C/W$

i) $T_A = T_j - P_d \theta_{JA} = 100 - (500m)(180) = 10^\circ C$

Regulator does NOT need a heatsink

ii) $P_d = 5W$ $\theta_{CS} = 1.6^\circ C/W$

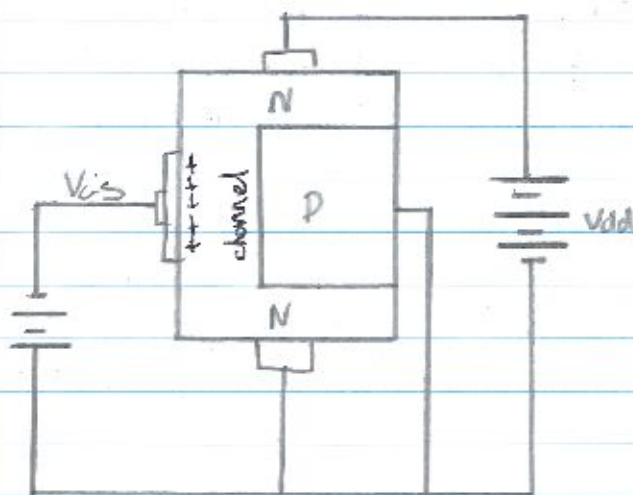
$\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA} \therefore \theta_{SA} = \theta_{JA} - \theta_{JC} - \theta_{CS}$

New $\theta_{JA} = \frac{T_j - T_A}{P_d}$

$\therefore \theta_{SA} = \frac{T_j - T_A}{P_d} - \theta_{JC} - \theta_{CS}$
 $= \frac{100 - 10}{5} - 2.5 - 1.6$

$= 13.9^\circ C/W$ heatsink required.

A5.



Depletion mode MOSFETs use a reverse voltage V_{gs} to control current flow. As the diagram shows, it has 2 layers, an n-layer and a p-layer. The current flows through the n-layer channel like it is a pipe. The smaller the channel

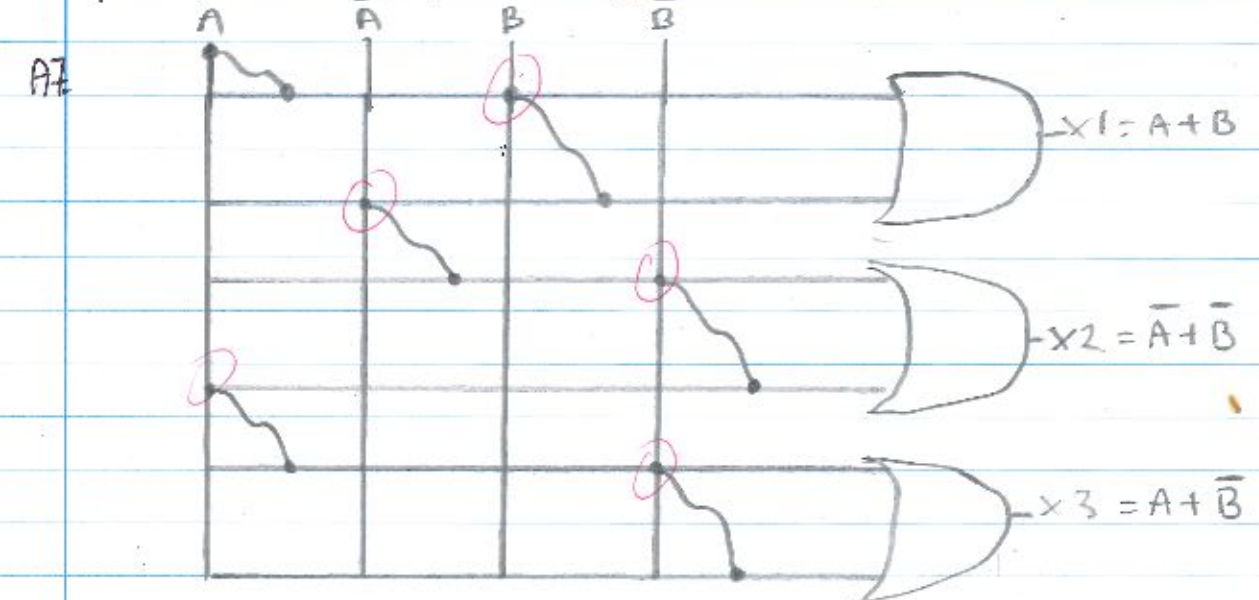
width, the less electrons can flow. If a reverse voltage is applied to the gate of the MOSFET, it repels free electrons in the channel and a layer of positive ions fill up the channel partly. If the negative/reverse voltage is increased, this effect also increases, allowing less free electrons to flow through the channel. $\therefore$ A depletion mode MOSFET

is a device which controls its current flow based on the reverse voltage V_{GS} .

A6. JFETs are unipolar devices as they utilize one junction however bipolar transistors use two.

JFETs are connected in reverse bias which gives high input impedance which provides isolation between input and output circuits. The bipolar transistor is connected in forward bias however and therefore has low input impedance and provides no isolation.

JFETs can have a gate current of 0A ($I_g = 0A$) to operate, whereas bipolar cannot.



Note junctions.

$$\text{Bb) i) } V_z = V_{out} - V_{BE} \\ = 6 - 0.6 = 5.4V$$

$$\text{ii) } R_s = \frac{V_{in} - V_z}{I_B + I_z} \quad I_B = \frac{I_c}{\beta} = \frac{1.2}{50} = 0.024A$$

$$= \frac{15 - 5.4}{0.024 + 5.6mA} = 324.3 \Omega$$

b) Series regulator circuits can easily be damaged if a load starts drawing excessive current. To counter this and protect the circuit, a current limiting circuit which consists of a transistor (Q_3) and a resistor (R_4). The resistor is connected between the base and emitter of Q_3 . When the current is normal, the voltage across R_4 is not enough to ON bias Q_3 , and therefore nothing happens.

However, if the current were to increase too much, the voltage across R_4 would ON bias the transistor Q_3 . This would cause a large current to be drawn on the emitter of Q_3 , which would flow through R_s . This would decrease the voltage on the base of Q_2 ~~which would limit the flow of current to the output.~~ (the pass transistor) which would limit the flow of current to the output. ~~essentially current limiting.~~ Therefore the current is limited and the circuit is protected.

$$\text{c) } P_d = 5W, T_A = 60^\circ C, H = 3'', 2'', E = 0.7, \text{ Fin thickness} = 0.01'' \\ T_J = 130^\circ C, \theta_{JC} = 2.5^\circ C/W, \theta_{CS} = 1.6^\circ C/W$$

$$\theta_{JA} = \frac{T_J - T_A}{P_d} = \frac{130 - 60}{5} = 14^\circ C/W$$

$$\theta_{JA} = \theta_{JA} - \theta_{JC} - \theta_{CS} \\ = 9.9^\circ C/W \text{ heatsink required}$$

For 3" heatsink

$$T_s = T_J - P_d \theta_{JA} = 130 - 5 \times 2.5 = 117.5 \\ h_r = 1.47 \times 10^{-10} \times E \left(\frac{T_s + T_A}{2} + 273 \right)^3 = 1.47 \times 10^{-10} \times 0.7 \left(\frac{117.5 + 60}{2} + 273 \right)^3 \\ = 4.871 \times 10^{-3}$$

$$h_c = 2.21 \times 10^{-3} \left(\frac{T_s - T_A}{H} \right)^{1/4} = 2.21 \times 10^{-3} \left(\frac{117.5 - 60}{3} \right)^{1/4} \\ = 4.624 \times 10^{-3}$$

$$h = h_r + h_c = 4.871 \times 10^{-3} + 4.624 \times 10^{-3} = 9.495 \times 10^{-3}$$

$$\alpha = 0.44 \text{ from nomograph} \\ \eta = 65\% \text{ from nomograph}$$

$$\theta_{SA} = \frac{1}{2 \times H^2 \times \eta \times h} = \frac{1}{2 \times 3^2 \times 0.65 \times 9.495 \times 10^{-3}} = 9.002^\circ C/W$$

For 2" heatsink

$$h_c = 2.21 \times 10^{-3} \left(\frac{117.5 - 60}{2} \right)^{1/4} = 5.117 \times 10^{-3}$$

$$h = 9.988 \times 10^{-3}$$

$$\alpha = 0.45$$

$$\eta = 91\% \text{ from nomograph}$$

$$\theta_{SA} = \frac{1}{2 \times 2^2 \times 0.91 \times 9.988 \times 10^{-3}} = 13.75^\circ C/W$$

The only suitable heatsink is the 3" heatsink as its θ_{SA} value is below the required θ_{SA} value of $9.9^\circ C/W$.

d) A boost converter is used to increase the ~~voltage~~ ^{output voltage} of a circuit if it does not provide enough. An example would be in electric cars where a battery would not be able to provide a high enough voltage to drive the motor, so a boost converter is used. Alternatively, boost converters are also used to prolong battery life. As a battery discharges, its voltage slowly decreases. If this were to decrease too much it may become useless for its application. However, a boost converter can boost a battery voltage back up to a sufficient level instead of it needing to be replaced. It operates by having a DC input, which flows through an inductor allowing it to gain energy in the form of a magnetic field.

~~While~~ while the MOSFET is ON. The MOSFET is controlled by a high frequency square wave which turns it ON and OFF rapidly.

During the ON state, the MOSFET shorts the right side of the inductor to ground. This allows the inductor to gain energy. Little to no current flows through the rest of the circuit as the diode, capacitor and load have much more impedance than the conductive MOSFET.

During the OFF state the sudden change stops the short circuit and the polarity of the potential across the inductor reverses due to its back emf. The energy in the magnetic field starts collapsing and it pumps current into the circuit.

The combination of V_{in} and V_L forward biases the diode and a voltage equal to $V_{in} + V_L$ is provided to the load, therefore increasing the output voltage. The capacitor charges to $V_{in} + V_L$ ready to discharge during the next ON cycle to provide a constant output voltage.

5

30/30

B2a) A JFET operates under the principle where a current flows through a channel which can be controlled by a voltage on its gate. The width of this channel determines how much current can flow, a wide channel effectively has a 'low' resistance and a thin channel has a 'high' resistance. A JFET only has a single junction which forms this channel. ~~V_{GS}~~ V_{GS} determines the width of the channel and controls how much current can flow. JFETs only use one type of charge carrier (electrons) rather than two (electrons and holes).

5

$$b) I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_{GS(off)}} \right]^2 \quad I_D = 8mA \quad I_{DSS} = 12mA \quad V_{GS(off)} = -4.5V$$

$$\frac{I_D}{I_{DSS}} = \left[1 - \frac{V_{GS}}{V_{GS(off)}} \right]^2 \rightarrow \sqrt{\frac{I_D}{I_{DSS}}} = 1 - \frac{V_{GS}}{V_{GS(off)}} \rightarrow \frac{I_D}{I_{DSS}} + \frac{V_{GS}}{V_{GS(off)}} = 1$$

$$1 - \sqrt{\frac{I_D}{I_{DSS}}} = \frac{V_{GS}}{V_{GS(off)}} \rightarrow V_{GS(off)} \left(1 - \sqrt{\frac{I_D}{I_{DSS}}} \right) = V_{GS}$$

$$\therefore V_{GS} = -4.5V \left(1 - \sqrt{\frac{8mA}{12mA}} \right) = -0.826V$$

4

c) Metastability in an FPGA is when a register enters an unknown state. This can happen in 2 ways:
A signal is introduced that is asynchronous to the clock domain whether it is an internal signal or external. This needs synchronising and a method of doing so is by implementing a multistage synchroniser.

Another cause for metastability is when there are multiple registers operating on the same synchronous clock, however phase or clock skew can cause metastability. This can be countered by modifying place and route configuration or by modifying output logic.

d) $F_{clk} = 20\text{MHz}$ $t_{clk} = 50\text{ns}$ $\frac{1}{20 \times 10^6} = 50 \times 10^{-9}$
 $t_{prop} = 6.7\text{ns}$ $t_{su} = 1\text{ns}$

i) resolution time, $t_r = t_{clk} - t_{prop} - t_{su}$
 $= 50\text{ns} - 6.7\text{ns} - 1\text{ns} = 42.3\text{ns}$

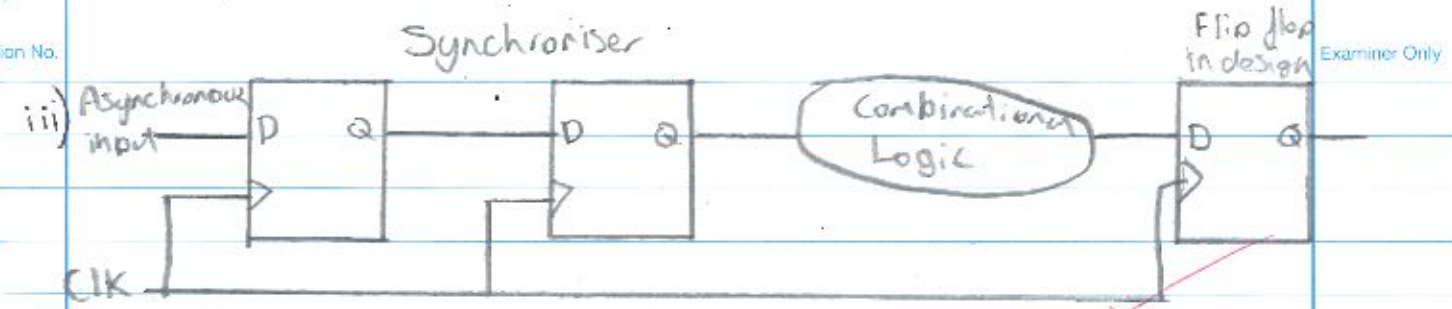
ii) $MTBF = \frac{e^{\frac{t_r}{T_0}}}{T_0 \times F \times a}$ $a = 2\text{MHz}$
 $T_0 = 9.6 \times 10^{-18}\text{s}$
 $MTBF = \frac{e^{\frac{42.3\text{ns}}{0.2\text{ns}}}}{9.6 \times 10^{-18} \times 20\text{M} \times 2\text{M}} = 1.857597843 \times 10^{95}$
 $= 5.89 \times 10^{87} \text{ years}$

CLOCK FREQUENCY QUADRUPLER

$F_{clk} = 80 \times 10^6$

$MTBF = \frac{e^{\frac{42.3\text{ns}}{0.2\text{ns}}}}{9.6 \times 10^{-18} \times 80\text{M} \times 2\text{M}} = 4.643994609 \times 10^{94}$
 $= 1.47 \times 10^{87}$

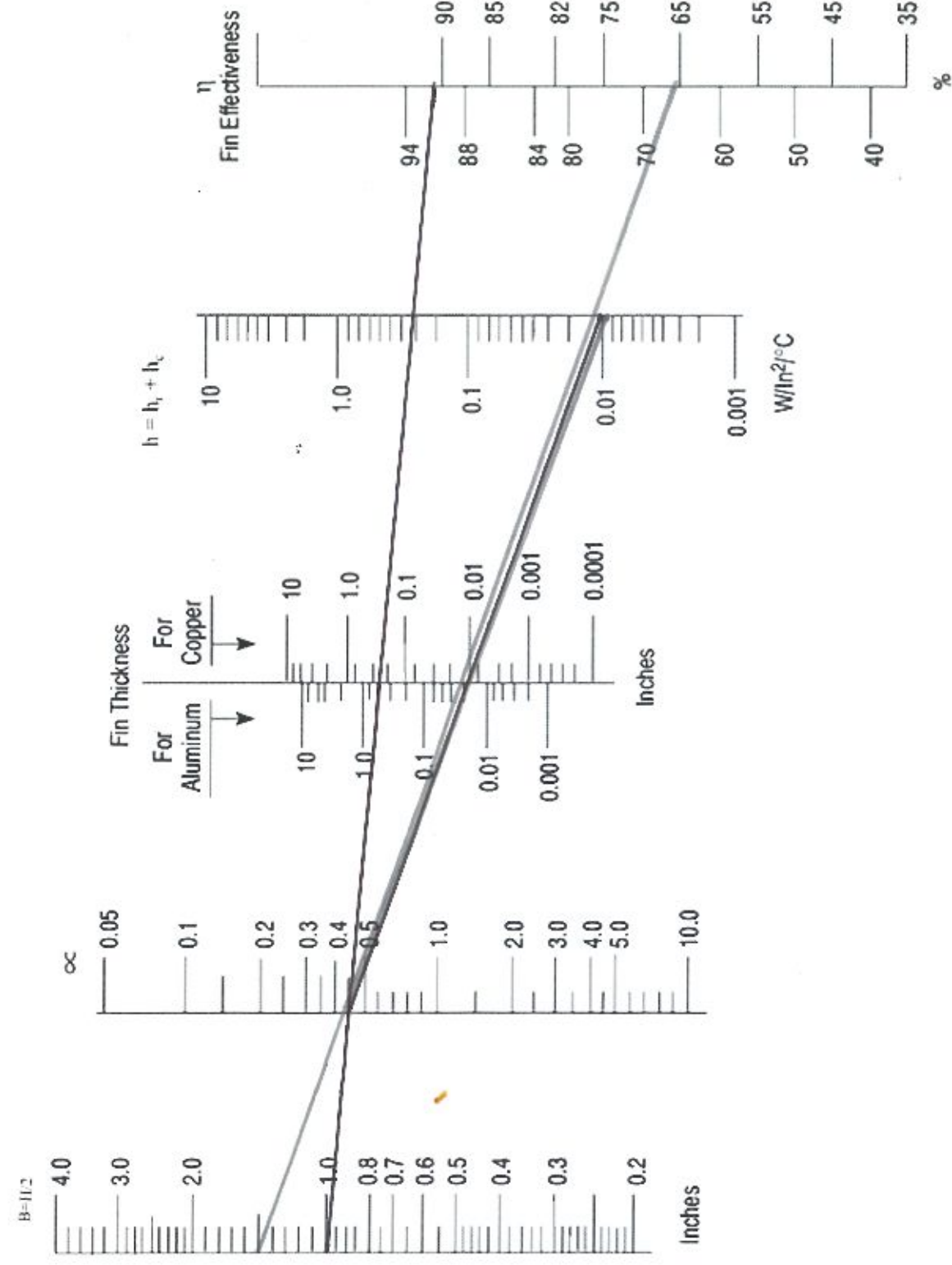
Quadrupling clock frequency reduced the time it takes for a metastable condition to be met.



$MTBF = \frac{e^{\frac{t_r}{T_0}}}{T_0 \times F \times a} \times k \left[\frac{e^{\frac{t_r}{T_0}}}{T_0 \times F} \right]$ $k = \text{number of additional flip flops}$

$= \frac{e^{\frac{42.3\text{ns}}{0.2\text{ns}}}}{9.6 \times 10^{-18} \times 80\text{M} \times 2\text{M}} \times 1 \left[\frac{e^{\frac{42.3}{0.2\text{ns}}}}{9.6 \times 10^{-18} \times 80\text{M}} \right] =$
 $= 4.644 \times 10^{94} \times ?$

Remove this page and insert into your answer booklet



$h = 2$
 $h = 3$



SURNAME: Payne

FORENAME(S): Kristian

12 Pages

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4. Write your answers in ink.
5. Begin each answer on a fresh page. Do all rough work in the answer book and cross it through.
6. No part of this book is to be torn out; it must be handed in complete.
7. If more books than one are used, fasten them together using the tags available from the invigilator(s).
8. **Every book must be handed in. In no circumstances may answer books, used or unused, be taken out of the examination venue.**

1	Student Number	1503517/1 ~~199283~~
2	Title of Examination Paper	Electronic design
3	Module Code	SGEE 6000
4	Date and Time of Examination	03/05/19 09:30
5	Examination Venue	Coleg Sir odr G24
6	Seat Number	3
7	Number of Answer Books handed in	

List the numbers of the questions you have attempted	Office Use
A	14
B1	19
B2	9
Total	42

(Gweler yr ochr arall am y fersiwn Cymraeg)



Prifysgol Cymru
University of Wales
Trinity Saint David

Llyfr Atebion Arholiadau

12 Tudalen

Cyfarwyddiadau i Ymgeiswyr

1. Rhwch yr holl wybodaeth y gofynnir amdant yn y blychau isod.
2. Rhwch eich enw yn y lle a ddarparwyd ar y dde, pwygch et a' i seil! I lawr (gan ddefnyddio'r label a ddarparwyd) i guddio'ch enw.

3. Rhaid i'r atebion fod mewn llawysgriflen ddarlennadwy. Gall yr Arholwyr naill ai anwybyddu sgrïpt annarllennadwy, neu drefnu iddi gael ei theipio a chael yr ymgeisydd i dalu.
4. Ysgrifennwch eich atebion mewn inc.
5. Dechreuwch bob ateb ar dudalen newydd. Gwnewch unrhyw fras nodiadau yn y llyfr atebion a thynnu llinell drwyddynt.
6. Ni ddylid rhwgo unrhyw ran o'r llyfr. hwn; rhaid ei gyflwyno yn gyfan.
7. Os defnyddir mwy nag un llyfr, rhwymwch hwy gyda'i gilydd gan ddefnyddio'r tagiau sydd ar gael oddi wrth y gwyllwtr/gwythwyr.
8. Rhaid dychwelyd pob llyfr. Ni chaniateir mynd â llyfrau atebion, wedi eu defnyddio neu heb eu defnyddio, allan o'r lleoliad arholi o dan unrhyw amgylchadau.

Rhesbwch ffau'r cwestigynau a ymgestlwyd	Cyflunswm
Af Ddlbenion y Swyddfa	

7	Nifer y Llyfrau Atebion a gyflwynwyd	
6	Rhif Sedd	
5	Lleoliad yr Arholiad	
4	Dyddiad ac Amser yr Arholiad	
3	Cod y Modwl	
2	Teitl y Papur Arholiad	
1	Rhif Myfyrwr	

(See the other side for English version)

Llenwch, plygwh a seliwh
(gweler nodyn 2 isod)

CYFENW:

ENW(AU) CYNTAF:

A1) A1) $R_S = ?$

$$V_{in} = 10V$$

$$V_Z = 2.5V$$

$$I_Z(\min) = 1.2mA$$

$$R_L = 1k \rightarrow 2k$$

$$R_{S_{max}} = \frac{V_{in} - V_Z}{I_{L_{max}} + I_{Z_{min}}} = \frac{10 - 2.5}{? + 1.2mA}$$

$$I_{L_{max}} = \frac{V_Z}{R_{L_{max}}} = \frac{2.5}{\frac{2000}{1000}} = 1.25 \times 10^{-3} A$$

$$R_{S_{max}} = \frac{10 - 2.5}{1.25 \times 10^{-3} + 1.2 \times 10^{-3}} = 3061 \Omega$$

A3) A Square Wave drives a Switching Circuit, ~~that~~ an Unregulated DC ~~out~~ input is converted to ~~an~~ high current, high frequency AC which is then converted ^{Back} to a Stable DC output.

A4) $P_D = 500mW$

$$\cancel{T_J = 100^\circ C} \quad T_J = 100^\circ C$$

$$\theta_{JA} = 180^\circ C/W$$

$$\theta_{CS} = 1.6^\circ C/W$$

$$\theta_{JC} = 2.5^\circ C/W$$

$$i) \cancel{T_J = T_A = T_J = 0.5 \times 180}$$

$$T_A = T_J - P_D \times \theta_{JA}$$

$$T_A = 100 - 0.5 \times 180$$

$$T_A = 10^\circ$$

Regulator can operate up to 10° without heatsink so would need a heatsink to operate at $22^\circ C$

A4)

ii)

$$P_D = 5W$$

$$T_0 = 100^\circ C$$

$$\theta_{JA} = 180^\circ C/W$$

$$\theta_{CS} = 1.6^\circ C/W$$

$$\theta_{JC} = 2.5^\circ C/W$$

$$T_A$$

$$\theta_{JA} = \frac{T_A - T_0}{P_D} - (\theta_{JC} + \theta_{CS})$$

$$\theta_{JA} = 100 -$$

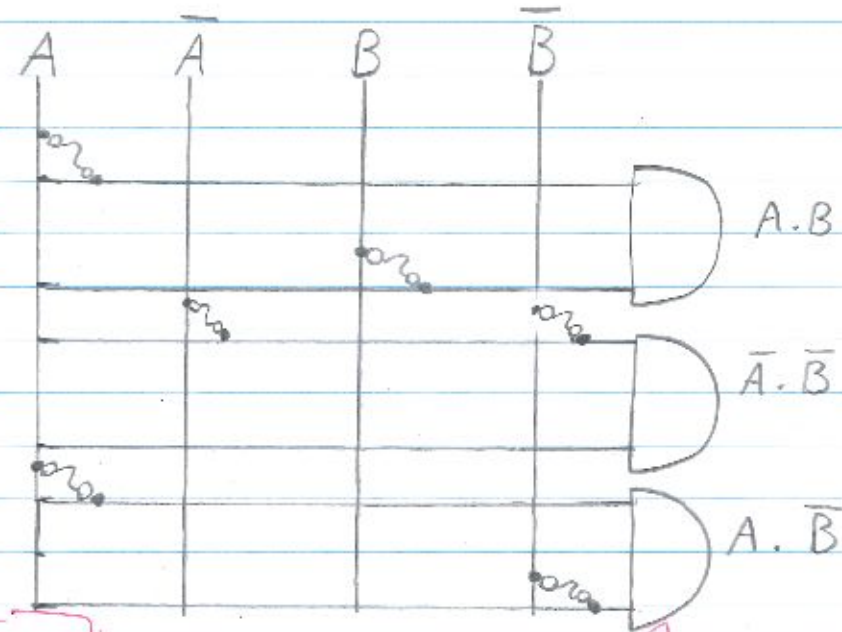
$$\frac{T_0 - T_A}{P_D} - (\theta_{JC} + \theta_{CS})$$

$$\theta_{JA} = \frac{100 - 22}{5} - (1.2 + 2.5) = 11.9^\circ C/W$$

An $11.9^\circ C/W$ heatsink is required

A6) JFET's input is reverse biased where bipolar transistor is forward biased

A7



A2 at end

Part A 14/40.

5

B1)

$$a) I_C = 1.2A$$

$$V_{out} = 6V$$

$$V_{in} = 15V$$

$$\beta = 50$$

$$V_{BE} = 0.6V$$

$$I_{ZM} = 5.6mA$$

$$i) V_Z = V_{out} - V_{BE}$$

$$V_Z = 6 - 0.6 = 5.4V$$

$$ii) R_S = \frac{V_{in} - V_Z}{I_B + I_Z}$$

$$I_B = \frac{I_C}{\beta} = \frac{1.2}{50} = 0.024A \approx 24 \times 10^{-3}A$$

$$R_S = \frac{15 - 5.4}{24 \times 10^{-3} + 5.6 \times 10^{-3}} = 324\Omega$$

B1)

c) $pD = 5$
 $T_A = 60^\circ\text{C}$
 $\epsilon = 0.7$
 $T_J = 130^\circ\text{C}$
 $\theta_{JC} = 2.5^\circ\text{C/W}$
 $\theta_{CS} = 1.6^\circ\text{C/W}$

$$\text{required } \theta_{SA} = \frac{T_J - T_A}{PD} - (\theta_{JC} + \theta_{CS})$$

$$\text{required } \theta_{SA} = \frac{130 - 60}{5} - (2.5 + 1.6) = 9.9^\circ\text{C/W}$$

$$T_S = T_J - (\theta_{JC} \times PD)$$

$$T_S = 130 - (2.5 \times 5) = 117.5$$

$$h_r = 1.47 \times 10^{-10} \times \epsilon \times \left(\frac{T_S + T_A}{2} + 273 \right)^3$$

$$h_r = 1.47 \times 10^{-10} \times 0.7 \times \left(\frac{117.5 + 60}{2} + 273 \right)^3$$

$$h_r = 4.67 \times 10^{-3} \text{ W/in}^2/^\circ\text{C}$$

3" HS

$$h_c = 2.21 \times 10^{-3} \times \left(\frac{T_S - T_A}{H} \right)^{\frac{1}{4}}$$

$$h_c = 2.21 \times 10^{-3} \times \left(\frac{117.5 - 60}{3} \right)^{\frac{1}{4}}$$

$$h_c = 4.81 \times 10^{-3} \text{ W/in}^2/^\circ\text{C}$$

$$h = h_c + h_r = 4.81 \times 10^{-3} + 4.67 \times 10^{-3} = 9.48 \times 10^{-3} \text{ W/in}^2/^\circ\text{C}$$

* From nomogram

$$\alpha = 0.45$$

$$B = H/2 \quad B = 1.5$$

$$\eta = 62.5\%$$

$$\theta_{SA} = \frac{1}{2 \times H^2 \times \eta \times h}$$

$$\theta_{SA} = \frac{1}{2 \times 3^2 \times 0.625 \times 9.48 \times 10^{-3}}$$

$$\theta_{SA} = 9.38^\circ\text{C/W}$$

2" HS

$$h_c = 2.21 \times 10^{-3} \left(\frac{T_S - T_A}{H} \right)^{\frac{1}{4}}$$

$$h_c = 2.21 \times 10^{-3} \left(\frac{117.5 - 50}{2} \right)^{\frac{1}{4}}$$

$$h_c = 2.21 \times 5.33 \times 10^{-3} \text{ W/in}^2/^\circ\text{C}$$

$$h = h_c + h_r = 5.33 \times 10^{-3} + 4.67 \times 10^{-3} = 10 \times 10^{-3}$$

* From nomogram

$$\alpha = 0.45$$

$$B = H/2 \quad B = 1$$

$$\eta = 91\%$$

$$\theta_{SA} = \frac{1}{2 \times H^2 \times \eta \times h}$$

$$\theta_{SA} = \frac{1}{2 \times 2^2 \times 0.91 \times 10 \times 10^{-3}}$$

$$\theta_{SA} = 13.74^\circ\text{C/W}$$

All method
 correct with
 carried error
 (used 50°C instead
 of 60°C)

13

- B1)
c) The 3" heat sink would be appropriate for the application as its θ_{SA} value is below the required θ_{SA} . The 3" heatsinks θ_{SA} value is above the required so it would not be suitable. ✓

B2)

- b) $I_D = 8\text{mA}$
 $I_{DSS} = 12\text{mA}$
 $V_{GS(0SS)} = -4.5\text{V}$
 $V_{GS}?$

$$I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_{GS(0SS)}} \right]^2$$

$$V_{GS} = V_{GS(0SS)} \times \left[1 - \sqrt{\frac{I_D}{I_{DSS}}} \right]$$

$$V_{GS} = -4.5 \times \left[1 - \sqrt{\frac{8 \times 10^{-3}}{12 \times 10^{-3}}} \right]$$

$$V_{GS} = -0.83\text{V} \quad \checkmark$$

B2)

- d) $f_{\text{clock}} = 20\text{MHz}$
 $a = 2\text{MHz}$
 $t_{\text{prop}} = 6.7 \times 10^{-9}$
 $\tau = 0.2 \times 10^{-9}$
 $t_0 = 9.6 \times 10^{-18}$
 $t_{\text{so}} = t_{\text{r}} + t_{\text{setup}} = 1 \times 10^{-9}$

$$t_r (\text{resolution time}) = t_{\text{clock}} - t_{\text{prop}} - t_{\text{setup}}$$

$$t_{\text{clock}} = \frac{1}{f_{\text{clock}}} = \frac{1}{20 \times 10^6} = 50 \times 10^{-9}$$

$$t_r = 50 \times 10^{-9} - 6.7 \times 10^{-9} - 1 \times 10^{-9} = 42.3 \times 10^{-9} \quad \checkmark \quad \checkmark$$

$$MTBF = \frac{e^{\frac{t_r}{\tau}}}{t_0 \times s \times a}$$

$$MTBF = \frac{e^{\frac{42.3 \times 10^{-9}}{0.2 \times 10^{-9}}}}{9.6 \times 10^{-18} \times 20 \times 10^6 \times 2 \times 10^6} \quad \checkmark \quad \checkmark$$

$$MTBF = 3.990222084 \times 10^{12} \text{ seconds} \quad \times$$

$$MTBF_{\text{years}} = \frac{MTBF}{2.3 \times 10^7} = 5.42 \times 10^5 \text{ years} \quad \times$$

$$MTBF_{\text{years}} = \frac{MTBF}{3.2 \times 10^7} = 124694.4 \text{ years} \quad \times$$

(2)

(2)

B2)

$$ii) f_{clock} = 80 \text{ MHz}$$

$$\alpha = 2 \text{ MHz}$$

$$t_{prop} = 6.7 \times 10^{-9}$$

$$\tau = 0.2 \times 10^{-9}$$

$$t_0 = 9.6 \times 10^{-18} \text{ s}$$

$$t_{setup} = 1 \times 10^{-9}$$

$$t_{clock} = \frac{1}{80 \times 10^6} = 12.5 \times 10^{-9}$$

$$\begin{aligned} t_{tr} &= t_{clock} - t_{prop} - t_{setup} \\ &= 12.5 \times 10^{-9} - 6.7 \times 10^{-9} - 1 \times 10^{-9} \\ &= 4.8 \times 10^{-9} \end{aligned}$$

$$MTBF = \frac{e^{\frac{t_r}{\tau}}}{t_0 \times \alpha \times \alpha}$$

$$MTBF = \frac{e^{\frac{4.8 \times 10^{-9}}{0.2 \times 10^{-9}}}}{9.6 \times 10^{-18} \times 80 \times 10^6 \times 2 \times 10^6}$$

$$MTBF = 0.05761597 \times 10^{29} \text{ seconds}$$

$$MTBF_{\text{years}} = \frac{MTBF}{3.2 \times 10^7} = 2.83 \times 10^{22}$$

Quadrupling the clock frequency increases the MTBF

9/30

A2) Voltage increase is off set.

As V_{out} increases, voltage across R_2 increases. this increases V_F which means more current enters into the base of Q_1 .

2

Remove this page and insert into your answer booklet

