



Complete, fold and seal
(see note 2 below)

SURNAME: Peppard

FORENAME(S): Samuel

Examination Answer Books

12 Pages

Instructions to Candidates

1. Please give the information requested in the boxes below
2. Enter your name in the space provided to the right, fold the flap and seal down (using the label provided) to hide your name
3. The answers must be legibly written. The Examiners cannot ignore illegible script or have it typed and the expense of typing charged to the candidate.
4. Write your answers in ink.
5. Begin each answer on a fresh page. Do all rough work in the answer book and cross it through.
6. No part of this book is to be torn out; it must be handed in complete.
7. If more books than one are used, fasten them together using the tags available from the invigilator(s).
8. Every book must be handed in. In no circumstances may answer books, used or unused, be taken out of the examination venue.

1	Student Number	2308344
2	Title of Examination Paper	Micros, Peripherals and Interfaces
3	Module Code	ALDA 4004
4	Date and Time of Examination	8/1/2025 9:00
5	Examination Venue	310
6	Seat Number	005
7	Number of Answer Books handed in	1

List the numbers of the questions you have attempted	Office Use
1	6 1/2
2	0
3	1 1/2
4	10
5	9
6	1
	28
	x 2
Total	56 1/2

6 1/2

0

1 1/2

10

9

1

28

1) a) Return - Return back to different part of code
 - Return Back from code to the main Section

1 1/2 1 1/2

b) Sleep - Pause and stay on standby
 - tells the chip to turn off

1 1/2 1 1/2

c) ADDLW - Add Literal ^{and} ~~to~~ Working register
 - Add the value of Literal to the value of the Working Register

1 1/2

d) BCFSS, b - BCF - Begin Count Function
 - Count from number f to number b

x x

0

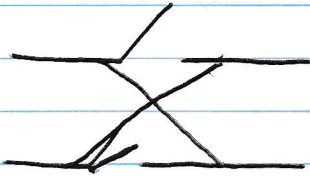
e) ~~DEC~~ DECF - Decrement the File register
 - ~~So~~ Decrement the File register by a value of 1

2

2

6 1/2

2)

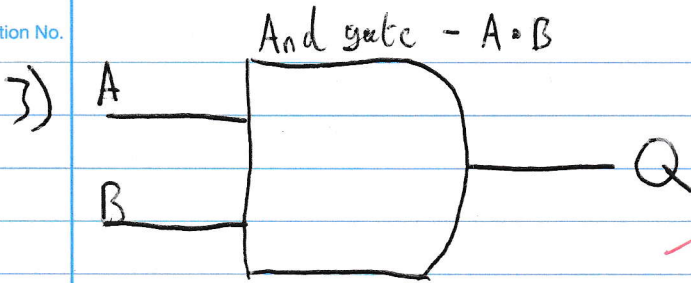


• Switch Bounce can be reduced by ensuring the switch is

+

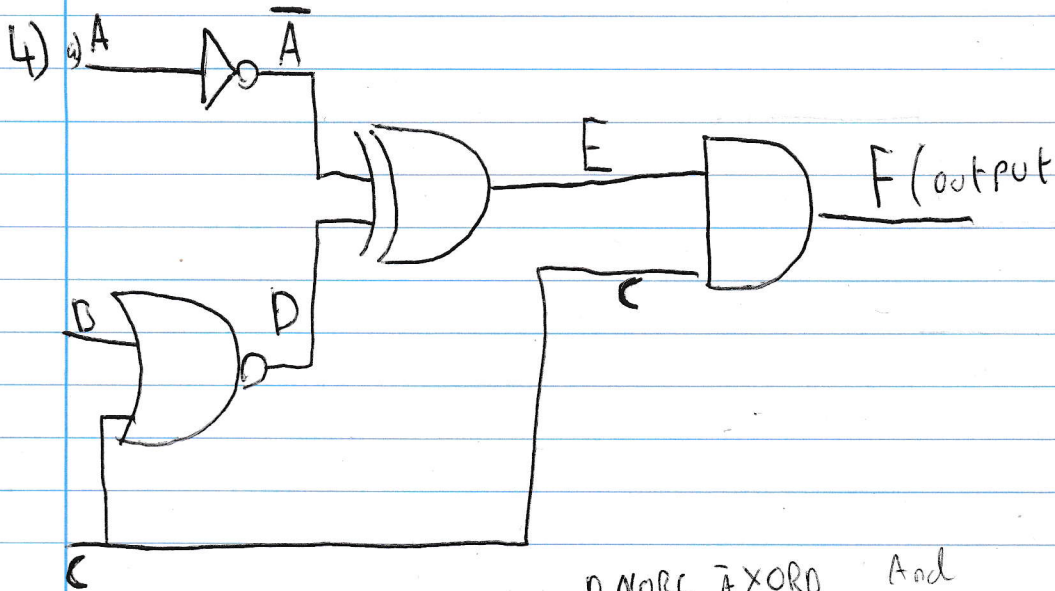
x

o



Q	A	B
0	0	0
0	0	1
0	1	0
1	1	1

 $1\frac{1}{2}$ $1\frac{1}{2}$



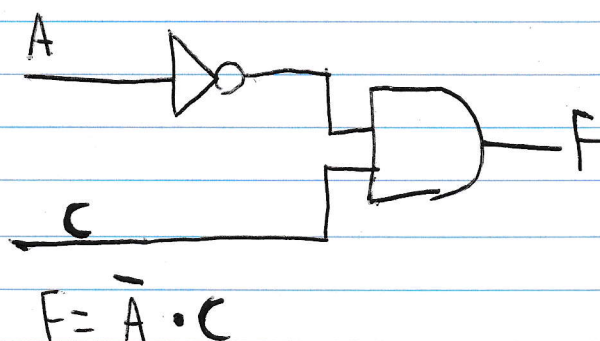
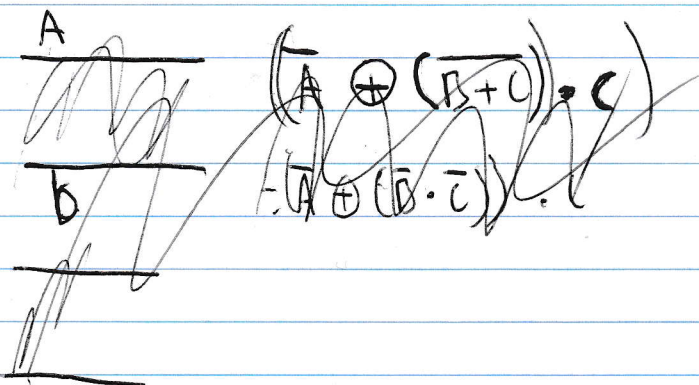
or

0	0	0
0	1	1
1	0	1
1	1	1

A	B	C	$\bar{A}$	D NORC	E $\bar{A} \times \text{OR} D$	F And
0	0	0	1	1	0	0
0	0	1	1	0	1	1
0	1	0	1	0	1	0
0	1	1	1	0	1	1
1	0	0	0	1	1	0
1	0	1	0	0	0	0
1	1	0	0	0	0	0
1	1	1	0	0	0	0

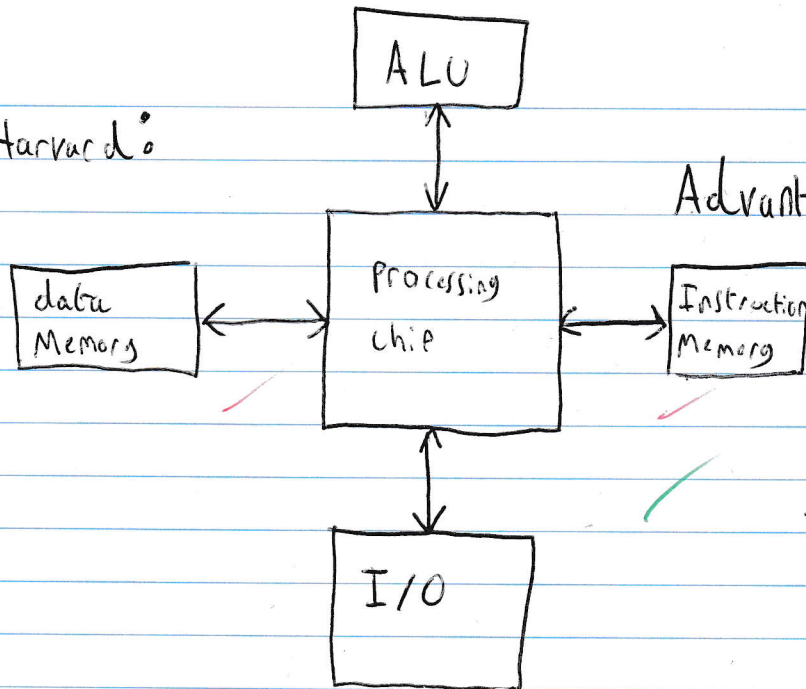
b)

A	B	C	F
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0



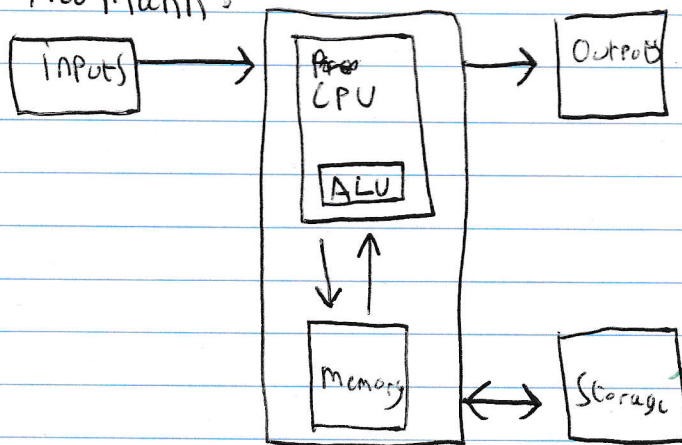
10

5) Harvard:



Advantage: 2 buses for ~~separate~~ data and instruction which therefore allows for simultaneous flow of info
- stopping bottleneck issue

Von Neumann:



Advantage: - ~~More~~ cheaper and simpler which makes it more accessible

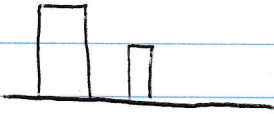
Harvard

- 2 buses for instruction and data - Allows for faster flow of data and simultaneous flow

Von Neumann

- One bus - causes bottlenecking issues
- Much

6) PWM - Pulse Width Modulation DAC - Digital - Analog Converter



- You can use PWM to create a ~~digital~~ DAC by altering the width of the pulses
- This therefore can mimic an analog system
- if you constantly push out a pulse with minimal width it can create an analog ~~for~~ signal

