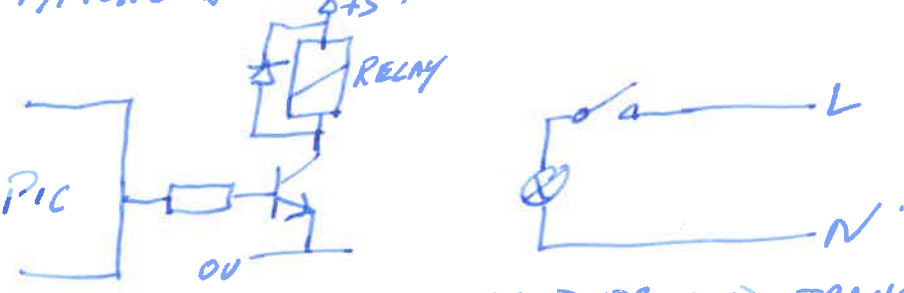
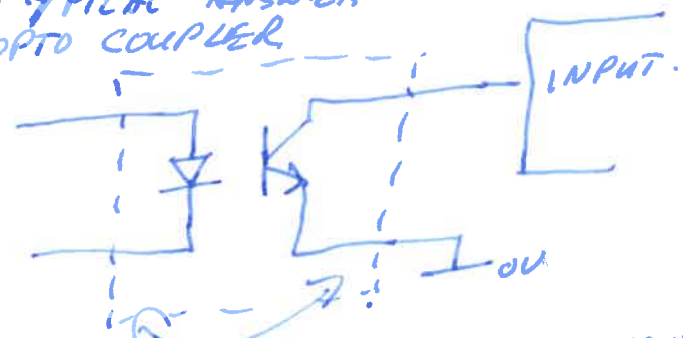
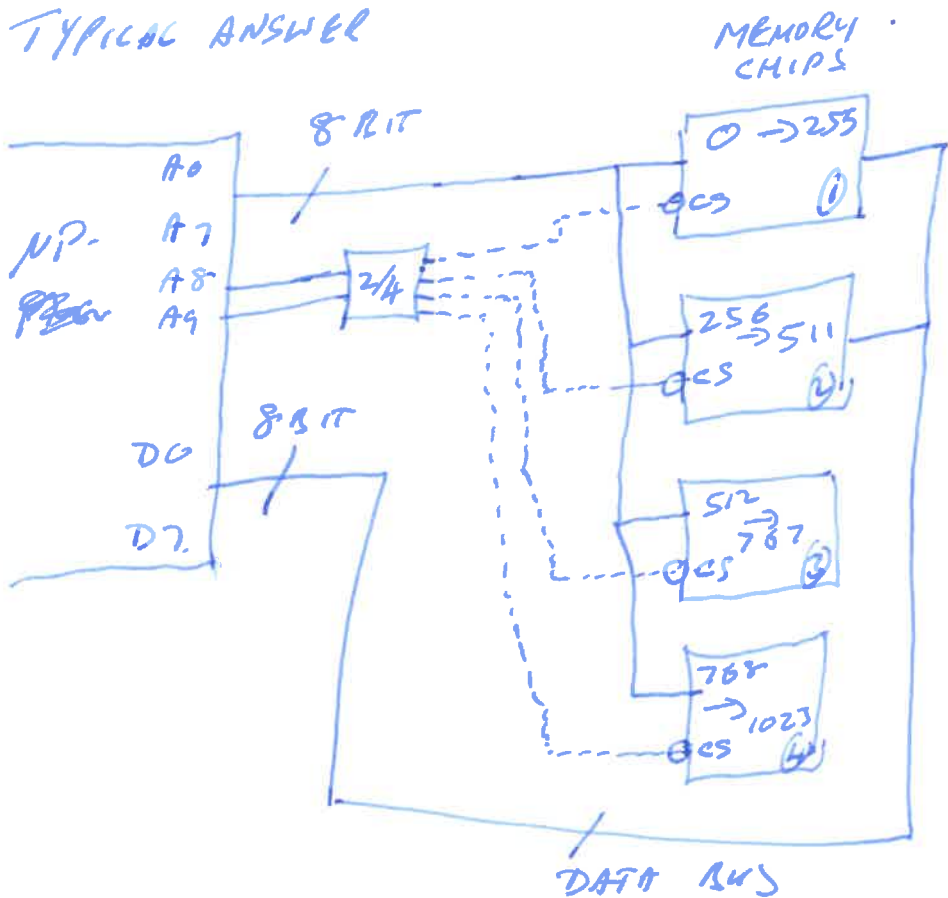
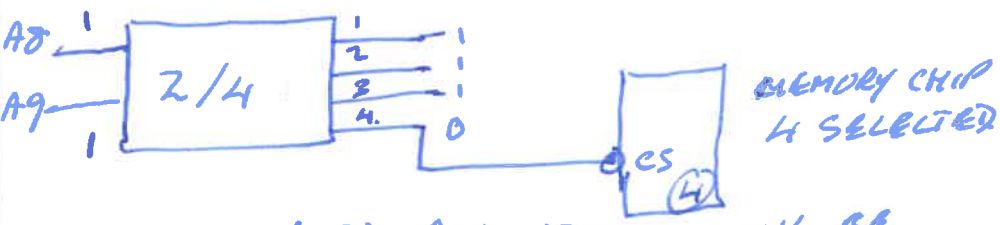
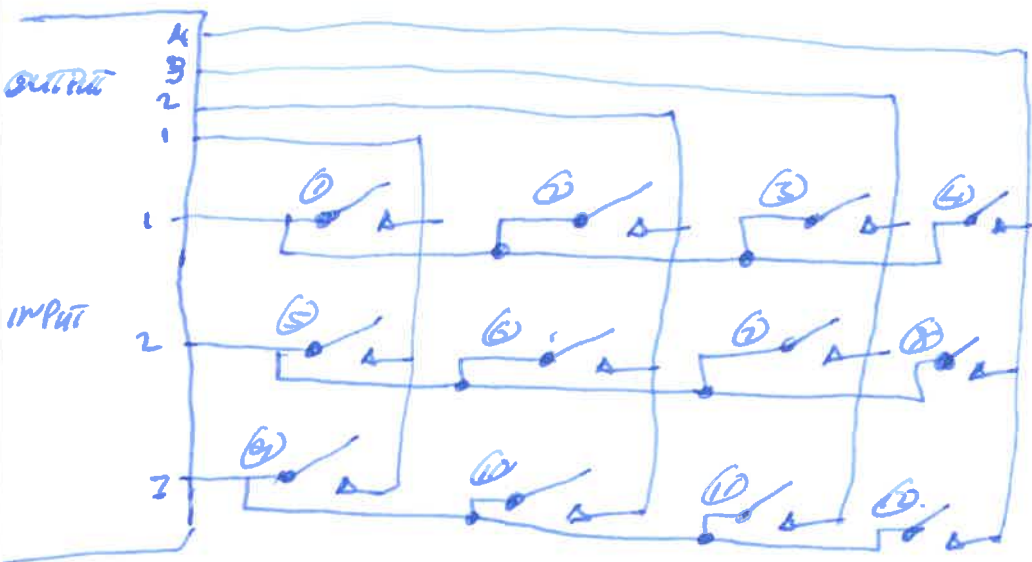
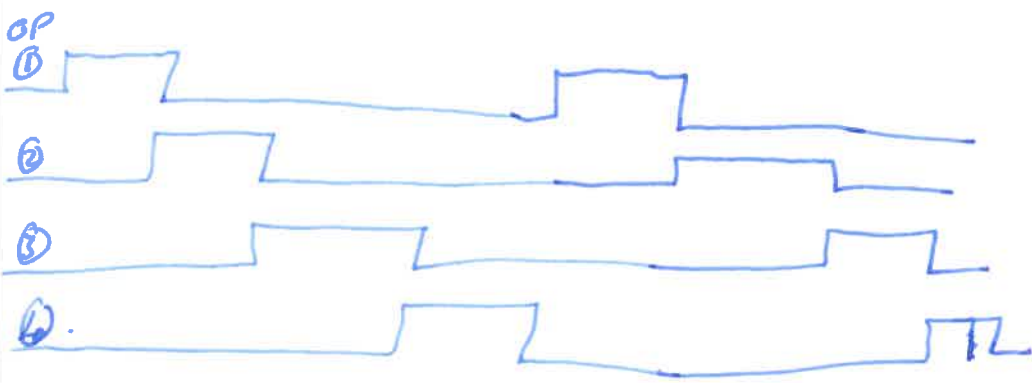


Question		marks
Q1 a)	<pre> MOVLW 0X7B MOVWF POST1 MOVLW 0X96 ADDWF POST1,1 </pre> $C = 1$ $DC = 1$ $Z = 0$ $OE = 00010001$ POST1 W. X 01111011 01111011 01111011 01111011 10010110 01111011 10010110 100010001	(1) (1) (1)
b)	<pre> MOVLW 0X4C MOVWF DATA1 RLF DATA1 INCF DATA1 RLF DATA1 INCF DATA1 </pre> $C = 1$ $DATA1 = 00110011$ DATA1 W 01001100 " 01001100 01001100 01001100 100110010 100110011	(1) (1) (1)
c)	<pre> COUNT1 EQU 0X12 → 0X12. LOOP. MOVLW 0X6 → MOVLW 0X05 MOVWF COUNT1 → MOVWF COUNT1 CALL DELAY1 → LOOP CALL DELAY1 DECF COUNT1 → DECF COUNT1 GOTO LOOP → GOTO LOOP. NOP → NOP NOP → NOP </pre>	(1) (1) (2)

Question		marks
2 (a).	EXPECT. KEY POINTS SUCH AS •) SUBROUTINES ARE USED ~~THROUGH~~ FREQUENTLY USED SECTIONS OF CODE - E.G. DELAYS. •) MINIMISE CODE •) SIMPLIFY CODE FOR TESTING. •) ~~MODIFIERS~~ CALLED FROM WITHIN MAIN BODY OF CODE. - PREDICTABLE.	(3)
b).	KEY POINTS E.G. •) USED FOR CODE THAT MUST BE SERVICED DUE TO TIME RESTRAINTS. •) EXTERNAL EVENTS CAUSE INTERRUPTS •) NOT PREDICTABLE. •) INTERNAL CLOCK MAY CAUSE INTERRUPTS •) <u>INTERRUPT VECTOR AT 0X000E.</u>	(3)
c).	FOR SUBROUTINES STACK HOLDS P.C FOR <u>INTERRUPTS STACK HOLDS P.C.</u>	(2)
d).	MAY WISH TO STORE W REG, + STATUS REG. ETC IN SW STACK IN CASE OF INTERRUPTS DUE TO ASYNCH. CALLS. USE RETFIE - <u>NOT RETURN.</u>	(2)
e).		

Question		marks
Q3. a)	KEY POINT IS A 16F84A IS A D.C. DEVICE WITH NO A.C. CAPABILITY.	(1)
b)	TYPICAL ANSWER +5.  MUST INCLUDE DIODE AND TRANSISTOR. - OTHER SOLUTIONS MAY BE ACCEPTED - Eg THYRISTOR.	(3)
c)	KEY POINTS ARE SWITCH BOUNCE AND NEED TO READ SWITCH AT LEAST TWICE WITH SHORT DELAY TO ALLOW SWITCH CONTACTS TO SETTLE 	(3)
d)	TYPICAL ANSWER OPTO COUPLER  NO ELECTRICAL CONNECTION OTHER DEVICES MAY BE ACCEPTABLE.	(3)

Question		marks
Q1 a)	TYPICAL ANSWER  MEMORY CHIPS 0 → 255 (chip 1) 256 → 511 (chip 2) 512 → 767 (chip 3) 768 → 1023 (chip 4) DATA BUS MUST SHOW ACTIVE LOW CHIP SELECT. 2 → 4 DECODER - CORRECT MEMORY ADDRESSES. - COMMON 8 BIT ADDRESS BUS - TRI STATE OUTPUTS ON MEMORY b). MEMORY LOCATION 810 WILL BE IN CHIP. 4. BINARY EQUIVALENT = $\overline{11} \overline{00101010}$  CHIP 4 ENABLED ALL OTHERS WILL BE TRI-STATE → HIGH IMPEDANCE	(5) (5)

Question		marks
Q5a)	<u>TYPICAL ANSWER</u>  Switches are connected in 3x4 MATRIX. (4x3 ALSO OK). 4 PINS ARE USED FOR PRODUCING A SCANNING OUTPUT SIGNAL. 3 INPUTS USED FOR READING SWITCH STATE  EACH COLUMN IS SCANNED IN TURN. AN ACTIVE ROW INDICATES SWITCH PRESSED [NOT NECESSARY TO SHOW PULL DOWN RESISTORS (OR PULL UP IF OTHER SOLUTION PROPOSED. OR DIODES IN CASE OF 2 SWITCHES PRESSED)]	5

Question		marks
Q5b)	SOLUTION SHOULD DESCRIBE SCANNING SEQUENCE WITH 1 SWITCH PRESSED. COULD ALSO MENTION DEBOUNCE. ANSWER WILL DEPEND ON ACTUAL PROPOSED CIRCUIT. BUT MUST BE CONSISTENT.	(5).
Q6.	P.C IS AT LOCATION 0X20 SO WE ARE PROCESSING COMMAND AT 0X15 IE GOTO 0X08. - LOCATION 0X22 HAS 0X1 SO NEXT INSTRUCTION: - ADDP <pre> LOOP. NOP. MOVF 0X22, W. ADDWF PCL, F GOTO 0X16 STATE2 NOP. NOP. MOVLW 0X3. MOVWF 0X22. GOTO 0X08. LOOP NOP. MOV 0X22, W ADDWF PCL, F GOTO 0X20 STATE4 NOP NOP. DELFSZ 0X20, F </pre> PL 00 0A W HAS 01 0C ← OFFSET 0D. ADDED TO PCL. — 022 HAS 03. W HAS 03 PCL HAS 0X0E 0X20 HAS 0X03. KEY POINTS ARE ADDING OFFSET TO PCL. PCL POINTS TO NEXT INSTRUCTION. (BUT GOTO OVERRIDES). CORRECT MEMORY LOCATIONS USED.	(10).