

Assignment 2

by Joseff Jones

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HND Electrical and Electronic Engineering

PSDE5029 – Virtual Instrumentation and
Control Systems
Assignment 2 – NI LabVIEW Magnitude
Comparator

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1. Introduction

This assignment involved using LabVIEW software to interface to an FPGA via the NI ELVIS II board to give a digital magnitude comparison between two 8-bit digital signals which will indicate whether the comparison is less than, equal to or greater than a set value. The first 8-bit signal is to be obtained from an analogue input ranging from 0-5V, which is used to represent a load applied to a load cell which will then be converted to the desired 8-bit digital signal. The second 8-bit signal will be a value set in grams from 0-1000gms and will then be converted to an 8-bit value to be output to the FPGA via the NI ELVIS II board.

Also, an 8-bit magnitude comparator would be designed, simulated and tested practically on the Nexys 4 DDR FPGA board which will compare two 8-bit set values, which are set using switches. These will be output onto LEDs which will indicate whether the comparison is greater than, equal to or less than.

The LabVIEW design would be adapted to allow data logging of the load cell input to LabVIEW and comparison outputs over a specified time period.

The figure below is the block diagram of the finished design from the assignment brief.

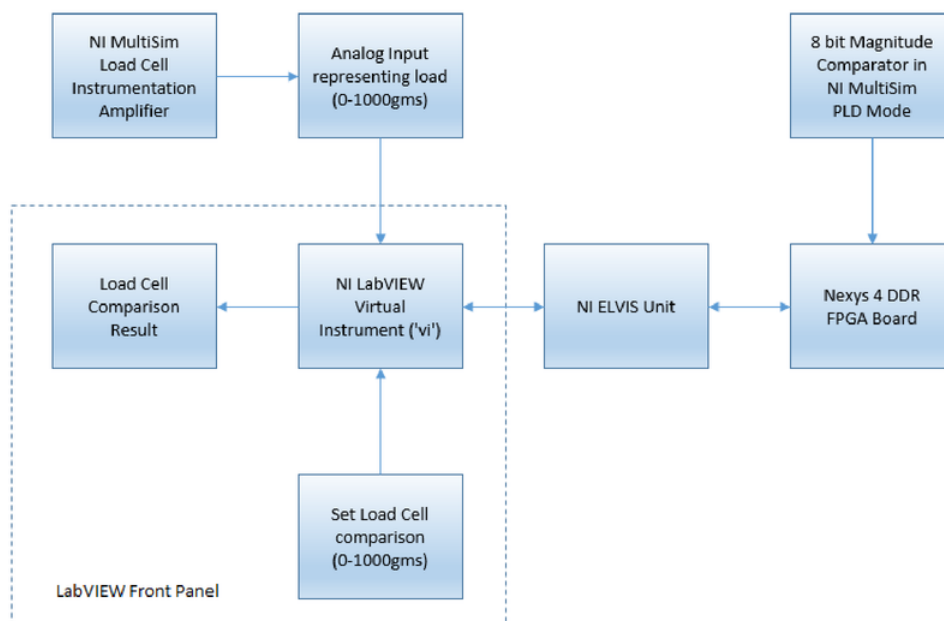


Figure 1 - Block Diagram of Finished Design

Good detailed introduction

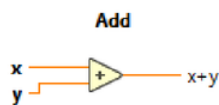
2. Research

Research was carried out into a number of topic areas in order to gain relevant knowledge to tackle and comprehend the tasks of the assignment, the findings of the research are shown in the sections below.

2.1 - NI DAQmx data acquisition icons used in LabVIEW

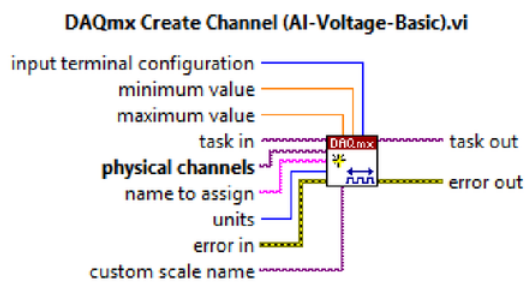
NI DAQmx data acquisition icons are the icons used in LabVIEW which are basically visual representations of functions; they are a toolset for developing programs. Below is a list of the most common data acquisition icons.

Add



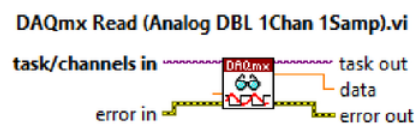
The add icon takes a number of inputs and sums them together.

Analogue Input Voltage



The analogue input voltage icon is used to measure voltage. External excitation can be used to scale the voltage using the AI custom voltage.

Analogue Read



The analogue read icon reads a value from an input task. The input must be a single analogue input and doesn't need to be an integer.

Clear

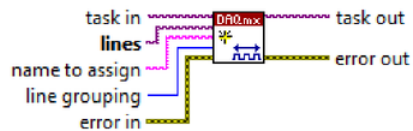
DAQmx Clear Task.vi



The clear icon is used for clearing the task. Before doing this, it releases any useful resources that the task reserved.

Digital Input

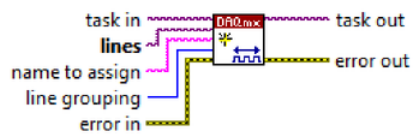
DAQmx Create Channel (DI-Digital Input).vi



Similarly to the analogue input, the digital input just measures a digital signal. This icon has multiple parameters – digital lines can be separated into multiple channels or combined into a single channel.

Digital Output

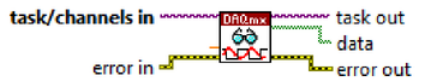
DAQmx Create Channel (DO-Digital Output).vi



Like the digital input, but for outputs. The digital output can create single channels or multiple channels.

Digital Read

DAQmx Read (Digital 1D Bool 1Chan 1Samp).vi



The digital read icon reads arrays of Boolean values from single digital input channels.

Error Out



Error out is used to provide standard error information.

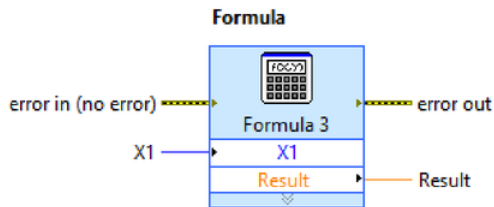
Feedback Node

Feedback Node



The feedback node stores data from one loop iteration or VI execution to the next.

Formula



The formula icon is used to create utilize calculations wherever they may be needed. Most mathematical functions that can be performed on a scientific calculator can also be performed on the formula icon.

Number to Boolean

Number To Boolean Array



The number to Boolean array converts a number to a Boolean array. The Boolean array that is produced will either be an array of 8, 16, 32 or 64, varying with the amount of bits in the integer.

Round to Nearest

Round To Nearest



As its name suggests, this icon rounds float values to an integer value. If the input is between two integers, it returns the nearest even integer.

Wait

Wait Until Next ms Multiple



The wait icon is used to synchronize function by waiting until the value of the timer becomes a multiple of a pre-designated millisecond multiple.

While Loop

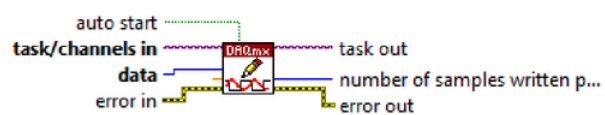
While Loop



The while loop contains circuits or perhaps specific components that need to be repeatedly scanned until a specific condition occurs.

Write

DAQmx Write (Digital U32 1Chan 1Samp).vi



The write icon writes a 32-bit unsigned integer (from -2147483648 to 2147483647) that contains a single digital output channel.

*Good, comprehensive research carried out on the LabVIEW
DAQmx icons used within the assignment*

2.2 - Digital Magnitude Comparators

Magnitude comparators are devices that can compare the magnitude of any two binary words; once compared, the magnitude comparator can then deem whether one binary word is greater than the other, less than the other, or equal to the other. Digital magnitude comparators are found in many places in technology such as microcontrollers and central processing units, and even gates such as the XNOR gate, which is a very basic comparator itself as it only produces a positive output if both of its inputs are equal.

To give an example of digital magnitude comparators, a 1-bit digital magnitude comparator will be explained. Below is a 1-bit digital magnitude comparator circuit (obtained from f-alpha.net).

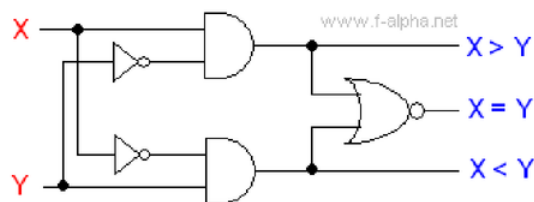


Figure 2 - 1-Bit Digital Magnitude Comparator

The operation of this comparator can be derived from the following truth table.

Inputs		Outputs			
B	A	A>B	A=B	A<B	
0	0	0	1	0	
0	1	1	0	0	
1	0	0	0	1	
1	1	0	1	0	

From the truth table, it can be seen that $A=B$ is 1 at two points – when A and B are 0, and when A and B are 1. This truth table is important because it exemplifies the fundamental characteristics of a digital magnitude comparator, the behaviour can be carried over to much larger-scale digital magnitude comparators by cascading together a number of these to produce n-bit comparators, which can handle multiple words of binary values at a time and compare them. An example of this can be seen in the 4-bit digital magnitude comparator made up of gates in the figure on the next page.

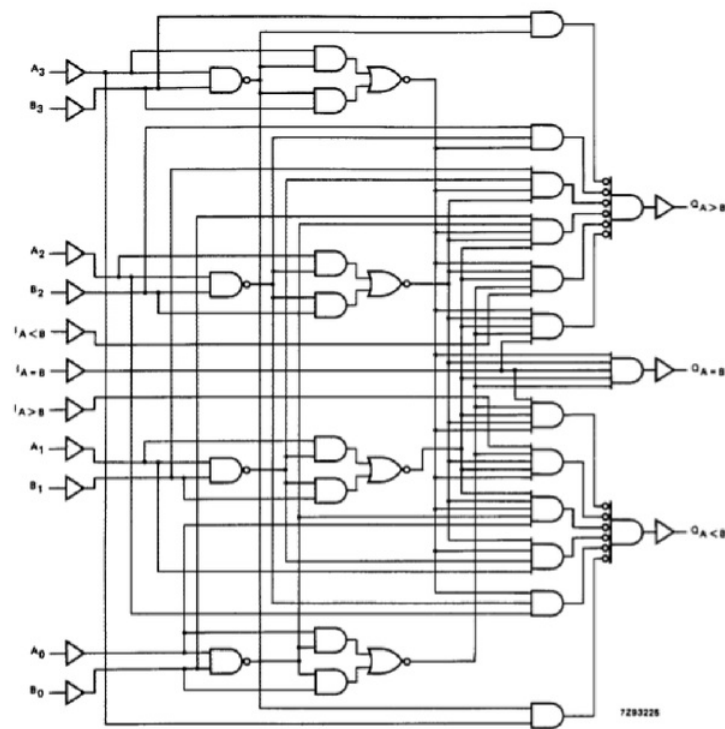


Figure 3 - 4-bit Magnitude Comparator using Logic Gates

The above figure was obtained from the official 74HC/HCT85 data sheet, which is a 4-bit magnitude comparator. As can be seen n-bit magnitude comparators can get quite big, but n-bit magnitude comparators themselves to produce even bigger magnitude comparators – an example of this can be seen from the figure below where three 4-bit magnitude comparators are cascaded to produce a 12-bit magnitude comparator, again found from the official 74HC/HCT85 data sheet.

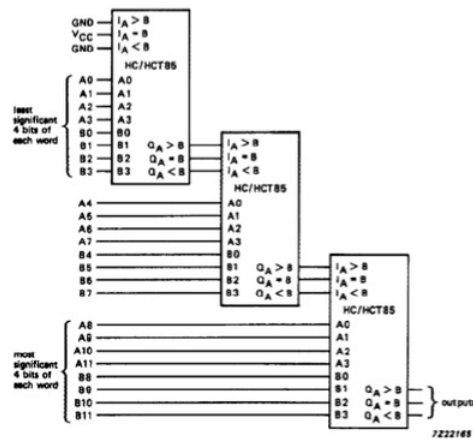


Figure 4 - 12-bit Magnitude Comparator Using Cascading 4-bit Magnitude Comparators

Good understanding shown on how a magnitude comparator functions

2.3 - Analogue to Digital Converters

Analogue-to-digital converters (ADCs) come in several different types, some of the most common types are sub-ranging, sigma-delta, successive approximation, integrating, sigma-delta and flash. There are many different types because there is a trade-off between sample-rate (speed, essentially) and resolution. Different applications have different needs – for example, radio-frequency test equipment typically use sub-ranging ADCs even though flash ADCs are faster, because sub-ranging ADCs have much better resolution which is invaluable in RF test equipment. A graph of the resolution of the mentioned ADCs versus their sample-rate is shown in the figure below and was obtained from www.edn.com.

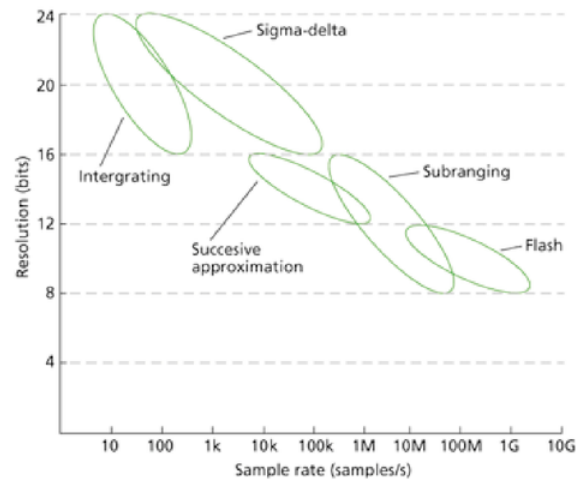


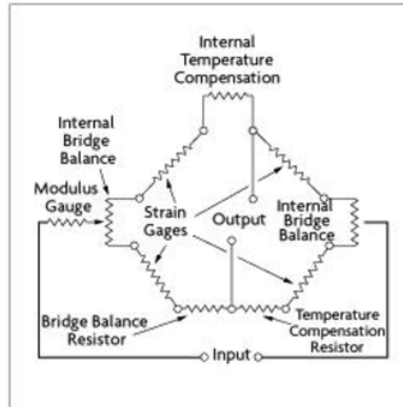
Figure 5 - Resolution Versus Sample Rate in ADCs

The fastest of ADCs, the flash ADC, are most suitable for applications that utilize large bandwidths and generally aren't used if it can be helped – this is because they consume large amount of power, have low resolution and are expensive (although are decreasing in price as technology advances and comparators become more and more mass-produced). They are made by cascading highly efficient comparators – the amount of comparators in the circuit depends on the amount of bits that the ADC is converting; for an 8-bit converter, the circuit would employ 2^8-1 comparators, for a 16-bit converter, the circuit would employ $2^{16}-1$ comparators etc. which is why the bigger the flash ADC the more exponentially expensive and power-hungry it is. A typical application of flash ADCs would be satellite communication and radar processing.

Limited research carried out

2.4 - Load Cells (namely LCKD-1Kg)

Load cells are a type of transducer that convert force (typically weight) into an electrical signal. The LCKD series are “designed to measure load ranges from 1kg to 1000lbs” (Subminiature Load Cell LCKD Series Rugged Industrial Design, 2018) and are a type of strain-gauge. Strain-gauge based load-cells are the most common type, and are developed using a Wheatstone-bridge circuit. An example of this circuit is shown below (obtained from omega.com).



Good

Figure 6 - Wheatstone-Bridge Strain-Gauge

Strain-gauge load cells are bonded to a structure that deforms when weight is applied to it. As can be seen in the figure above, four strain-gauges are often used together to obtain accurate values and maximum-sensitivity while also providing compensation for changes from temperature. Two of the four strain-gauges are usually there for tension, and the other two for compression. When weight is applied, the strain-gauge will compress and the electrical resistance of the circuit will increase with proportion to the load.

Good detail but could have been further researched

3. Design of Assignment Requirements

The assignment involved designing a magnitude comparator on Multisim, a signal conditioning circuit on Multisim and a LabVIEW circuit. The design process for these circuits are shown in the sections on the following pages (sections 3.1, 3.2 and 3.3).

3.1 – Magnitude Comparator on Multisim

Designing the magnitude comparator on Multisim involved using two comparators, a number of switches, a number of LEDs and three digital inputs (0,1,0). The resulting circuit is shown below.

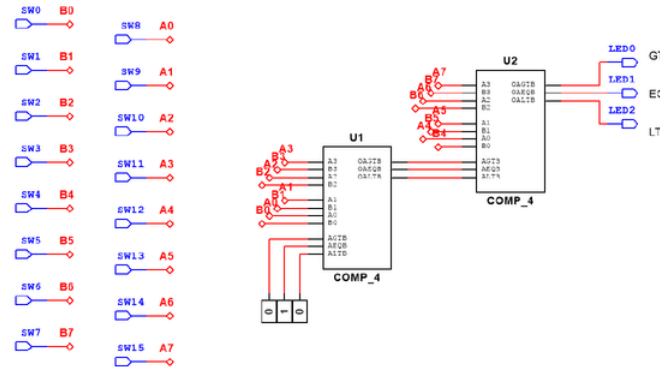


Figure 7 - Magnitude Comparator Design

The comparators are there to compare the switch inputs from A0-A7 and B0-B7, the LEDs are there to indicate whether A is equal to B, A is greater than B, or A is less than B. The digital inputs are there to keep the circuit functioning in stable manner. The on-page connectors shown in red are there to indicate where connections are made – A0-A3 and B0-B3 are connected to the U1 comparator and A4-A7 and B4-B7 are connected to the U2 comparator. The above circuit was used when uploading the magnitude comparator to the Nexys 4 board. When simulating the circuit, the switches and LEDs could not be used as they did not have any simulative functionality as they were; to rectify this, the circuit was altered. The altered circuit for simulation can be seen in the figure below.

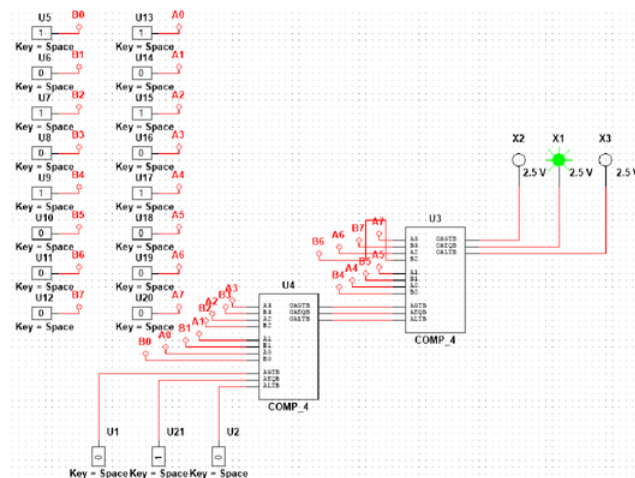


Figure 8 - Magnitude Comparator Multisim Design

The switches were replaced with digital inputs which either represent a 1 or a 0 signal and the LEDs were replaced by indicators which would either light up amber, green or red depending on whether A was greater than B, A was equal to B, or A was less than B, respectively.

When uploading the magnitude comparator to the NI ELVIS II board, the circuit was altered further. The switches and indicators were switched to Pmod connections, where switches were labelled “JA” and “JB” and LEDs were labelled “JC”. This can be seen in the figure below.

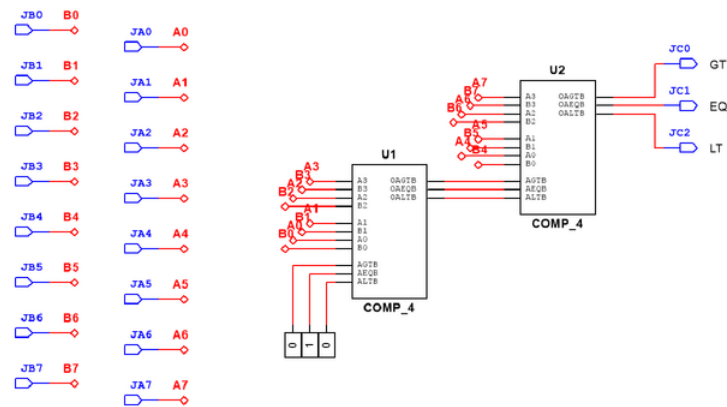


Figure 9 - Magnitude Comparator with Pmod Connectors

When connecting to the NI ELVIS II board, the Pmod JA, JB and JC pinout is shown in the figure below.

4	3	2	1	0
9	8	7	6	5

Figure 10 - NI ELVIS II JA, JB and JC Pinout

[Very good detail on the design of the magnitude comparator in MultiSim simulation and downloading to the FPGA](#)

3.2 – Signal Conditioning Circuit on Multisim

The circuit for the signal conditioner can be seen in the figure below.

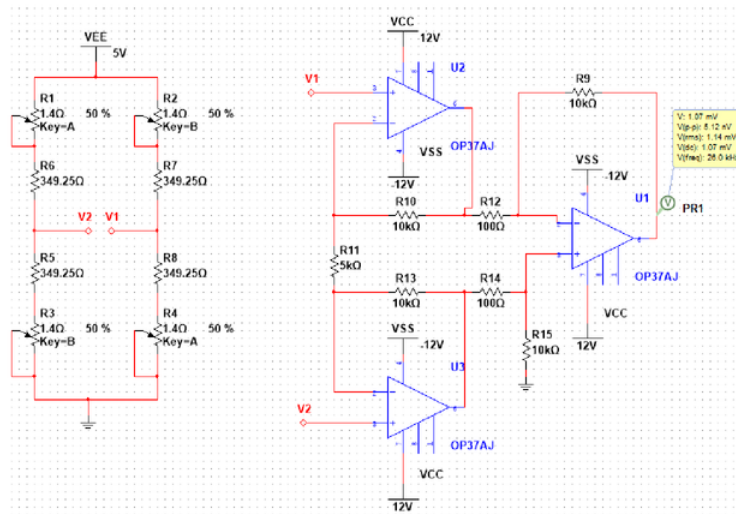


Figure 11 - Signal Conditioning Circuit Design

The signal conditioning circuit was designed on Multisim which could be used to convert a load into a proportional voltage, which could be analysed to easily read the size of the load. The left part of the circuit contains the load cell and the right part contains the instrumentation amplifier. The load cell part of the circuit was designed using a 5V VEE input which would split through to a pair of potentiometers, a pair of resistors, V1 and V2, another pair of resistors and another pair of potentiometers.

The instrumentation amplifier part of the circuit was designed by following the basic schematic for an instrumentation amplifier and altering the values to accommodate the desired output. The basic schematic for an instrumentation amplifier is shown in the figure below.

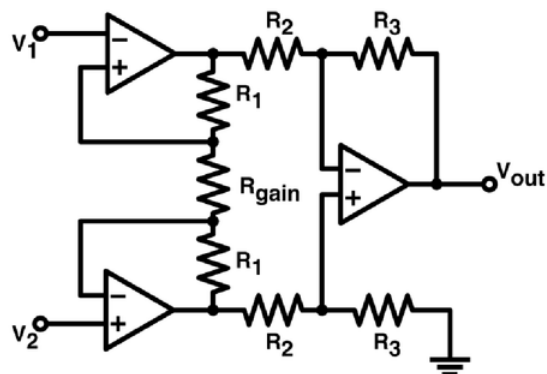


Figure 12 - Instrumentation Amplifier Basic Schematic from allaboutcircuits.com

In order to produce the desired output, an equation was used to determine the correct values that would result in the desired gain value of 500, the equation is:

$$Gain = (1 + 2 \frac{R_1}{R_{gain}}) * \frac{R_3}{R_2}$$

Where in the Multisim circuit Rgain was 5kΩ, R1 was 10kΩ, R2 was 100Ω and R3 was 10kΩ, the produced gain was:

$$Gain = (1 + 2 (\frac{10}{5}) * \frac{10000}{100}) = 500$$

The gain needed to be 500 because 500 was a sufficient value to amplify the voltage by as it was quite a small value being put into the circuit.

Quite a small value? The actual designed value was 10mV @ full load (1000gms) hence the reason for the gain of 500 to give 0-5V over 0-1000gms

3.3 – LabVIEW Circuit

The LabVIEW circuit was designed to encompass both of the previous circuits into one whole circuit - its function is to interface to an FPGA via the NI ELVIS II board to compare two 8-bit outputs and to indicate whether the comparison is equal to, less than or more than; therefore, it is both a magnitude comparator and a signal conditioner. The circuit takes an analogue input signal in the range of 0-5V which is used to represent a load applied to an LCKD-1Kg load cell; this load is then converted to an 8-bit signal and then be output to the FPGA via the NI ELVIS II board. The circuit then takes another signal which is a set value in LabVIEW in the range of 0-1000gms, this value is also converted to an 8-bit digital signal, to be compared to the analogue input signal. The finished LabVIEW circuit can be seen in the figure below.

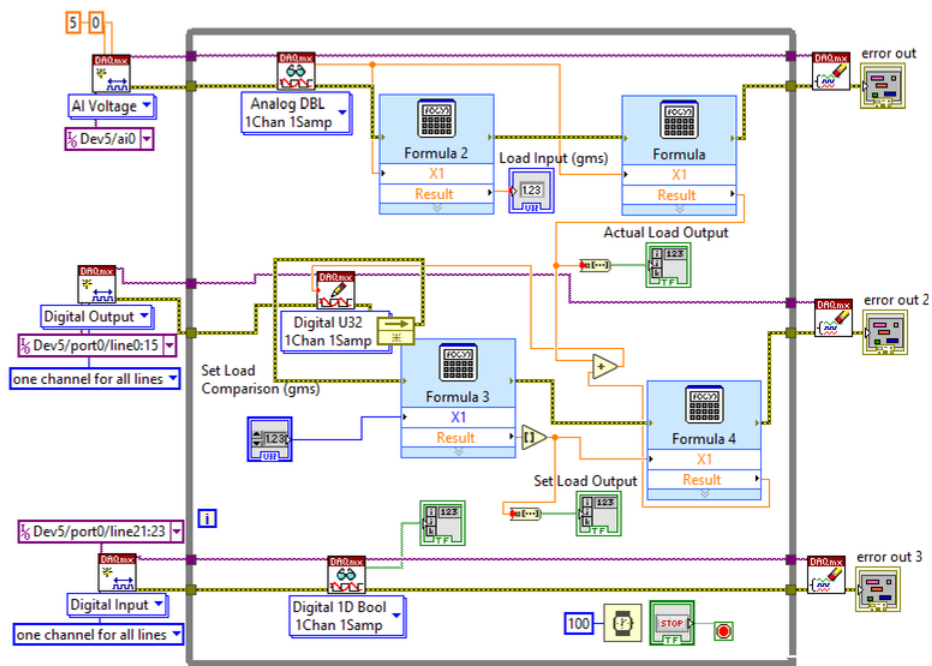


Figure 13 - Design of LabVIEW Circuit

In order to explain the LabVIEW design, the next few figures show parts of the design and beneath them is an explanation of each part and where it fits into the design.

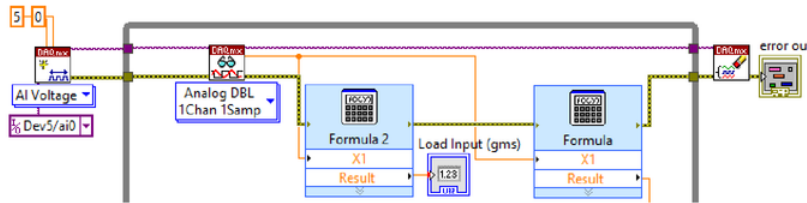


Figure 14 – Explanation of Design of LabVIEW Circuit (1/5)

The leftmost icon is the analogue input voltage – the two values connected in orange are the minimum and maximum values, 0 to 5. The “AI Voltage” is simply the units to be measured, and the purple box below it is the name of the custom scale, which is the connection to the ELVIS II board.

The icon to the right of it is a “read” icon, which is used here to read the input as a single channel with a single sample.

The “Formula 2” icon is the ADC and is used for turning the input analogue signal into a value that can be stored in 8-bits; it achieves this by first dividing the input value by 5 (because the max input value is 5, meaning the output will not be too big) and then multiplying that value by 256 (to represent 2^8).

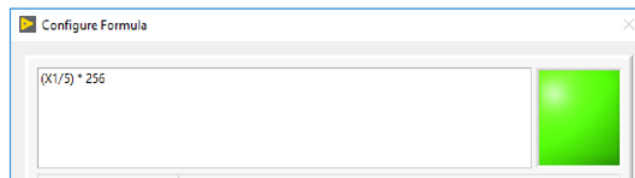


Figure 15 - “Formula 2” Parameters

The load input (gms) icon is there to show the load input value on the GUI.

The “Formula” icon is used for calculating the output value in grams based on the input voltage. The input (X1) is first divided by 5 (as 5 is the maximum voltage input) and then multiplied by 1000 (as 1000 is the maximum amount of grams).

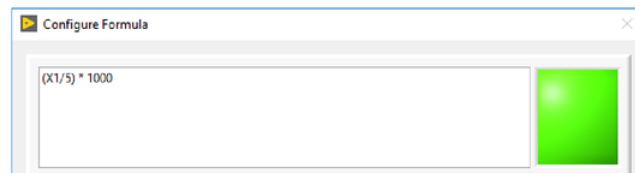


Figure 16 - “Formula” Parameters

The icon to the right of “Formula” is the “clear task” icon, which is used here to clear any task that’s still being processed, but not before releasing any resources to the error out.

The final icon is the error out icon, which is used to identify error information and provide error out functionality.

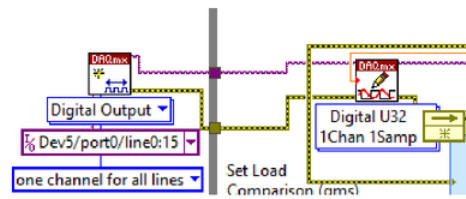


Figure 17 - Explanation of Design of LabVIEW Circuit (2/5)

On the row below are the next few icons.

The first icon is the digital output – this is there to provide the 16 bits which are being used for comparison, those bits are ports 0-7 and ports 8-15.

The next icon is a write icon, which is used to read the input value and carry on with the task and carry the error message.

The yellow icon to the right of the write icon is a feedback node, which is used to store data between loop iterations.

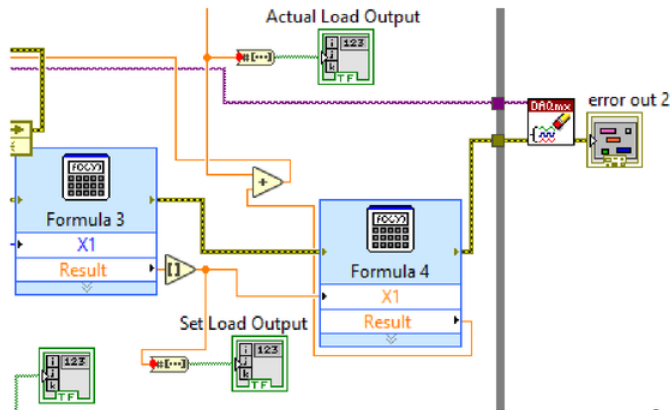


Figure 18 - Explanation of Design of LabVIEW Circuit (3/5)

Formula 3 is used for turning the value of grams from the set load comparison icon into a value that can be represented in 8-bits for 8-bit comparison. This is achieved by dividing the input value of grams by 1000 (as 1000 grams is the maximum possible amount) and then multiplying that value by 256 (to represent 8-bits).

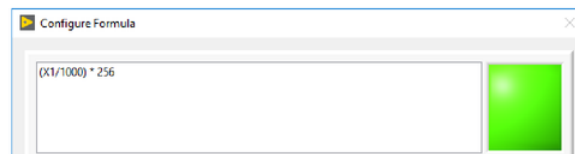


Figure 19 - "Formula 3" Parameters

The yellow triangular icon to the right of Formula 3 is a "round to nearest" icon, which allows the rounding of values to their nearest integer. This is important because non-integer values cannot be represented in 8-bits. *Not quite the reason this icon is used...*

The yellow icon below Formula 3 is a number to Boolean array, which is used to convert the input integer value into a Boolean array – in this case it returns a Boolean array of 8, because the number of bits in the input integer will not exceed 8 due to the calculations carried out previously.

The set load output is the icon which is being used to measure the input from the number to Boolean array before it and display it on the GUI in the form of 8-bit squares representing 8-bits.

The yellow icon with a "+" inside it is there to simply add two values together – in this case it's adding the output from "Formula 4" and "Formula" and forwarding the added values to digital U32 write icon.

Formula 4 is used for multiplying the output from formula 3 by 256 and then forwarding it to the "+" icon.

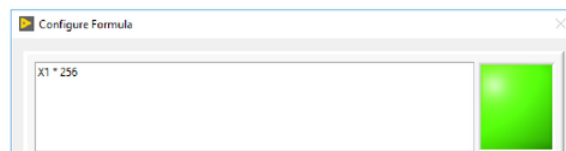


Figure 20 - "Formula 4" Parameters

The yellow icon to the left of the “actual load output” is a number to Boolean array - this case it returns a Boolean array of 8, because the number of bits in the input integer will not exceed 8 due to the calculations carried out previously.

The actual load output is the icon which is being used to measure the actual load output from the number to Boolean array icon to the left of it and display that value on the GUI in the form of 8-squares representing 8-bits.

The icon to the right of “Formula 4” is the “clear task” icon, which is used here to clear any task that’s still being processed, but not before releasing any resources to the error out.

The final icon is the error out icon, which is used to identify error information and provide error out functionality.

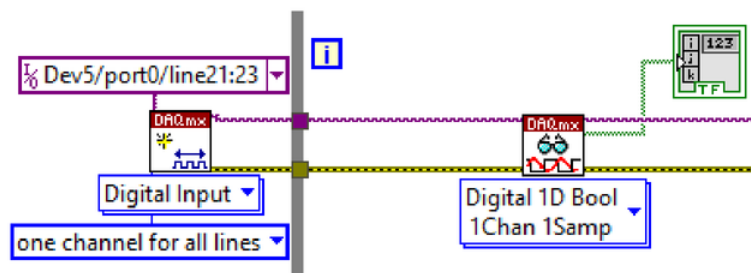


Figure 21 - Explanation of Design of LabVIEW Circuit (4/5)

The icon on the left is the digital input from the ELVIS II board which is being used to represent the input signal of whether the comparison is greater than, less than or equal to.

The digital 1D Bool is there to read the input as a Boolean value.

The icon to the top right is used to take the output from the read icon before it and display the output on the GUI in the form 3-squares representing 3-bits.

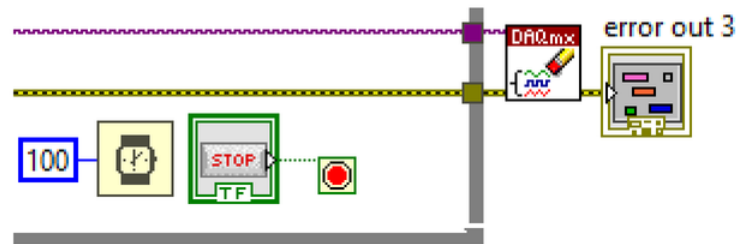


Figure 22 - Explanation of Design of LabVIEW Circuit (5/5)

The watch icon at the bottom right with the constant 100 value going into it is used to refresh loop the circuit every 100ms (every tenth of a second).

The stop icon is there to place a button on the GUI for stopping the circuit.

The icon to the left of error out is the "clear task" icon, which is used here to clear any task that's still being processed, but not before releasing any resources to the error out.

The final icon is the error out icon, which is used to identify error information and provide error out functionality.

Excellent detail on how the LabVIEW 'vi' was designed

The GUI that was produced by the Labview circuit was tidied up to have a simple and legible design that clearly shows the set load digital output, the actual load cell digital output and whether the load cell digital output was greater than, less than or equal to the set load digital output. The figure below shows the GUI that was produced.

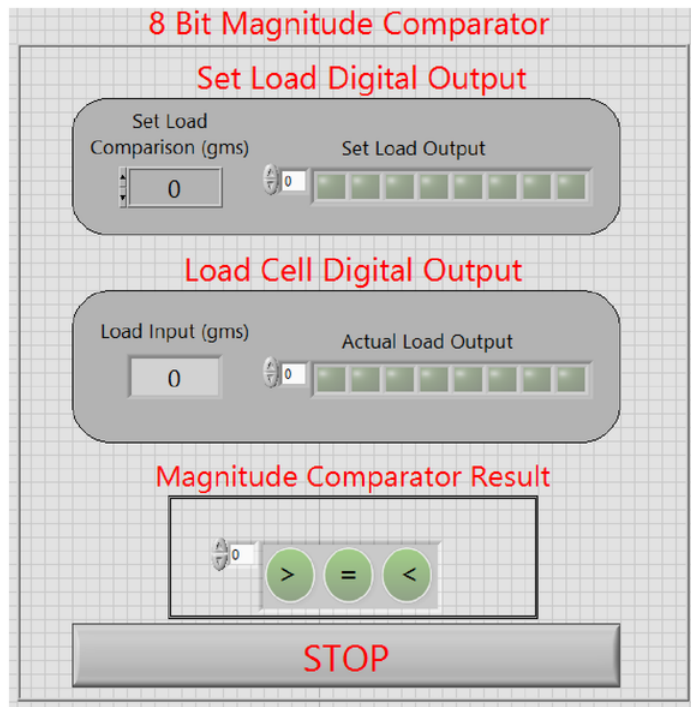


Figure 23 - LabVIEW GUI

The figure shows all of the things included in the design – a display of the load in grams, a numeric value for comparison, the set load output, the actual load output, a stop button and data for whether the circuit is greater than, less than or equal to.

4. Analysis of Signal Conditioning Circuit, NI Labview and Multisim Simulated Results

The assignment involved analysing the magnitude comparator on Multisim, a signal conditioning circuit on Multisim and a LabVIEW circuit. The analysis processes for these circuits are shown in the sections below.

4.1 – Magnitude Comparator on Multisim

The first circuit to be analysed was the 8-bit magnitude comparator; this involved simulating the circuit to obtain three results – greater than, less than and equal to. In order to test this, three indicators were attached to the output of the circuit where the leftmost indicator indicated that A was greater than B, the centremost indicator indicated that A and B were equal, and the rightmost indicator indicated that A was less than B.

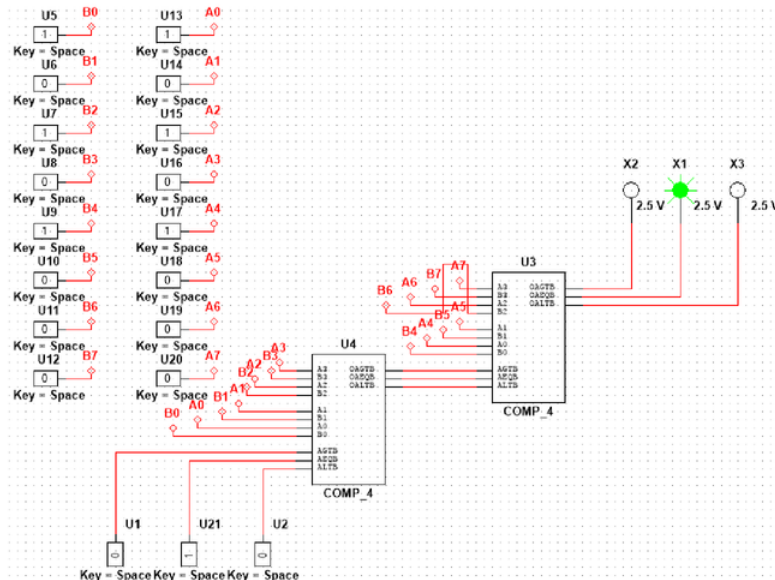


Figure 24 - Magnitude Comparator Analysis - A Equal to B

The first test for the circuit involved setting both A and B equal; they were both set to 00010101 (from MSB to LSB). Running the simulation produced the expected output of the centremost indicator being triggered, as can be seen in the figure above.

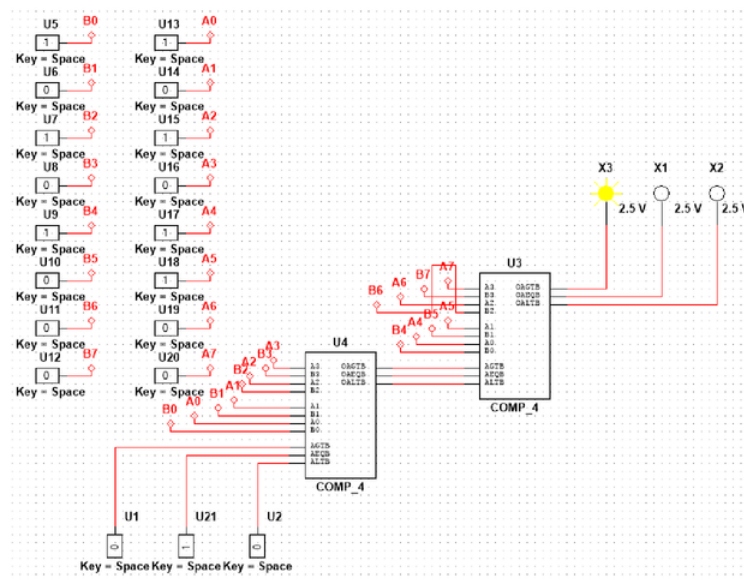


Figure 25 - Magnitude Comparator Analysis - A Greater Than B

The next test for the circuit was to make A greater than B, this was achieved by setting A to 00110101 and B to 00010101. The circuit produced the proper output, where the leftmost indicator lamp was activated.

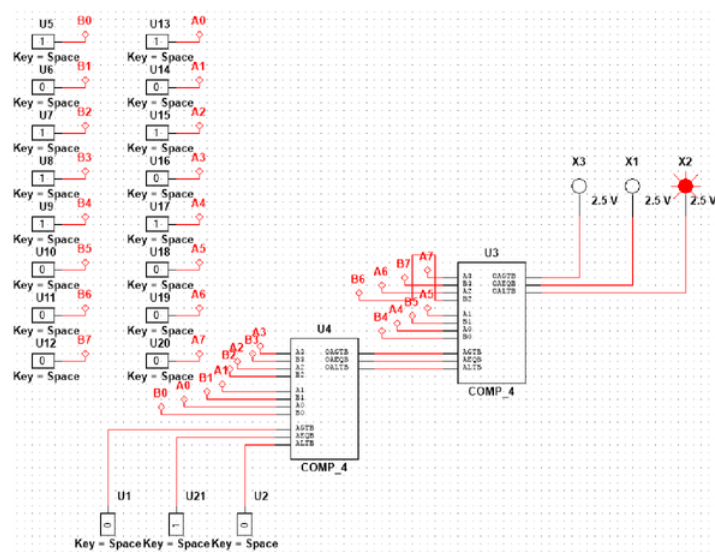


Figure 26 - Magnitude Comparator Analysis - A Less than B

The final test for the circuit was to make A less than B, this was achieved by setting A to 00010101 and B to 00011101. The resulting output was the correct indicator being activated – the rightmost indicator.

Good analysis of MultiSim simulated results

4.2 – Signal Conditioning Circuit on Multisim

The signal conditioning circuit designed on Multisim can be seen in the figure below.

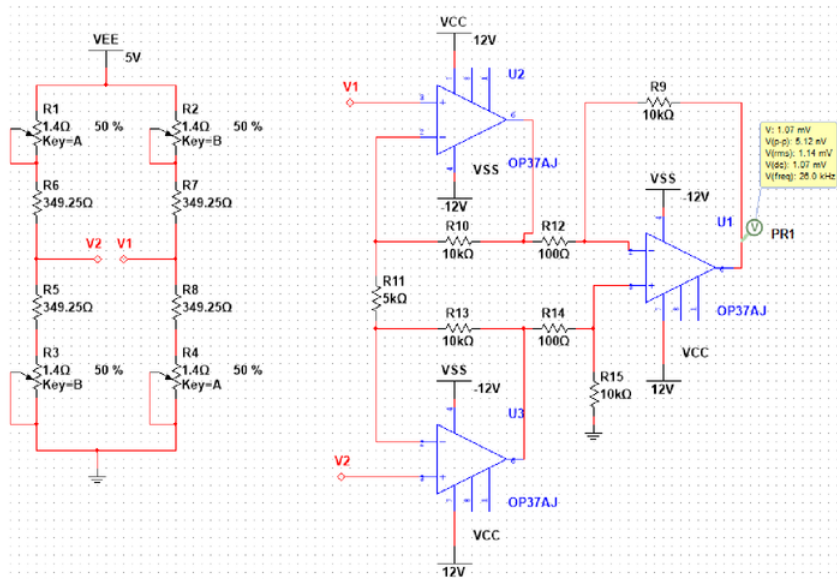


Figure 27 - Signal Conditioning Circuit to be Analysed

In the load cell part of the circuit, each potentiometer was paired with the potentiometer in the opposite corner of the load cell, and each pair (denoted as A and B) could be altered from 0% resistance to 100% resistance in increments of 5% which would change the resulting output voltage of the load cell. When A was at 50% and B was at 50%, this would simulate a load cell with no load, and when A was at 100% and B at 0%, this would simulate a load cell at full load. The table below shows the resulting simulated load values based on the potentiometer values and the graph shows the resulting voltage based on the load.

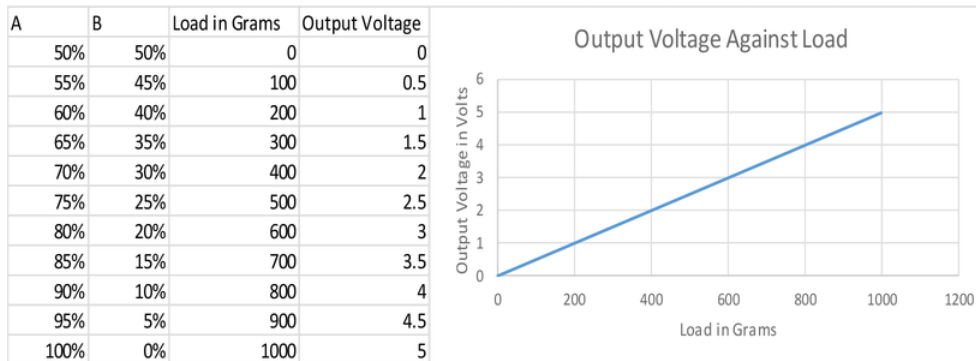


Figure 28 - Output Voltage/Grams based on Potentiometer Values

Good graphical analysis of the output voltage of the load cell over its load range

Before testing the final circuit (found in task 6), a prototype circuit was drawn up to test the 8-bit functionality of the LabVIEW circuit, this circuit can be seen in the figure below.



The figure displays a LabVIEW front panel and a subVI titled "Variable Power Supplies".

Front Panel:

- Analogue Input:** A numeric display showing the value 1.35.
- Digital Value:** A numeric display showing the value 65.5838.
- 8-bit Digital Output:** A row of eight green LEDs, all of which are currently lit.
- STOP:** A large red button labeled "STOP".

Variable Power Supplies SubVI:

- Manual Voltage Controls:** Two circular voltage controls. The left one is set to 0.00 V, and the right one is set to 1.35 V. Both have a "RESET" button below them.
- Sweep Settings:** A section for configuring a voltage sweep. It includes:
 - Supply Source:** A dropdown menu set to "Supply".
 - Start Voltage:** A numeric display set to -12.00 V.
 - Step:** A numeric display set to 0.25 V.
 - Stop Voltage:** A numeric display set to 0.00 V.
 - Step Interval:** A numeric display set to 1000 ms.
- Instrument Control:** A section for controlling the hardware. It includes:
 - Device:** A dropdown menu set to "Dev5 (NI ELVIS II)".
 - Buttons:** Four buttons at the bottom: "Run" (green arrow), "Sweep" (red sine wave), "Stop" (red square), and "Help" (red question mark).

Figure 30 - Prototype LabVIEW Circuit Analysis (1/3)

In the above figure, a test was carried out where 1.35V was injected into the circuit and outputs could be seen in the GUI to the left. The analogue input was read 1.36V and the output digital value was 69.5838, which based on the calculation of $\frac{1.36}{5} * 256 = 69.632$ is close enough to the actual value.

Good detail...

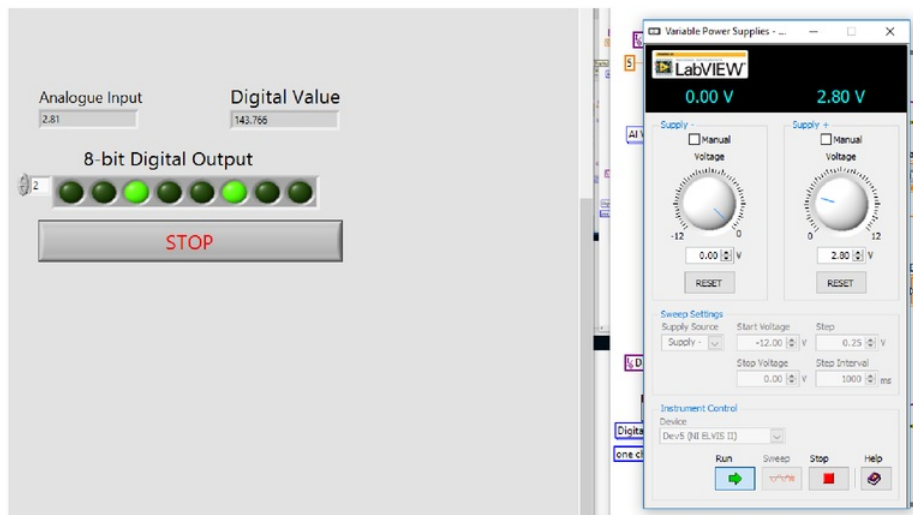


Figure 31 - Prototype LabVIEW Circuit Analysis (2/3)

In the above figure, a test was carried out where 2.80V was injected into the circuit and outputs could be seen in the GUI to the left. The analogue input was read 2.81V and the output digital value was 143.766, which based on the calculation of $\frac{2.8}{5} * 256 = 143.36$ is close enough to the actual value.

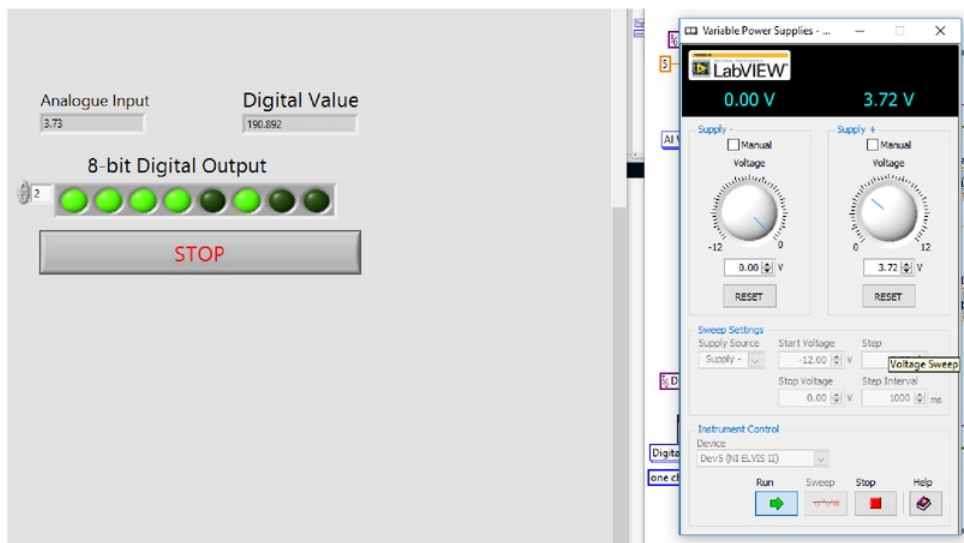


Figure 32 - Prototype LabVIEW Circuit Analysis (3/3)

In the above figure, a test was carried out where 3.72V was injected into the circuit and outputs could be seen in the GUI to the left. The analogue input was read 3.73V and the output digital value was 190.892, which based on the calculation of $\frac{3.72}{5} * 256 = 190.464$ is close enough to the actual value.

Very good set of results for the LabVIEW ADC

5. Practical Build and Test via NI ELVIS Board

The assignment involved building the magnitude comparator, the signal conditioning circuit and the LabVIEW circuit. The analysis processes for these circuits are shown in the sections below.

5.1 – Practical Build of Magnitude Comparator

In order to port the circuit from Multisim onto the Nexys4 DDR board, the circuit that was used to simulate the 8-bit magnitude comparator needed to be adapted and have its inputs and outputs changed to SW1, SW2 etc. and LED0, LED1 and LED2. The adapted circuit can be seen in the figure below.

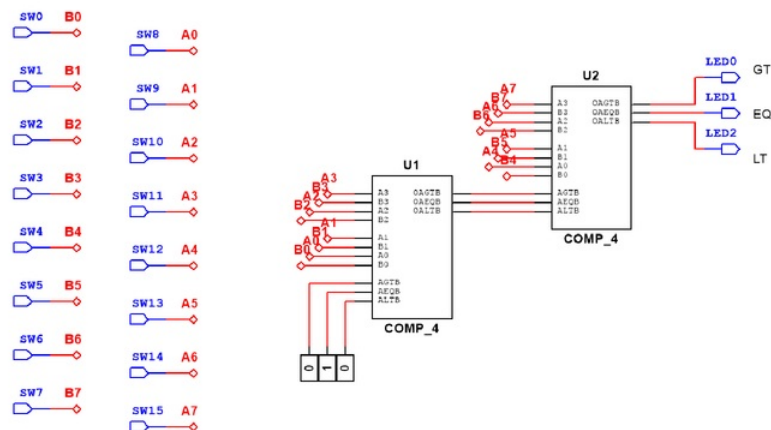


Figure 33 - Adapted Multisim Magnitude Comparator Circuit

The adapted circuit was then uploaded to the Nexys4 DDR board, where it was tested by changing switches 0-7 and switches 8-15 and then checking the output by looking at the LEDs on the right.

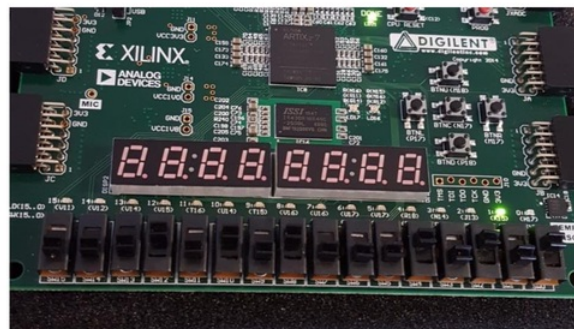


Figure 34 - Practical Build of Magnitude Comparator - A and B Equal

The above figure shows the output when both groups of switches were set to 00010101 – the result was the centremost LED being activated, indicating that A and B are equal as expected.

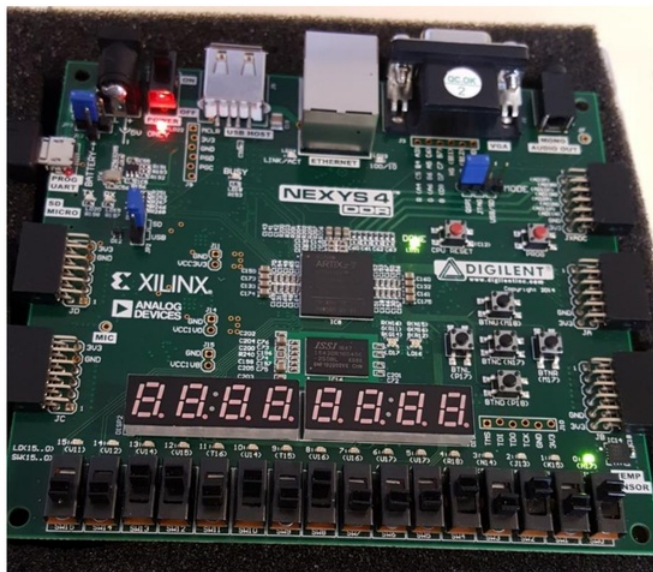


Figure 35 - Practical Build of Magnitude Comparator - A Greater than B

The above figure shows the output when A was 00110101 (MSB to LSB) and B was 00010101 - the result was the rightmost LED being activated, indicating that A was greater than B as expected.

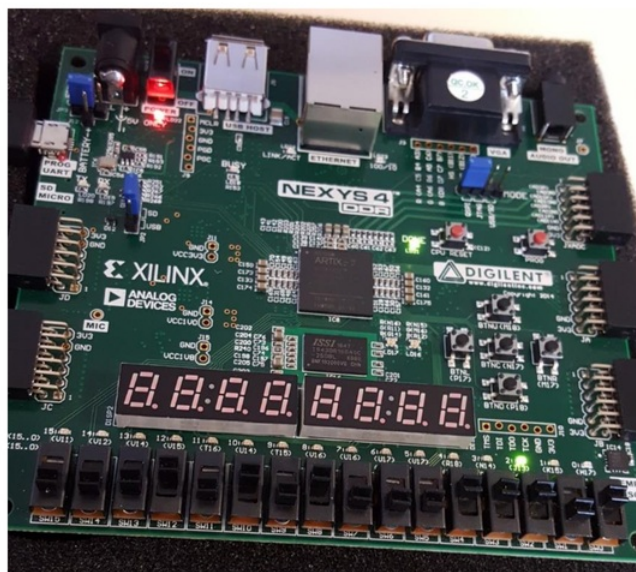


Figure 36 - Practical Build of Magnitude Comparator - A Less than B

The above figure shows the output when A was 00010101 and B was 00011101 - the results was the leftmost LED being activated, indicating that A was less than B as expected.

Good set of practical results shown which confirm the simulated results in MultiSim

5.2 – Practical Build of Signal Conditioning Circuit

The signal conditioning circuit was not practically built alone, but it was included in the final LabVIEW circuit in section 7. The simulation was proof enough that the signal conditioner would work, as it confirmed all theory.

5.3 – Practical Build of LabVIEW Circuit via NI ELVIS Board

The LabVIEW that was produced was uploaded to an FPGA board which was connected to the NI ELVIS II board. The connections can be seen in the figure below.

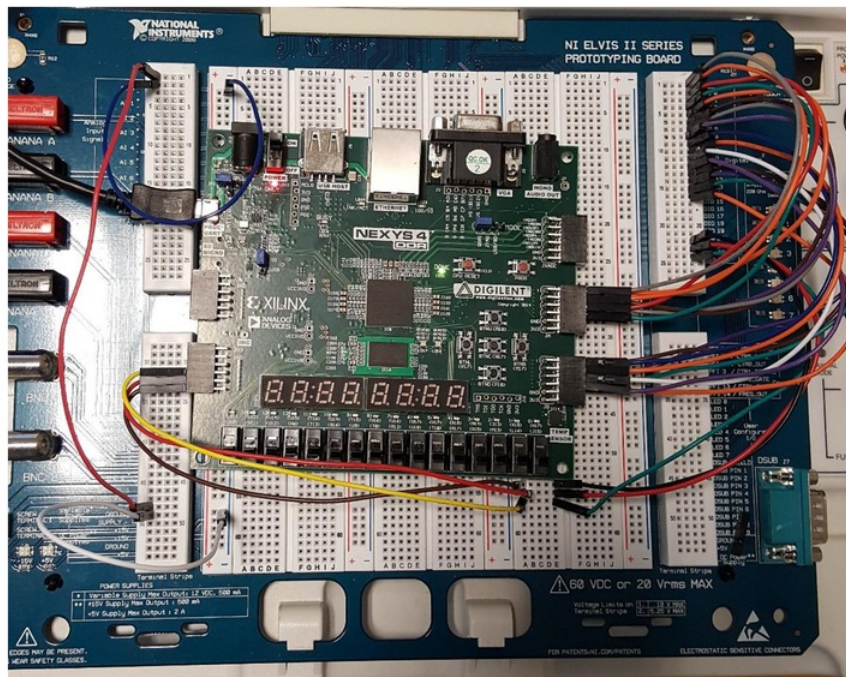


Figure 37 - Practical Build of LabVIEW Circuit

To test the circuit practically, the virtual power supply was set to a value below the set-point, equal to the set-point and above the set-point that was set on the GUI on LabVIEW and then the FPGA processed the two 8-bits along lines 0-15 which produced an output on one of three-bits, which would represent the less than, equal to or greater than.

Good pictorial evidence, but the connection to the PMOD connectors could have been explained in more detail

6. Analysis of NI LabVIEW/FPGA Results

The LabVIEW circuit that was produced was then tested on the FPGA by inputting a variable power supply into the LabVIEW circuit that was built in order to test it. Testing the LabVIEW circuit involved setting a value for comparison and then using the variable power supply to compare with the value that was set for comparison. The value that was set for comparison was 255.

Less Than

In the figure below the variable power supply was setup to produce an input of 1.11V; based on a range of 0-5V and a range of 0-1000gms, the 1.11V input produced a load of 224gms (although calculating the expected output produces 222gms as the range of grams is 200 times greater than the range of volts and $1.11V * 200 = 222$), as can be seen on the left of the figure. This value of 224gms was less than the value that was set for comparison, and so (at the top of the screen) the rightmost light was lit up to indicate that the input was less than the value that was set for comparison. *Good*

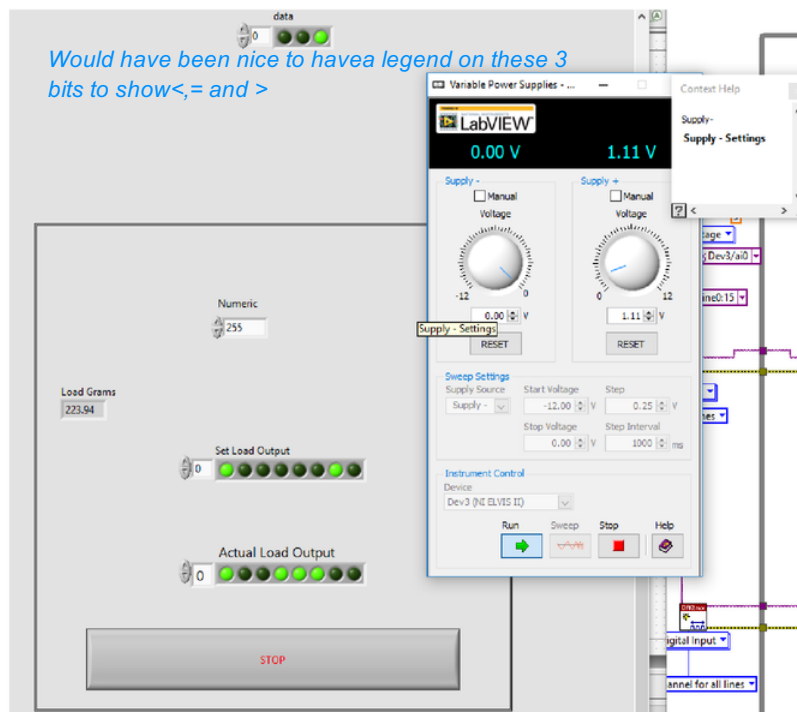


Figure 38 - LabVIEW Circuit - Less Than

In the above screenshot, the “set load output” lights didn’t do anything, since the variable power supply was in control of the load output. The set load output binary value shows 01000001 (it’s backwards on the GUI); which results in a value of 65 – this comes from $255/1000 * 256 = 65.28$ where 255 is the set numeric value, 1000 is the maximum value and 256 is the max binary value. The actual load output value shows 00111001 results in a value of 55 – this comes from $1.11/5 * 256 = 56.832$ where 1.11 is the input voltage, 5 is the maximum voltage and 256 is the max binary value.

Greater Than

The same test was carried out with a voltage that produced a greater load in grams than the set value; the voltage that was used on the variable power supply was 1.81V and the produced load in grams was 363gms (as opposed to the calculated 362gms). As expected, the LabVIEW circuit produced an output of greater than, indicated by the light on the left.

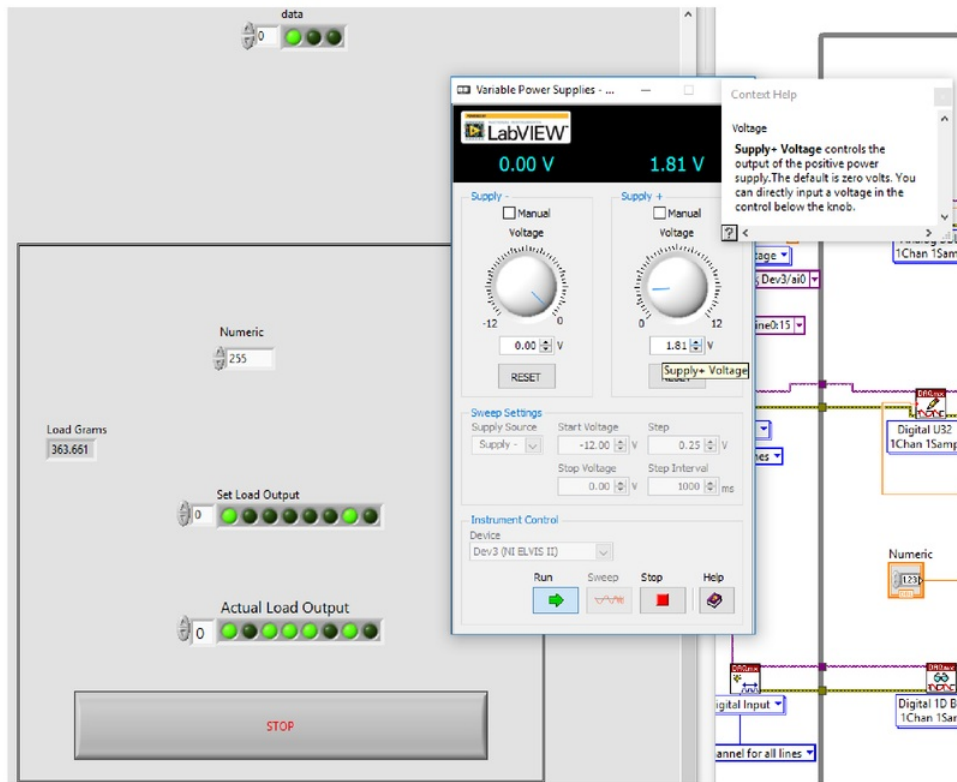


Figure 39 - LabVIEW Circuit - Greater Than

The actual load output value shows 01011101 which results in a value of 93 – this comes from $1.81/5 * 256 = 92.672$ where 1.81 is the input voltage, 5 is the maximum voltage and 256 is the max binary value. *Good result, explained well*

Equal To

The final test for the LabVIEW circuit was to set the variable power supply to input a voltage that would produce a load of 255, to match with the set value. 1.26V produced the correct load, and as expected, the middle light was activated to indicate that the set value and the load are equal.

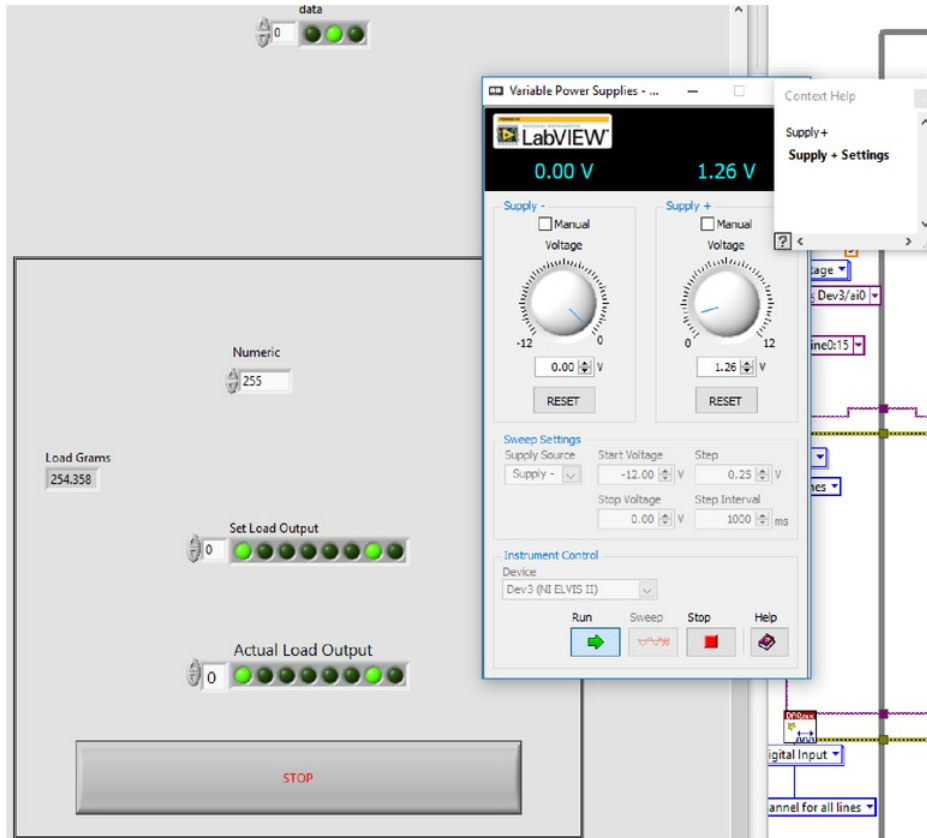


Figure 40 - LabVIEW Circuit - Equal To

The actual load output value shows 01000001 which results in a value of 65 – this comes from $1.26/5 * 256 = 64.512$ where 1.26 is the input voltage, 5 is the maximum voltage and 256 is the max binary value. *Good result...*

A good set of practical results which have been analysed well showing good understanding of the assignment requirements

7. Adapt Design to Fit New Purposes or Applications

The LabVIEW design that was created was adapted to have its outputs logged, which were then plotted using Excel to be further analysed. The adapted design can be seen in the figure below.

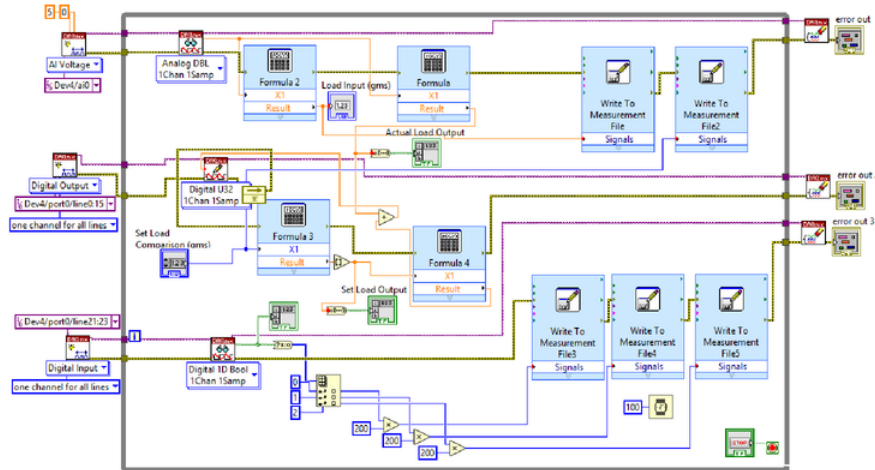


Figure 41 - Adapted LabVIEW Design

The LabVIEW design had five write to measurement files added – one was for load input (gms), one was for set load comparison (gms) and the last three were for when the load input was under the set load, when the load was equal to the set load and when the load was over the set load. For the last three, the output value was multiplied by 200 since the output would either be 0 or 1, and that was difficult to be seen in one graph with the load input and set load comparison values when they were all compared in an Excel graph.

More detail on the 'index array' icon would have been beneficial, but otherwise, a good explanation given

In order to take results from the LabVIEW design and produce the measurement files, a sweep was performed which involved taking values every second in a designated range – for 300g, the sweep was performed from 1.4V to 1.6V, since 1.5V is the equivalent of 300g when comparing 0-5V and 0-1000grams and a sweep is performed for $\pm 10\text{mV}$. The GUI for the adapted design is shown in the figure below, and the software to simulate a variable power supply for the LabVIEW design is on the right of the figure.

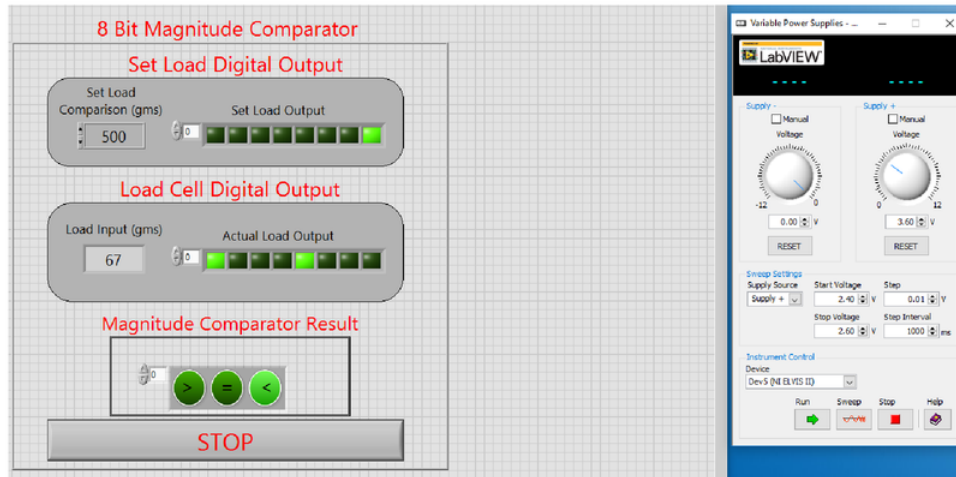


Figure 42 - Adapted Design's GUI and Variable Power Supply Software

8. Analysis of Data Logging Excel Results

The adaptation of the LabVIEW circuit allowed the data logging of numerous information, specifically: load input (gms), set load comparison (gms), load input under set load, load input equal to set load and load input over set load. The last three were multiplied by 200 so that they could be put on the same graph as the load information. When the adapted design was run using the “write to measurement” function in LabVIEW, the following five files were created.

Name	Date modified	Type	Size
test	29/03/2018 09:52	LVM File	5 KB
test1	29/03/2018 09:52	LVM File	3 KB
test2	29/03/2018 09:52	LVM File	3 KB
test3	29/03/2018 09:52	LVM File	3 KB
test4	29/03/2018 09:52	LVM File	3 KB

Figure 43 - Created Test Files

The files included a lot of information that was recorded by the LabVIEW software, and was written as can be seen in the figure below.

```

test.lvm - Notepad
File Edit Format View Help

Channels      1
Samples      1
Date         2018/03/29
Time         09:52:08.3215789794921875
X_Dimension   Time
X0            0.000000000000000E+0
Delta_X       1.000000
***End_of_Header***
X_Value      Untitled      Comment
0.000000     67.284681
0.100266     67.445700
0.199924     67.606719
0.301181     67.349088
0.405635     67.413496
0.501966     67.703330
0.603161     67.381292
0.702950     67.574515
0.803218     67.477903
0.903486     67.477903
1.002779     67.445700
1.103018     67.606719
1.202709     67.606719
1.302976     67.349088
1.402710     67.574515
1.502984     67.316884
1.603242     67.606719
1.703844     67.445700
1.803015     67.381292
  
```

Figure 44 - Written File Format

The information was accurate but was difficult to read because there were so many readings. To rectify this, the information was put into an Excel spreadsheet and a graph was created to compare all of the results of each test file created.

The figure below shows how the data was put into the Excel spreadsheet- there were five columns, one for each of the produced outputs.

Time (secs)	Sweep from 480mg to 520mg	Set Comparison Value	Greater than	Equal to	Less than
0	67.284681	500	0	0	200
0.100266	67.4457	500	0	0	200
0.199924	67.606719	500	0	0	200
0.301181	67.349088	500	0	0	200
0.405635	67.413496	500	0	0	200
0.501966	67.70383	500	0	0	200
0.603161	67.381292	500	0	0	200
0.70295	67.574515	500	0	0	200
0.803218	67.477903	500	0	0	200
0.903486	67.477903	500	0	0	200
1.002779	67.4457	500	0	0	200
1.103018	67.606719	500	0	0	200
1.202709	67.606719	500	0	0	200
1.302976	67.349088	500	0	0	200
1.40271	67.574515	500	0	0	200
1.502984	67.316884	500	0	0	200
1.603242	67.606719	500	0	0	200
1.703844	67.4457	500	0	0	200
1.803015	67.381292	500	0	0	200
1.904285	67.477903	500	0	0	200
2.004548	67.510107	500	0	0	200
2.104818	67.284681	500	0	0	200
2.205081	67.574515	500	0	0	200
2.305414	67.4457	500	0	0	200
2.405024	67.4457	500	0	0	200
2.505288	67.606719	500	0	0	200
2.606558	67.606719	500	0	0	200
2.708307	67.381292	500	0	0	200
2.808483	67.413496	500	0	0	200
2.907747	67.574515	500	0	0	200
3.009016	67.574515	500	0	0	200
3.109282	67.413496	500	0	0	200
3.20955	67.349088	500	0	0	200
3.308863	67.606719	500	0	0	200
3.408866	402.818524	500	0	0	200

Figure 45 - Excel Spreadsheet

The figure below shows the graph that was produced using the data in the Excel spreadsheet.

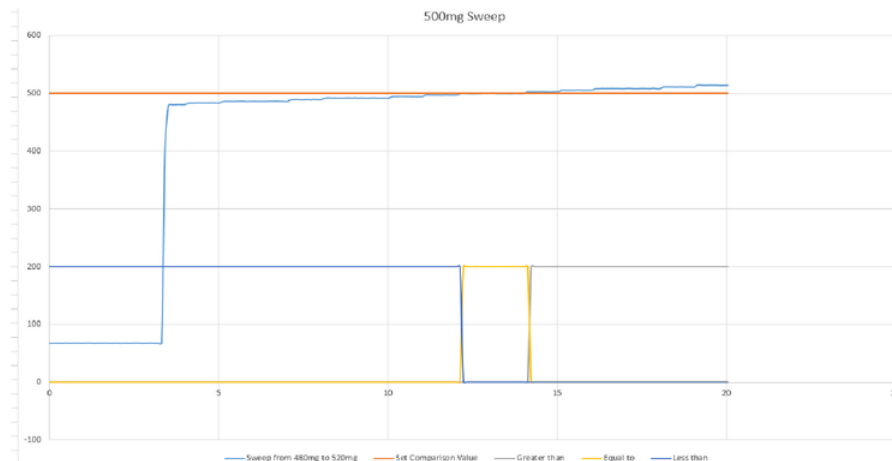


Figure 46 - Excel-Produced Graph

The graph that was produced has a legend at the bottom to show what the individual graphs represent. The values for greater than, equal to and less than are 200 or 0 because the value outputs are meant to be either 1 or 0, so they're multiplied by 200 (as can be seen on LabVIEW front panel) in order to be seen on the above scatter graph. What can be observed from the graph is that the sweep comes into effect at around 3.5seconds, and then sweeps for another 16.5seconds. In that time, the greater than signal is a logic 1 for the first 12.5seconds, the equal to signal then comes on for about 2 seconds, and the less than signal then comes on for the remaining time.

9. Conclusions

In the few tasks involved within the assignment, LabVIEW and NI DAQmx features proved to be effective tools for developing efficient components and circuits which have been used to achieve multiple outcomes. I have learned that the applications of LabVIEW are many and the potential of LabVIEW is tremendous, circuits can be designed and expanded upon with ease when LabVIEW is utilised properly. The NI Elvis II board and Nexys 4 FPGA both proved very useful when practically testing the circuits that had been designed on LabVIEW and Multisim and were very friendly with the software in that there were no issues with uploading the designed circuits. The research that was done towards the beginning of the assignment proved useful for comprehending the theory behind ADCs, digital magnitude comparators and load cells; understanding NI DAQmx data acquisition icons proved extremely useful when designing the many LabVIEW circuits.

The assignment aims involved designing:

- A LabVIEW 'vi' that will interface to an FPGA via the NI ELVIS II board to give an 8-bit digital comparison from two input signals that had been converted to 8-bit
- An 8-bit magnitude comparator in Multisim on the Nexys 4 DDR FPGA board
- An adaptation on the LabVIEW design to allow data logging

Each of these files were designed, simulated and tested individually over several sessions and the report summarises the process of each part of the assignment to the best of my ability.

Good detailed conclusion given with some reflection noted.

10. Bibliography

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Rowe, M. (2018, April 20). *How do ADCs work?* Retrieved from EDN Network: <https://www.edn.com/design/test-and-measurement/4383626/How-do-ADCs-work->

Subminiature Load Cell LCKD Series Rugged Industrial Design. (2018, April 20). Retrieved from Omega: <https://www.omega.co.uk/pptst/LCKD.html>

Works cited could have been more varied

Assignment 2

GRADEMARK REPORT

FINAL GRADE

GENERAL COMMENTS

Instructor

68/100

PAGE 1

PAGE 2

PAGE 3

PAGE 4

Text Comment. Good detailed introduction

PAGE 5

PAGE 6

PAGE 7

PAGE 8

Text Comment. Good, comprehensive research carried out on the LabVIEW DAQmx icons used within the assignment

PAGE 9

PAGE 10

Text Comment. Good understanding shown on how a magnitude comparator functions

PAGE 11

Text Comment. Limited research carried out

PAGE 12

Text Comment. Good

Text Comment. Good detail but could have been further researched

PAGE 13

PAGE 14

PAGE 15

Text Comment. Very good detail on the design of the magnitude comparator in MultiSim simulation and downloading to the FPGA

PAGE 16

PAGE 17

Text Comment. Quite a small value? The actual designed value was 10mV @ full load (1000gms) hence the reason for the gain of 500 to give 0-5V over 0-1000gms

PAGE 18

PAGE 19

PAGE 20

PAGE 21

Text Comment. Not quite the reason this icon is used...

PAGE 22

PAGE 23

Text Comment. Excellent detail on how the LabVIEW 'vi' was designed

PAGE 24

PAGE 25

PAGE 26

Text Comment. Good analysis of MultiSim simulated results

PAGE 27

Text Comment. Good graphical analysis of the output voltage of the load cell over its load range

PAGE 28

Text Comment. Good detail...

PAGE 29

Text Comment. Very good set of results for the LabVIEW ADC

Text Comment. Good set of practical results shown which confirm the simulated results in MultiSim

Text Comment. Good pictorial evidence, but the connection to the PMOD connectors could have been explained in more detail

Text Comment. Good

Text Comment. Would have been nice to have a legend on these 3 bits to show <, = and >

Text Comment. Good result, explained well

Text Comment. Good result...

Text Comment. A good set of practical results which have been analysed well showing good understanding of the assignment requirements

Text Comment. More detail on the 'index array' icon would have been beneficial, but otherwise, a good explanation given

Text Comment. Less than

Text Comment. Greater than

Text Comment. Some confusion between less than and greater than but very good detail on how the results were obtained

Text Comment. Good detailed conclusion given with some reflection noted.

PAGE 41

Text Comment. Works cited could have been more varied

GRADING FORM: CSG-RUBIC

JOSEFF JONES

68

RESEARCH-INFORMED LITERATURE



Analogue / Digital Converters: Limited research carried out (2/5) Load Cells: Good detail but could have been further researched (3/5) Digital Magnitude Comparators: Good understanding shown on how a magnitude comparator functions (4/5) NI DAQmx in LabVIEW: Good, comprehensive research carried out on the LabVIEW DAQmx icons used within the assignment (3/5)

12

KNOWLEDGE AND UNDERSTANDING



Design of the signal conditioning circuit for LCKD-1Kg Load Cell: Good detail on the instrumentation amplifier but confusion as to why the gain needed to be 500 (2/5) Design of LabVIEW 'vi': Excellent detail on how the LabVIEW 'vi' was designed although slight confusion as to the use of the 'round to nearest' icon (8/10) Design of 4/8-bit Magnitude Comparator: Very good detail on the design of the magnitude comparator in MultiSim simulation and downloading to the FPGA (7/10) Re-design to suit

20

new applications: More detail on the 'index array' icon would have been beneficial, but otherwise, a good explanation given (3/5)

ANALYSIS



Analysis of signal conditioning circuit: Good graphical analysis of the output voltage of the load cell over its load range (4/5) Analysis of MultiSim Results: Good analysis of MultiSim simulated results. Good set of practical results shown from the FPGA which confirm the simulated results in MultiSim (4/5) Analysis of NI LabVIEW / FPGA results: A good set of practical results which have been analysed well showing good understanding of the assignment requirements (8/10) Analysis of data logging files in EXCEL: Some confusion between less than and greater than but very good detail on how the results were obtained (3/5)

19

PRACTICAL APPLICATION AND DEP.



Build interface between LabVIEW and the FPGA board via the NI ELVIS 11 board: Good pictorial evidence, but the connection to the PMOD connectors could have been explained in more detail (6/10)

6

SKILLS FOR PROFESSIONAL PRAC.



Deployment of appropriate media: Excellent use made of screen shots and pictorial evidence which enhanced the design and analysis of the assignment. (4/5) Report layout and readability: Very good flow throughout the assignment which covered all aspects of the assignment. (4/5)

11

Appropriate conclusion: Good detailed conclusion given with some reflection noted. (3/5)