1809812

by Liam George

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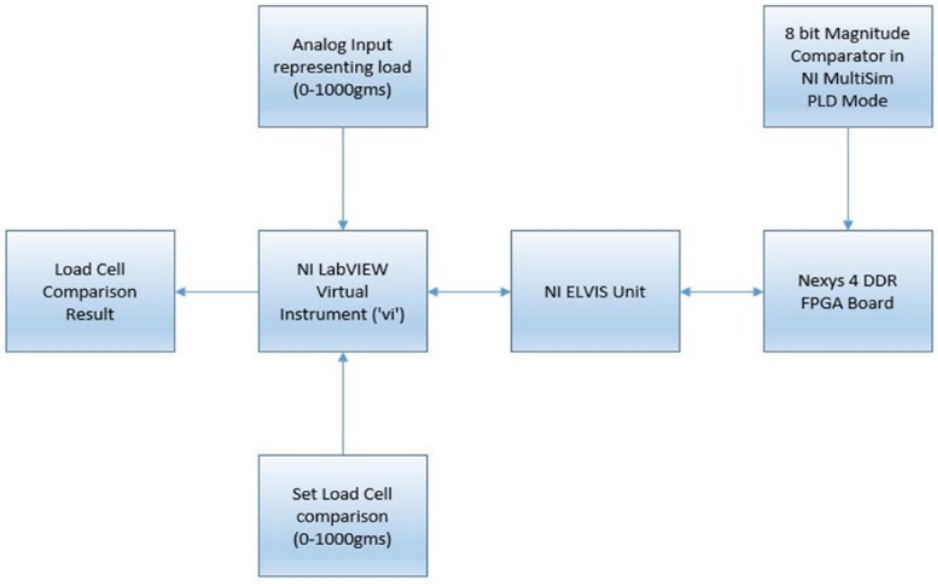
Good list of figures

1.0 Element 1

1.1 Introduction

As stated in the Assignment Brief.

The Figure below shows a block diagram of a magnitude comparator. Signal 1 is to be obtained from an analogue input to LabVIEW in the range of 0 – 5V representing a load applied to an LCKD-1Kg Load Cell which will be converted to an 8 bit digital signal and output to the FPGA via the NI ELVIS II board. Signal 2 is to be obtained from a 'set' value in LabVIEW in the range 0 – 1000gms, converted to an 8 digital signal and output to the FPGA via the NI ELVIS II board. (Jenkins, 2020)



(Jenkins, 2020)

Avoid the first person terms

In Element 1 We will be Researching, Designing, Simulating and Testing the 8 bit Magnitude Comparator, and Downloading to the Nexys 4 DDR FPGA Board and carrying out Practical tests.

The requirements are to Design and Implement a combinational logic system using VHDL and IP Integration using the Nexys 4 DDR FPGA development board.

Design and Simulate an 8-bit Magnitude Comparator in Multisim PLD mode, Analyze three sets of test results below, equal to and above the 'set' value.

The 4 bit adder and 4 bit comparator are the initial designs

1.2 Research

1.2.1 Digital design methods using VHDL an IP integration

Within Digital design, VHDL is used in each process of producing a chip, from the design process through to the testing process. VHDL (VHISC Hardware Description Language) is a major hardware description language and is used on FPGA (Field- programmable gate arrays) and ASIC (Application Specific Integrated Circuit) and many other Digital circuits.

VHDL uses a language as shown below in figure 1, an example from a program called Labview. VHDL is used to Interface the FPGA board with Labview and develop a system where it can be designed, Simulated and tested before implementation.

The program environment is Vivado from Xilinx

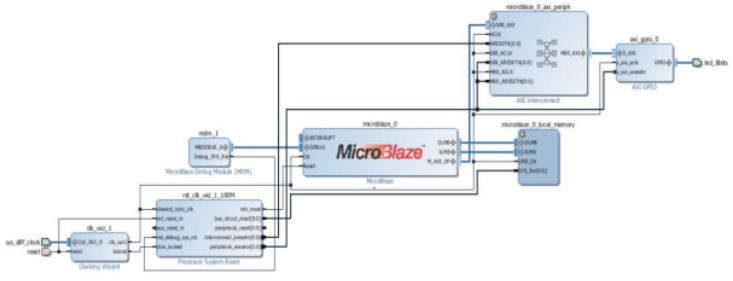
```
entity PID_Controler is
      Generic(Kp : std_logic_vector(7 downto 0) := B"11111010";
              Kv : std_logic_vector(7 downto 0) := B"00111100";
              Ki : std_logic_vector(7 downto 0) := B"00111100");
      Port(Actual_input : in  STD_LOGIC_VECTOR (29 downto 0);
        Dsired_input : in  STD_LOGIC_VECTOR (29 downto 0);
        PID_control : out  STD_LOGIC_VECTOR (34 downto 0);
        Reset : in  STD_LOGIC;
        CLK : in  STD_LOGIC;
        Sample_clk : in  STD_LOGIC);
end PID_Controler;
----------------------------------------------------------------------------
architecture Behavioral of PID_Controler is
----------------------------------------------------------------------------
------Signals definitions
----------------------------------------------------------------------------
signal Actual_input_buf : std_logic_vector(39 downto 0);
signal Desired_input_buf : std_logic_vector(39 downto 0);
signal Error_gain : std_logic_vector(47 downto 0);
signal Error_diff : std_logic_vector(39 downto 0);
signal Error_integral : std_logic_vector(39 downto 0);
signal Error : std_logic_vector(39 downto 0);
signal Error_diff_gain : std_logic_vector(47 downto 0);
signal Error_integral_gain : std_logic_vector(47 downto 0);
signal PID_control_buf : std_logic_vector(39 downto 0);
```

Good example and correct statement that it does make possible the interface with LabVIEW.

Figure 1 - VHDL language

(gate, 2020)

IP Integration is used to contain a full system which can be a single block which can be reused. Which minimises the design process and the integration of more systems easily. Using IP (Intellectual Properties) design means that multible blocks can be used to form a system which are connected together using a Feature found in Xilinx (Vivado) as shown below in figure 2.



Good example of IP design

Figure 2 - IP Integration Xilinx example

(Xilinx, 2020)

1.2.2 NI DAQmx data acquisition used in Labview

Labview uses the NI DAQmx driver for data acquisition, the NI DAQmx driver is the updated version of NI DAQ. NI DAQmx has many additional upgraded features but mainly the advance in its performance.
Shown Below shown in figure 3 is a typal Labview block diagram using NI DAQmx :-

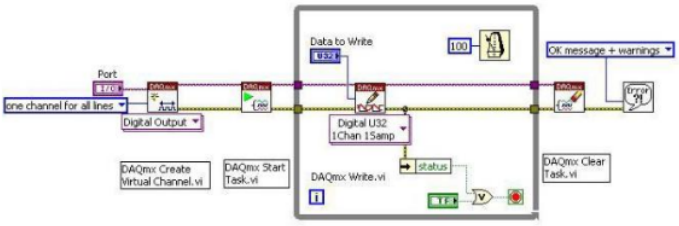


Figure 3 - Labview block diagram

(Instruments, 2020)

Above shown in figure 3 there are many communication blocks used to make up the NI DAQmx, The process and common graphics described below.

The Add Icon below shown in figure 4 is where the Inputs X and Y and Inputted together and Added together for the Output.



Figure 4 - Add Icon

The Analogue Input Voltage shown in figure 5 below measures voltage, where it creates channels to measure voltage, the AI- voltage-basic can be used to scale the voltage using excitation.

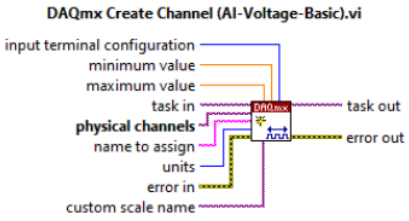


Figure 5 - Analogue Input Voltage Icon

Analogue read icon is used to read the input channels values allowing data to be outputted accordingly from different channels as shown below in figure 6.



Figure 6 - Analogue Read Icon

Clear task Icon releases the reserved tasks which are useful and clears the tasks that are not. Icon shown below in figure 7.

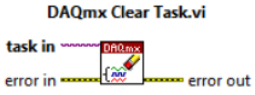


Figure 7 - Clear Task Icon

The Digital Input Icon shown below in figure 8 measures the digital input where the digital input can be outputted as a single channel or can be separated into multiple channels.

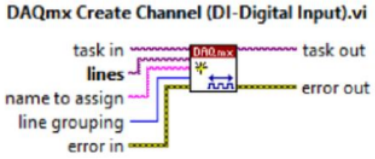


Figure 8 - Digital Input Icon

The Digital Output Icon shown in figure 9 has the same principle as the Digital input where the output can be a single channel or separated into multiple channels.

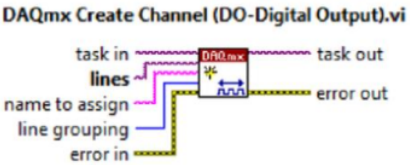


Figure 9 - Digital Output Icon

Digital read icon shown below in figure 10 reads a single digital input channel of Boolean values.

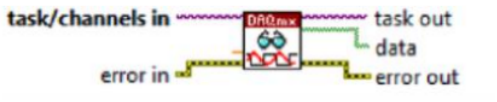


Figure 10 - Digital read Icon

The Write Icon writes an unsigned integer which is 32-bit and contains a single digital output channel as shown below in figure 11.

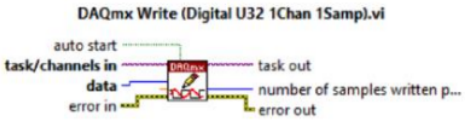


Figure 11 - Write Icon

The wait Icon is used to synchronise, by waiting until the next millisecond multiple as shown in figure 12 below.

Explanation covers the main relevant DAQ components needed for the system

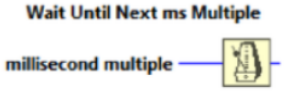


Figure 12 - Wait Icon

1.2.3 Digital Magnitude Comparators

Digital magnitude comparators are a combination of logic circuits used to compare two binary words and tell which one is greater than the other or whether they are equal.
A series of gates are used to compare their input signals and produce the output signals depending on conditions.

Below shown in figure 13 is an example of a 1-bit digital magnitude comparator.

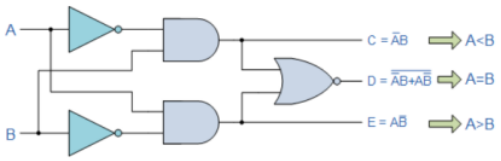


Figure 13 - 1-bit Digital Magnitude Comparators

The truth table below shown in figure 14 shows the operation of the 1-bit digital magnitude comparator shown above.

Inputs		Outputs		
B	A	A > B	A = B	A < B
0	0	0	1	0
0	1	1	0	0
1	0	0	0	1
1	1	0	1	0

Figure 14 - 1-bit digital magnitude comparator truth table

A truth table as shown above is very useful as the same process is used to produce much bigger magnitude comparators, by cascading to produce n-bit comparators.

Below shown in figure 15 is a 4-bit digital magnitude comparator, as you can see this is a much bigger comparator and is made up by various AND,NOR and NOT gates.

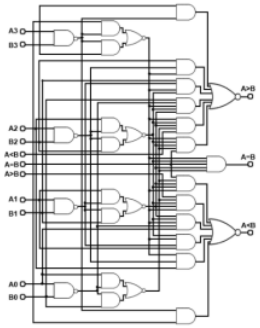


Figure 15 - 4 Bit digital magnitude comparator logic gates

As you can see in figure 15 above n-bit magnitude comparators can get quite big, and can be even bigger where cascading is used, where a multiple of comparators are cascaded to

produce bigger comparator. This can be minimized by using multi-bit comparators as shown below in figure 16.

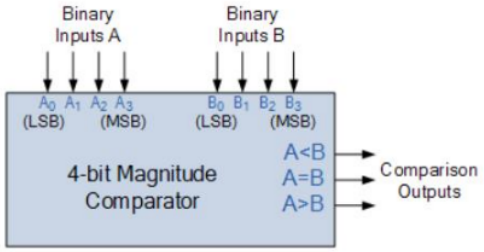
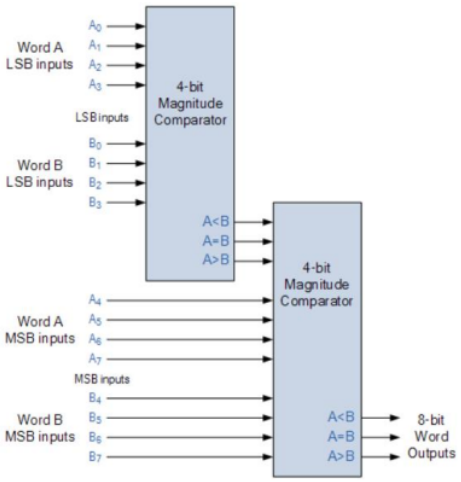


Figure 16 - Multi bit 4 bit magnitude comparator

(electronics-tutorials, 2018)

As shown in figure 16 above the multi bit comparator is used to compare multiple Binary Inputs and BCD and output produce an output if A<B , A=B or A>B.

Magnitude Comparators can be cascaded together to produce n-bits, which means words as much as 32 bits can be compared by connecting the Output of the first magnitude comparator to the cascading input on the second magnitude comparator, as shown below in figure 17 where to 4 bit magnitude comparators make up an 8 bit magnitude comparator.



Comparators are covered in good detail.

Figure 17 - multi bit 8 Bit magnitude Comparator

(electronics-tutorials, 2018)

The 8 bit magnitude comparator above in figure 17 will compare both 4 bit comparators together as an 8 bit comparator and produce output values for the 3 different conditions A<B, A=B or A>B.

1.2.4 Analogue to Digital Converters

ADC's (Analogue to digital converters) convert an analogue signal into digital, this is carried out by sampling the signal to determine the resolution. ADC's are used to convert an analogue signal into binary code which allows digital circuit to interface. The process shown below in the block diagram in figure 18.

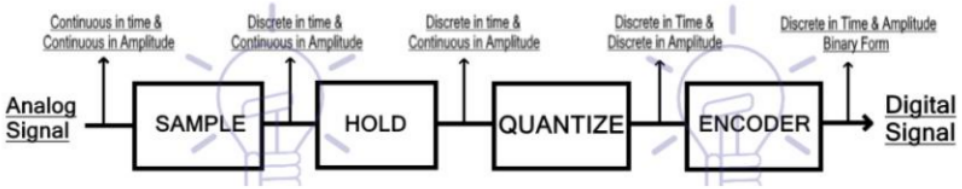


Figure 18 - Analogue to Digital Conversion Block Diagram

(technology, 2018)

There are many different types of analogue digital converters, the most common being Flash, Pipeline, SAR (Successive Approximation), sigma delta and integration. Shown below in figure 19 are the 5 main types plotted on a graph, showing the trade of between Resolution and Sampling rate. Each of these ADC's are used in different applications, due to the various applications shown in the graph below needing different factors to work efficiently.

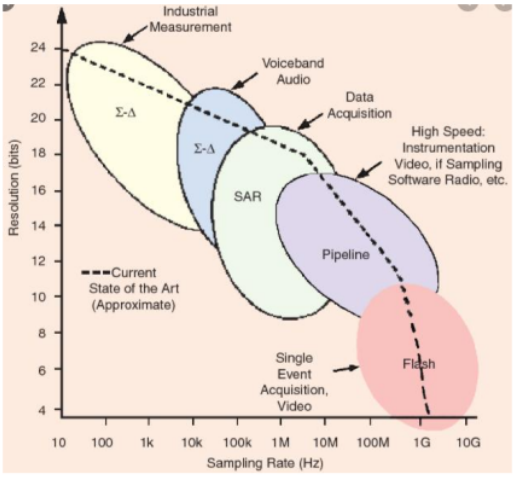


Figure 19 - ADC Converters Sample rate vs Resolution

(scholar, 2005)

Each of these ADC's have their Advantages and Disadvantages as shown below in the table in figure 20.

Architecture	Advantages	Disadvantages
Flash ADC	Very high speed Low latency	Not efficient for power and area
Delta-Sigma ADC	High resolution Low noise	Long latency Not suitable for channel multiplexing
Pipeline ADC	Fast sampling rate Moderate power consumption	Long latency
SAR ADC	Power and area efficient Low latency Suitable for channel multiplexing	Less power efficient for very high resolution

Figure 20 - ADC types Advantages and Disadvantages

(engineering, 2019)

The most common ADC used is the SAR (Successive approximation register), this is due to being suitable for a wide range of applications. The SAR as shown in figure 19 has a wide range of resolutions from 8- 20 bit whilst achieving a high sample rate.

Below shown in figure 21 is a basic design of a SAR ADC, and in figure 22 shows the sampling time graph.

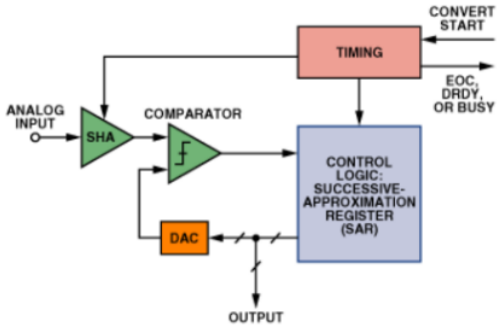


Figure 21 - SAR ADC Block Diagram

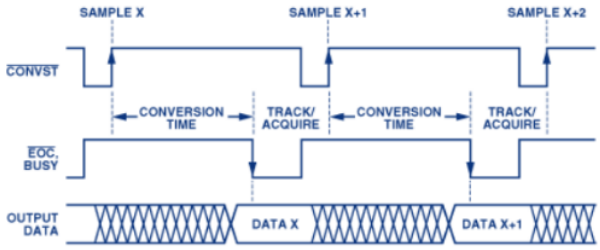


Figure 22 - SAR ADC sample time graph

(Kester, 2005)

Good work here. You have identified the relationship with resolution and sample rate which is determined by the conversion process.

1.2.5 Load Cells

A load cell is widely used within Industry to measure the weight of silos, hoppers and much more. Being a type of Transducer a loadcell converts force into an electrical signal, which is read by a system to show the weight of a product or substance. As the applied force (weight) changes the electrical signal changes accordingly.

There are many types of Loadcells used within Industry, one of the most common being the LCKD range. The LCKD series is made up of a stainless steel construction, which makes a good Robust loadcell which produces superior linearity and stability. The LCKD range consists of loadcells which can measure from 1kg to 1000lb as shown below in figure 23.



Figure 23 - LCKD series range

(Omega, 2020)

The LCKD range uses an Excitation voltage of 5V Dc and output voltage of up to 2mv. Due to resistance temperatures the LCKD uses a miniature circuit board housed within the loadcells cable to compensate.

Good explanation of the transducer load cell which is relevant to the task

This type of load cell uses a strain gauge construction where 4 strain gauges are used as shown in figure 24 below, this is to achieve accurate readings and maximum sensitivity. As shown in figure 24 a Wheatstone bridge uses two of the strain gauges for tension and the other two used for compression, giving proportional readings when a weight is applied.

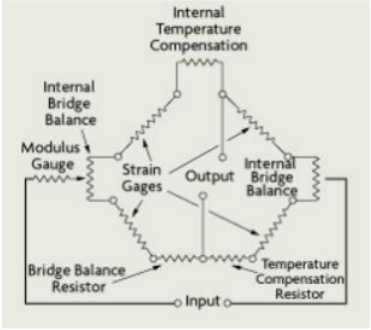


Figure 24 - Wheat stone bridge

(Omega, 2020)

1.2.6 Instrumentation and Signal Conditioning

Signal Conditioning is used to process an input signal from a transducer/ sensor and manipulate the signal to meet the requirements of the next stage. This can be carried out in many different ways to meet various requirements of the next stage. A few different signal conditioning processes used are:-

Amplification – Which is used if the voltage signal needs to be Amplified to meet requirements of DAQ.

Excitation – Excitation is where a transducer may need a separate power supply, an excitation supply could either be a voltage or a mA current depending on the transducer/sensor requirements.

Linearisation – This is needed when the signal from the transducer/ sensor doesn't correspond to actual measurement, linearity is used to ensure there is a straight line relationship.

Cold Junction – Compensates for cold junction temperature in the software.

Filtering – A filter is used to reduce any noise errors within the signal, using high or low pass filters.

Isolation – Prevents high voltage spike damaging other inputs or other parts of the circuit by isolating from one another

Figure 25 below shows how a signal conditioner is used within a circuit, between the transducer/ sensor and the plant readings, showing the processes involved to get an accurate and stable signal measurement reading.



Figure 25 - Signal conditioning system

(Onat, 2019)

Figure 26 below show another Signal conditioning system but with Excitation.

The stages of signal conditioning have been identified here and backed up with a good explanation and images.

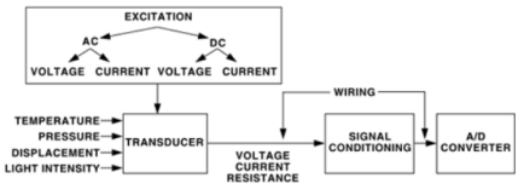
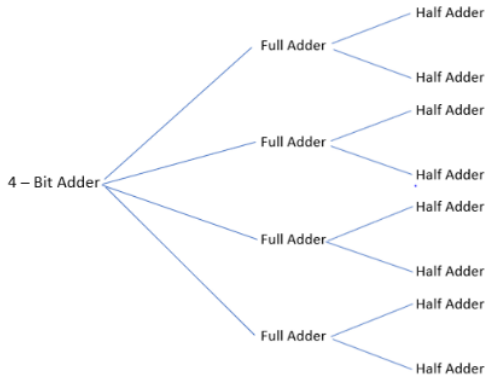


Figure 26 - Signal conditioning system with Excitation

1.3 Design Requirements

A 4 bit adder is designed using Xilinx Vivado software using VHDL language. Firstly a half adder is designed, as a 4 bit adder is made up of 4 Full Adders and a full adder is made up using 2 Half adders as shown below in the structure.



Hierarchy and inheritance have been identified

Figure 27 - 4 - Bit Adder construction

A Half adder is designed using a logic circuit and truth table as shown below in figure 29. Firstly shown In figure 28 is a block diagram of a half adder, which shows it is made up of 2 inputs and 2 outputs with a logic circuit in-between.



Figure 28 - Half Adder Block Diagram

(Circuitverse, 2019)

Figure 29 below shows the half adder Logic gate that's constructed and made up of an And gate and an XOR gate.

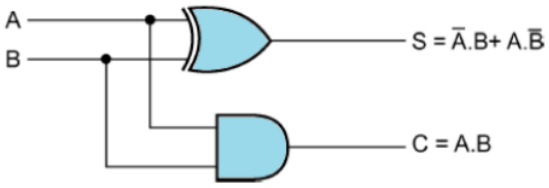


Figure 29 - Half Adder Logic gates

(Subham, 2014)

A Truth table is then made up as shown in figure 30 below showing all possible input and output combinations. And a Boolean expression can be derived.

A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Figure 30 - Half Adder truth table

(Subham, 2014)

Full Adder

Once the Half adder is fully built a full Adder can then be made, as the full adder is made up of 2 half adders as shown below in figure 31.

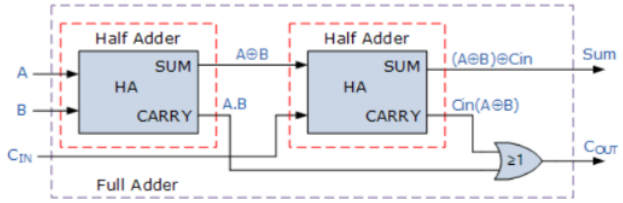


Figure 31 – Full Adder construction Block Diagram

(tutorials, 2019)

The Full adder logic diagram consists of two half adders combined together with an added OR gate as shown below in figure 32.

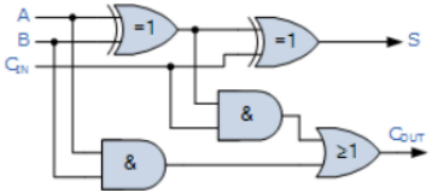


Figure 32 – Full Adder logic gates

(tutorials, 2019)

As the logic gates show above, the full adder has 3 Inputs A, B and Cin. The Sum of the first adder is fed into half adder(2). The C out on the First adder and second adder are fed into the added OR gate. The C in input is then fed into half adder(2) and for the C Out which is combined of both a previous full adder (if there was one) and the Half adder (2) to give a C out, Output.

A Truth table is then made up as shown in figure 33 below showing all possible input and output combinations. And a Boolean expression can be derived.

Inputs			Outputs	
A	B	C – IN	Sum	C - Out
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Figure 33 – Full Adder Truth table

(geeks, 2019)

A 4 bit adder can now be built by connecting 4 full adders together as shown below in figure 34.

4 bit adder design is explained with good images

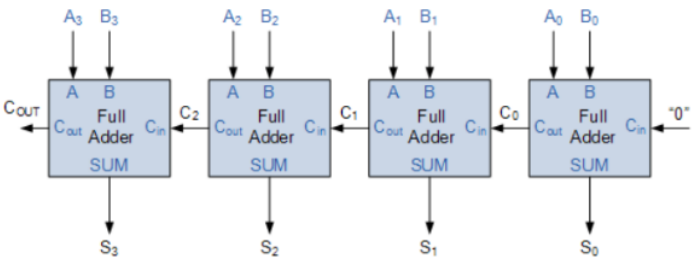


Figure 34 - 4 bit adder block diagram

Following the Design Requirements Using VHDL language and IP Integration in Xilinx Vivado, the structure can be followed to design and Implement using the Nexys FPGA development board.

1.4 Implementation

1.4.1 Half Adder

Using Xilinx Vivado, the Half Adder is designed using VHDL language as shown below in figure 35.

```
1  library IEEE;
2  use IEEE.STD_LOGIC_1164.all;
3  use IEEE.STD_LOGIC_unsigned.all;
4
5  entity halfadder is
6  port (a,b : in std_logic;
7        s,c : out std_logic);
8  end halfadder;
9
10 architecture Behavioral of halfadder is
11
12 begin
13 s <= a xor b;
14 c <= a and b;
15
16 end Behavioral;
```

Figure 35 - Half adder VHDL code

Using the VHDL code for the half adder, the full adder can now be designed. This is done by Duplicating the half adders VHDL code as shown in the Hierarchy shown in figure 36 below.

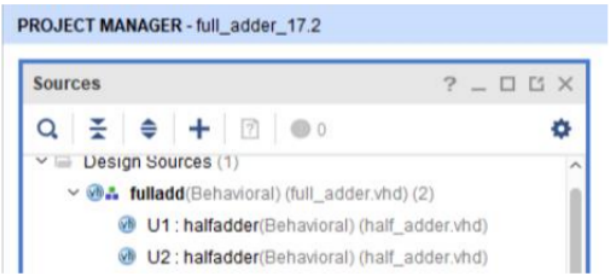


Figure 36 - Full Adder Hierarchy

1.4.2 Full Adder

As shown below in figure 37 is the VHDL code for the Full Adder which is made up of the 2 half adders as shown in lines 26 and 29.

```
5  a : in STD_LOGIC;
6  b : in STD_LOGIC;
7  cin : in STD_LOGIC;
8  cout : out STD_LOGIC;
9  s : out STD_LOGIC
10 );
11 end fulladd;
12 architecture Behavioral of fulladd is
13 component halfadder
14 port (
15 a : in STD_LOGIC;
16 b : in STD_LOGIC;
17 c : out STD_LOGIC;
18 s : out STD_LOGIC
19 );
20 end component;
21
22 signal s1 : STD_LOGIC;
23 signal c2 : STD_LOGIC;
24 signal c1 : STD_LOGIC;
25 begin
26 U1 : halfadder
27 port map(
28 a => a, b => b, c => c1, s => s1);
29 U2 : halfadder
30 port map(
31 a => s1, b => cin, c => c2, s => s);
32 cout <= c2 or c1;
33 end Behavioral;
```

Code is neat and tidy with a good explanation

Figure 37 - Full Adder VHDL code

1.4.3 4-Bit Adder

Using the Full Adder VHDL the 4-Bit adder can now be designed and Implemented. The 4 bit adder is made up of 4 full adders, cascading from one full adder to the next one. As shown below in figure 38, the Hierarchy shows the four full adders used to make up the 4-bit adder.

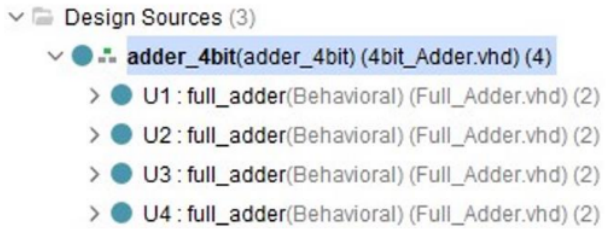


Figure 38 - 4-bit Adder hierarchy

Also shown in figure 39 below is the Hierarchy where the two half adders are used to make up a full adder, which is the same for U2, U3 and U4 full adders.



Source hierarchy is explained in good detail

Figure 39 - 4-Bit Adder Hierarchy

The 4-bit adder VHDL code is shown below in figure 40.

```
1  library IEEE;
2  use IEEE.std_logic_1164.all;
3  entity adder4bit is
4  port(
5  cin : in STD_LOGIC;
6  a0 : in STD_LOGIC;
7  a1 : in STD_LOGIC;
8  a2 : in STD_LOGIC;
9  a3 : in STD_LOGIC;
10
11 b0 : in STD_LOGIC;
12 b1 : in STD_LOGIC;
13 b2 : in STD_LOGIC;
14 b3 : in STD_LOGIC;
15
16 cout : out STD_LOGIC;
17 s0 : out STD_LOGIC;
18 s1 : out STD_LOGIC;
19 s2 : out STD_LOGIC;
20 s3 : out STD_LOGIC
21 );
22 end adder4bit;
```

```
24 architecture adder4bit of adder4bit is
25 component fulladd
26 port (
27 a : in STD_LOGIC;
28 b : in STD_LOGIC;
29 cin : in STD_LOGIC;
30 cout : out STD_LOGIC;
31 s : out STD_LOGIC
32 );
33 end component;
34 signal c1 : STD_LOGIC;
35 signal c2 : STD_LOGIC;
36 signal c3 : STD_LOGIC;
37 begin
38 U1 : fulladd
39 port map(
40 a => a0, b => b0, cin => cin, cout => c1,
41 s => s0);
42 U2 : fulladd
43 port map(
44 a => a1, b => b1, cin => c1, cout => c2,
45 s => s1);
46 U3 : fulladd
47 port map(
48 a => a2, b => b2, cin => c2, cout => c3,
49 s => s2);
50 U4 : fulladd
51 port map(
52 a => a3, b => b3, cin => c3, cout => cout,
53 s => s3);
54 end adder4bit;
```

Code is neat and tidy with no errors

Figure 40 - 4-Bit Adder VHDL code

1.4.4 4-Bit Comparator

The 4-Bit Comparator is a series of logic gates made up to compare 4 bit inputs. The comparator compares the two sets on the 4 inputs which as shown in figure 41 is set A and set B, with 3 outputs which are AGTB,AEQB and ALTB which correspond to the Nexys DDR board.

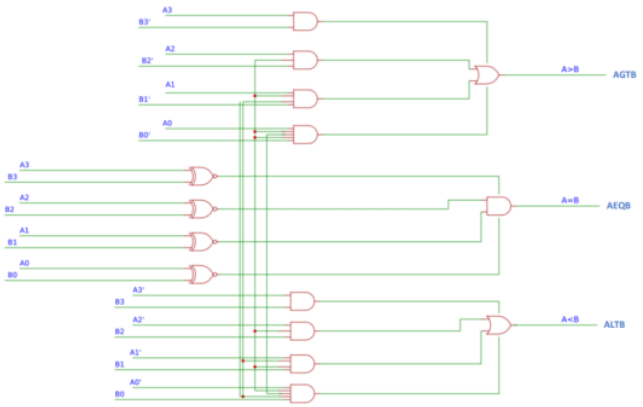


Figure 41 - 4-Bit Comparator

1.4.5 4-Bit Adder and 4-Bit Comparator Combined

To download to the Nexys DDR board the 4 bit adder and the 4 bit magnitude comparator must be combined. This is carried out by using IP Integration, as shown in figure 42 below both the adder and comparator connected accordingly.

IP design is good and backed up with an explanation

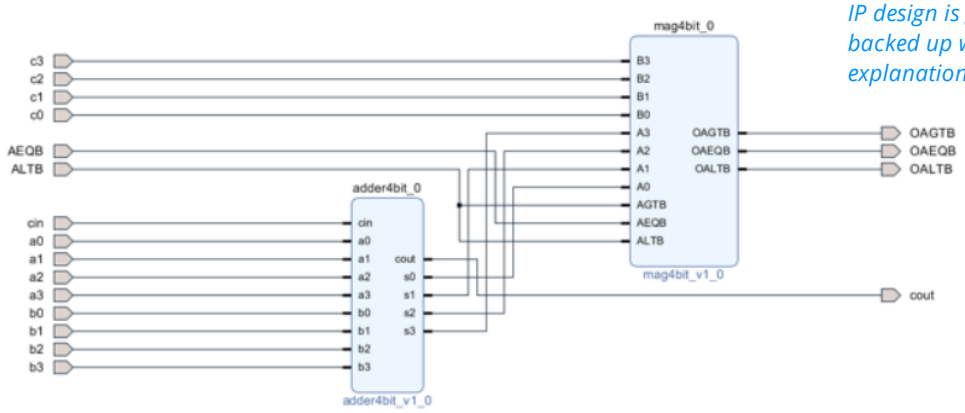


Figure 42 - 4-Bit Adder and 4-Bit Comparator Combined

As shown in figure 42 group C values are fed straight into the 4-bit magnitude comparator. The other 2 sets A and B are fed into the 4-bit adder which are both added together. These values are then compared, and the outputs OAGTB, OAEGB and QALTB indicate whither group C values are greater than, equal to or less than groups A and B combined.

1.4.6 4-Bit Multisim Magnitude Comparator

To carry out simulation and testing of the 4-bit magnitude comparator it was built in Multisim's PLD mode as shown below in figure 43.

AGTB = 0 AEQB = 1 ALTB = 0

Good design using PLD

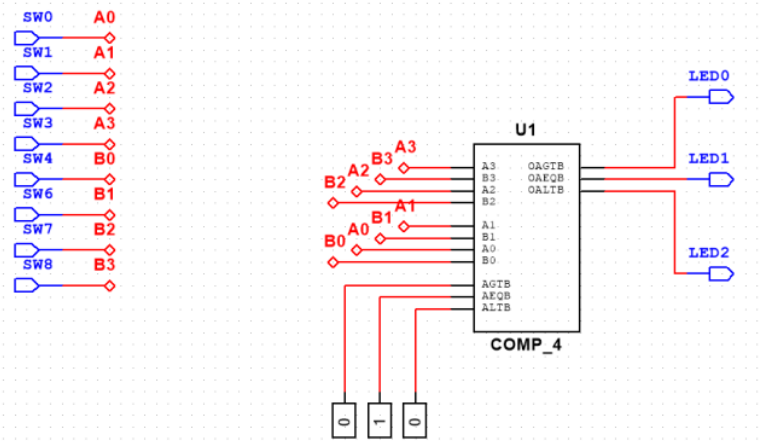


Figure 43 – 4-bit Magnitude comparator multisim PLD

4-Bit adder and Magnitude Comparator testing carried out on page 30.

1.4.7 8 Bit Magnitude Comparator

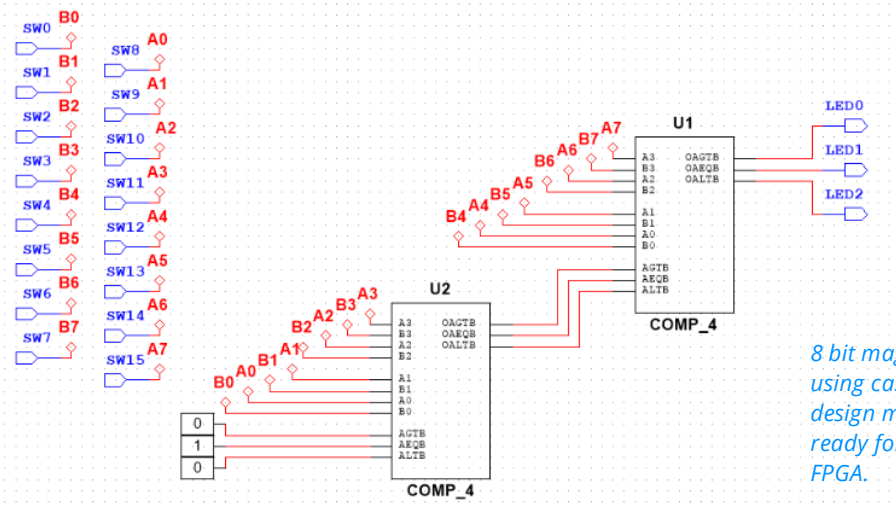
Using the tested 4-bit adder and comparator, this is then duplicated to make an 8-bit comparator in Xilinx Vivado as shown in the Hierarchy in figure 44 below.



Figure 44 - 8 bit adder Vivado hierarchy

To carry out simulation and testing of the 8-bit magnitude comparator it was built in Multisim's PLD mode as shown below in figure 45 where 2 4-bit comparators are connected together.

AGTB = 0 AEQB = 1 ALTB = 0



8 bit magnitude comparator using cascading IC's in PLD design mode is correct and ready for implementation with FPGA.

Figure 45 - 8-Bit magnitude comparator multisim PLD

1.5 Testing and Analysis

Each stage is tested to ensure the design is correct and working as it should :-

1.5.1 4-Bit testing and Analysis

Using the VHDL test code obtained, Tests were carried out on the 4-Bit Adder using the test bench mode. Firstly the test code shown in figure 46 was pasted into Vivado.

```
a0 <= '1';
a1 <= '0';
a2 <= '0';
a3 <= '0';
b0 <= '1';
b1 <= '0';
b2 <= '0';
b3 <= '0';
cin <= '0';
wait for 10 ns;
 a0 <= '1';
 a1 <= '1';
 a2 <= '1';
 a3 <= '0';
 b0 <= '0';
 b1 <= '0';
 b2 <= '1';
 b3 <= '0';
cin <= '0';
wait for 10 ns;
```

Good set of test data

Figure 46 - Vivado test bench VHDL code

Run Synthesis was used to check for error which showed none, so Simulation was run and the results shown below in figure 47.

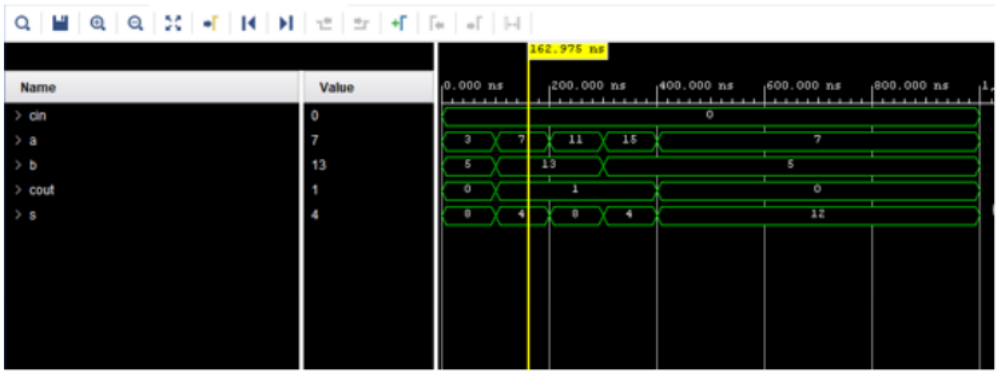


Figure 47 - 4-Bit adder test bench simulation

Very good test results using the virtual bus method. The carry out bit is set to logic 1 for the overflow bit.

The data arrays where converted into virtual bus, as you can see by the simulation above the 4-Bit adder is working as it should. The input values a and b which are represented in binary are varied and tests were carried out showing the output expected and simulated results shown in Table 1 below.

4-Bit Adder Results											
A			B			Expected			Simulated		
Binary	Decimal	Cin	Binary	Decimal	Cin	Binary	Decimal	Cin	Binary	Decimal	Cin
0011	3	0	0101	5	0	1000	8	0	1000	8	0
0111	7	0	0101	5	0	1100	12	0	1100	12	0

Table 1 - 4-Bit Adder Test results

As the table above shows the simulated results are the same as the expected, which prove that the 4-Bit adder is working correctly.

This now allows us to download to the FPGA Nexys 4 DDR board for further testing.

No test has been carried out for the 4 bit comparator using Vivado

Using the FPGA board 3 further tests were carried out which were :-

A>B A=B A<B

On the FPGA board the output LEDs where used to indicate each test using AGTB,AEQB and ALTB as derived below :-

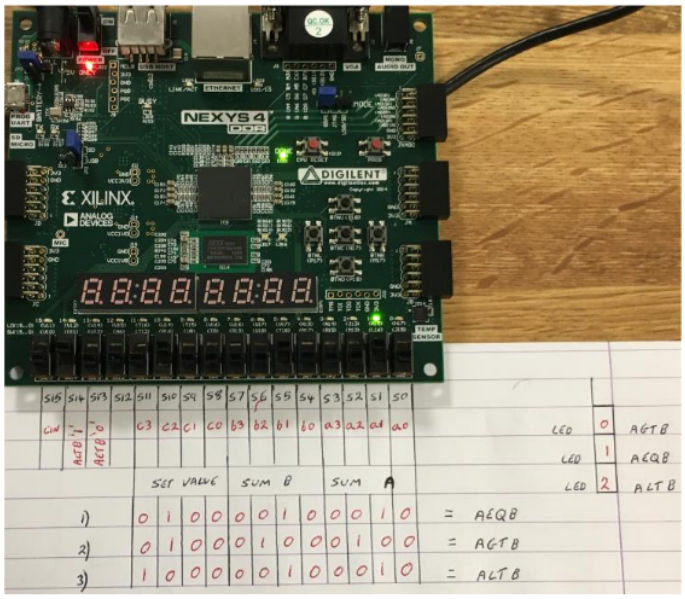
A>B = AGTB = LED 0

A=B = AEQB = LED 1

A<B = ALTB = LED 2

This needs a heading to explain what is being tested and its purpose. This is the 4 bit adder and 4 bit comparator test using FPGA.

To test A equal to B the FPGA Nexys 4 DDR board is shown below in figure 48.



Good test result

Figure 48 - 4-Bit Adder FPGA Board Test A=B

As show in figure 48, the switches where switched on corresponding to a binary code in Set value, sum A and Sum B shown in the table, Which illuminates LED 1 (AEQB) to show A is equal to B.

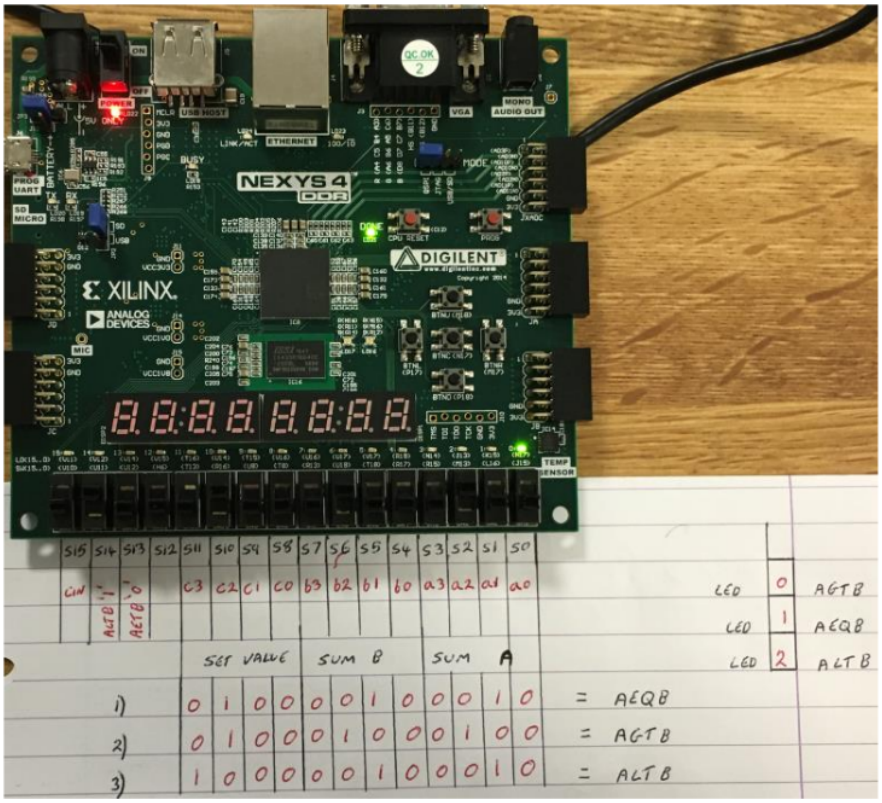
As shown in table 2 below the (Sum of A + Sum of B = 4) which is equal to the set value of 4.

AEQB	Test 1 A=B		
	Set Value	Sum of B	Sum of A
Binary	0100	0010	0010
Value	4	2	2

Table 2- Test 1 A=B

Good use of table. The set value is compared against the sum of A+B. The A=B term is misleading.

To test A greater than B the FPGA Nexys 4 DDR board is shown below in figure 49.



Good test result

Figure 49 - 4-Bit adder FPGA board test A>B

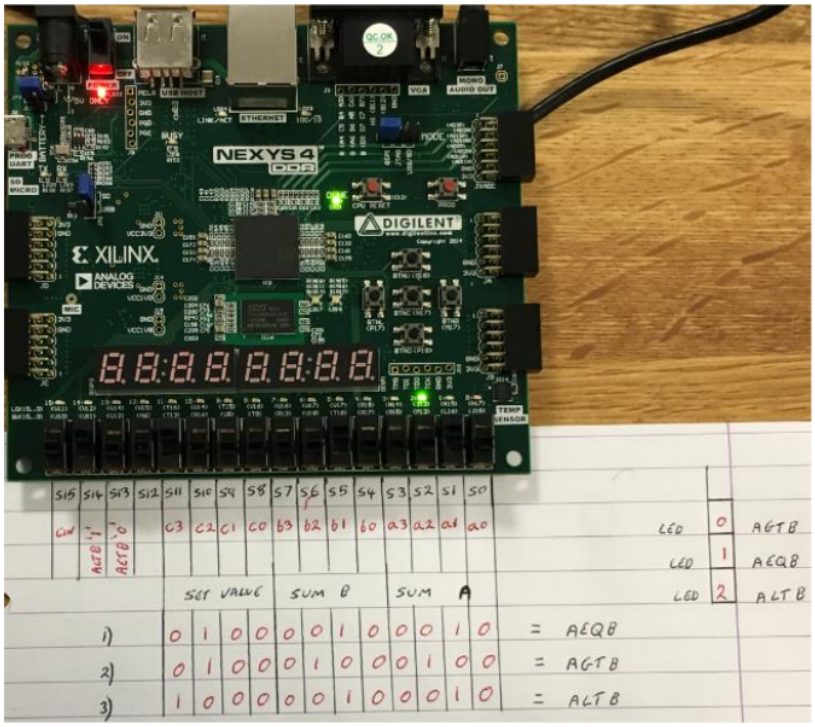
As show in figure 49, the switches where switched on corresponding to a binary code in set value, sum A and Sum B shown in the table, Which illuminates LED 0 (AGTB) to show A is greater than B.

As shown in table 2 below the (Sum of A + Sum of B = 8) which is greater than the set value of 4.

AGTB	Test 2 A>B		
	Set Value	Sum of B	Sum of A
Binary	0100	0100	0100
Value	4	4	4

Table 3 - Test 2 A>B

To test A Less than B the FPGA Nexys 4 DDR board is shown below in figure 50.



Good test result

Figure 50 - 4-Bit adder FPGA board test A<B

As show in figure 50, the switches where switched on corresponding to a binary code in set value, sum A and Sum B shown in the table, Which illuminates LED 0 (ALTB) to show A is Less than B.

As shown in table 4 below the (Sum of A + Sum of B = 4) which is Less than the set value of 8.

ALTB	Test 3 A<B		
	Set Value	Sum of B	Sum of A
Binary	1000	0010	0010
Value	8	2	2

Table 4 - Test 3 A<B

1.5.2 4-Bit Adder and 4-Bit Comparator combined testing

All Testing carried out on the 4-Bit Adder indicates that its working as it should and meets all requirements.

The combine circuit shown in Figure 42 page 21 shows the 4-Bit Comparator combined with the 4-bit adder.

Below in figure 29 shows the Magnitude comparator sim testing and the test bench data below.

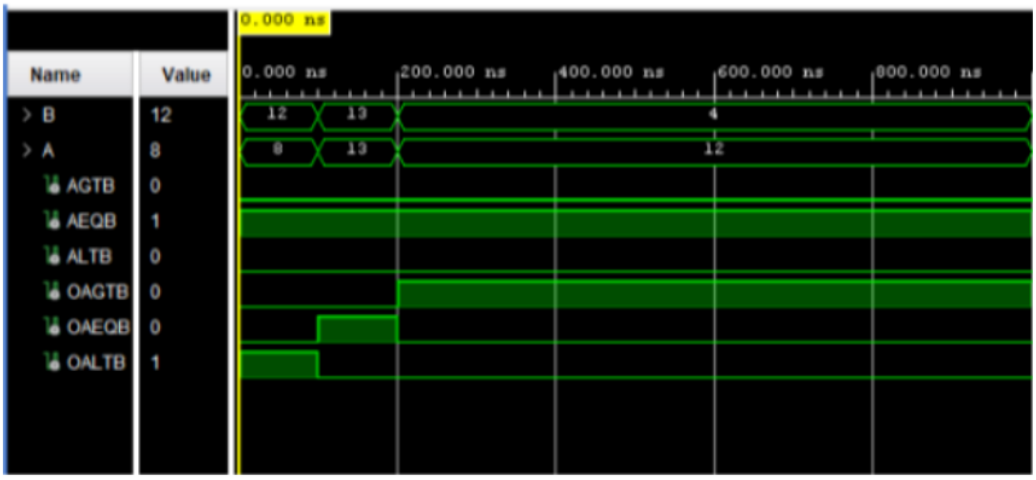


Figure 51 - Magnitude Comparator Sim Testing

Good test results showing all 3 states

Test Bench Data :-

```
B3 <= '1';
B2 <= '1';
B1 <= '0';
B0 <= '0';
A3 <= '1';
A2 <= '0';
A1 <= '0';
A0 <= '0';
AGTB <= '0';
AEQB <= '1';
ALTB <= '0';
wait for 100 ns;
B3 <= '1';
B2 <= '1';
B1 <= '0';
B0 <= '1';
A3 <= '1';
A2 <= '1';
A1 <= '0';
A0 <= '1';
AGTB <= '0';
AEQB <= '1';
ALTB <= '0';
wait for 100 ns;
```

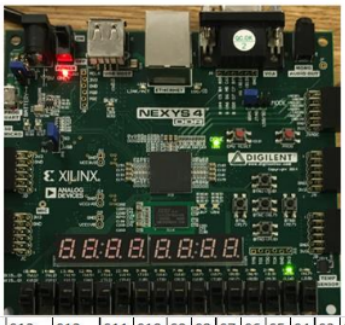
```
B3 <= '0';
B2 <= '1';
B1 <= '0';
B0 <= '0';
A3 <= '1';
A2 <= '1';
A1 <= '0';
A0 <= '0';
AGTB <= '0';
AEQB <= '1';
ALTB <= '0';
wait for 100 ns;
```

Test data is very good

The 4-bit adder and the 4-bit comparator combined circuit is now downloaded to the FPGA Nexys 4 DDR board for practical testing. As shown below a further 3 tests were carried out.

Practical Test 1

The Switches switched according to Test 1 Binary code as figure 51 shows. Which shows that the sum of a and b are equal to B which is shown by lighting up Led 1 AEQB.



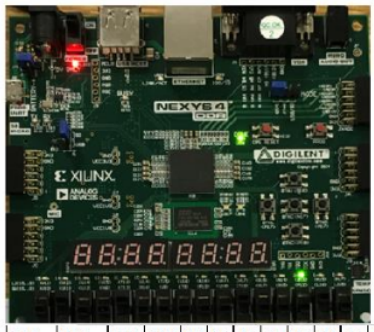
	S15	S14	S13	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1	S0	
	Cin		AGTB	AEQB	B3	B2	B1	B0	b3	b2	b1	b0	a3	a2	a1	a0	
	Inputs				B				b				a				
Test 1	0	0	0	1	1	0	0	0	0	1	0	0	0	1	0	0	LED 1 = AEQB
Test 2	0	0	0	1	0	1	0	0	1	1	0	0	0	0	1	0	LED 2 = AGTB
Test 3	0	0	0	1	1	1	1	0	0	0	1	0	0	1	0	0	LED 0 = ALTB

Figure 52 - 4-Bit adder and Comparator combined Practical test 1

As Figure 51 shows practical Test 1, A=B works as it is designed to do so.

Practical Test 2

The Switches switched according to Test 2 Binary code as figure 52 shows. Which shows that the sum of a and b are greater than B which is shown by lighting up Led 2 AGTB.



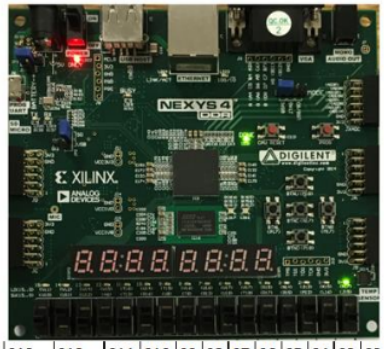
	S15	S14	S13	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1	S0	
	Cin		AGTB	AEQB	B3	B2	B1	B0	b3	b2	b1	b0	a3	a2	a1	a0	
	Inputs				B				b				a				
Test 1	0	0	0	1	1	0	0	0	0	1	0	0	0	1	0	0	LED 1 = AEQB
Test 2	0	0	0	1	0	1	0	0	1	1	0	0	0	0	1	0	LED 2 = AGTB
Test 3	0	0	0	1	1	1	1	0	0	0	1	0	0	1	0	0	LED 0 = ALTB

Figure 53 - 4-Bit adder and comparator combined practical test 2

As Figure 52 shows practical Test 2 A>B works as it should.

Practical Test 3

The Switches switched according to Test 3 Binary code as figure 53 shows. Which shows that the sum of a and b are less than B which is shown by lighting up Led 0 ALTB.



These tests are repeats of the above tests.

	S15	S14	S13	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1	S0	
	Cin		AGTB	AEQB	B3	B2	B1	B0	b3	b2	b1	b0	a3	a2	a1	a0	
	Inputs				B				b				a				
Test 1	0	0	0	1	1	0	0	0	0	1	0	0	0	1	0	0	LED 1 = AEQB
Test 2	0	0	0	1	0	1	0	0	1	1	0	0	0	0	1	0	LED 2 = AGTB
Test 3	0	0	0	1	1	1	1	0	0	0	1	0	0	1	0	0	LED 0 = ALTB

Figure 54 - 4-Bit adder and comparator combined practical test 3

As Figure 53 shows practical Test 3 A<B works as it should

Below shown in Table 5 is the 3 Practical tests and their outcomes for the combined 4-Bit adder and Comparator.

4-bit adder and 4-bit comparator combined Practical test results													
	Inputs			B		b		a		Outputs			
	Cin	AGTB	AEQB	Bit	Value	Bit	Value	Bit	Value	ALTB	AEQB	AGTB	Cout
Test 1	0	0	1	1000	8	0100	4	0100	4	0	1	0	0
Test 2	0	0	1	0100	4	1100	12	0010	2	0	0	1	0
Test 3	0	0	1	1110	14	0010	2	0100	4	1	0	0	0

Table 5 - 4-bit adder and 4-bit comparator combined practical test results

The table is good and shows the test data with results.

As you can see from this table all aspects of the design is proven and shows that it's all working as it is designed to do so.

1.5.3 8-BIT TESTING AND ANALYSIS

To test the 8-Bit Magnitude Comparator it will be firstly built, simulated and tested on multisim, then downloaded to the FPGA Nexys Board for Practical testing. There will be 3 tests carried out on each.

8-Bit Magnitude Comparator shown below in figure 54 :-

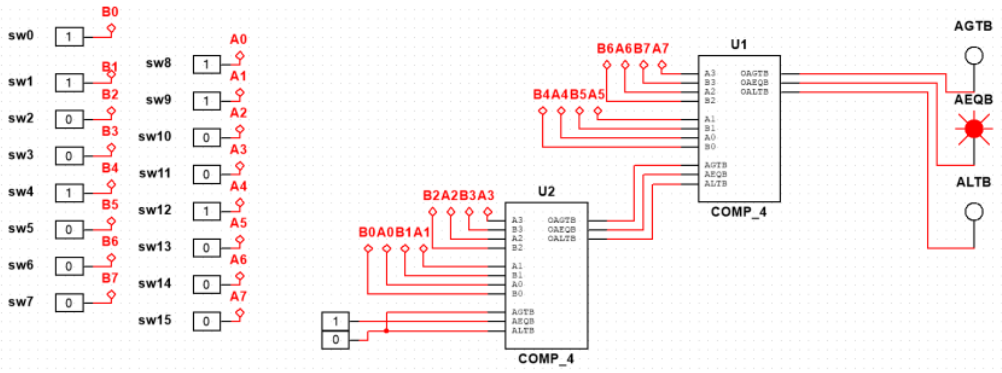


Figure 55- 8-Bit Magnitude Comparator multisim test 1

To carry out these tests the switches in multisim are switched to correspond with the Binary code to test the system and to test AGTB,AEQB and ALTB outputs are corresponding as they should.

Firstly test 1 was carried out on Multisim to test A is Equal to B as shown above in figure 54. Using Binary code shown in Table 6 below, showing values used for the tests and also the expected and actual outcome.

Test 1				
	A	B	Expected	Actual
Binary	11001000	11001000	A=B	A=B
Value	200	200	A=B	A=B

Table 6 - 8 Bit comparator test 1 results A=B

As Table 5 shows above, the 8-Bit comparator works as it should as the Actual results are the same as the Expected result being A=B. Also shown in Figure 54, AEQB LED is Lit indicating this is correct.

Test 2 is carried out on the 8-Bit Magnitude Comparator to test A is greater than B. As shown in figure 55 below the Binary Code is used and the Output AGTB Led has lit.

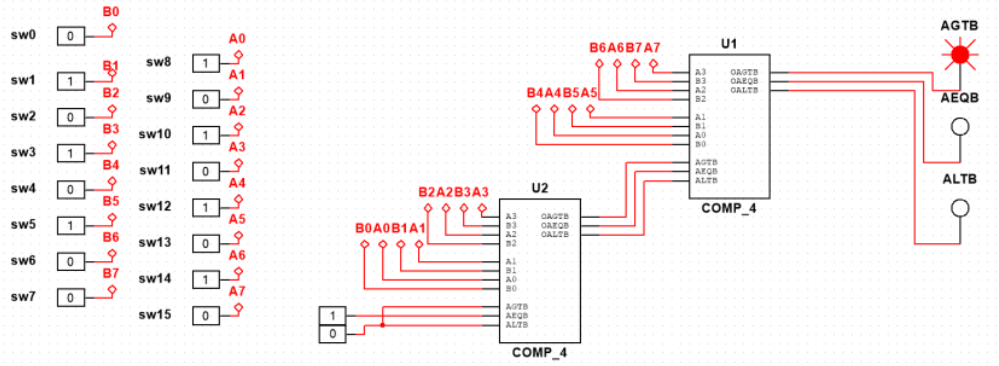


Figure 56 - 8-Bit Magnitude Comparator Multisim Test 2

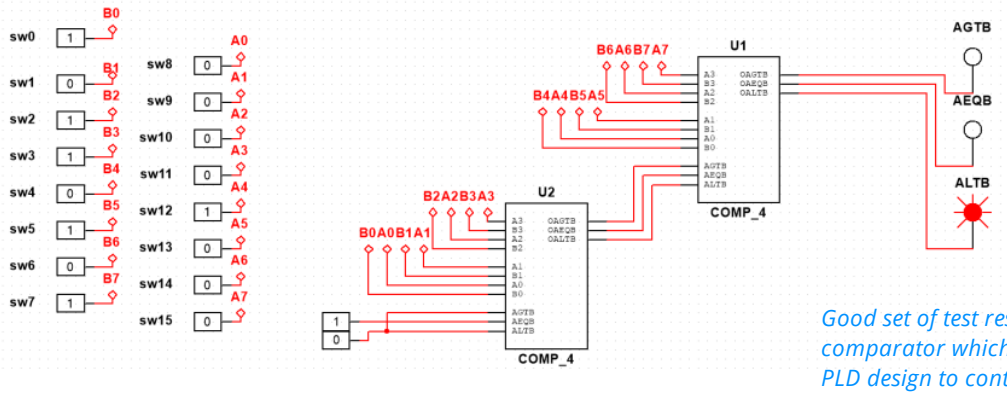
Test 2 was carried out on Multisim to test A is more than B as shown above in figure 55. Using Binary code shown in Table 7 below, showing values used for the tests and also the expected and actual outcome.

Test 2				
	A	B	Expected	Actual
Binary	10101010	01010100	A>B	A>B
Value	170	84	A>B	A>B

Table 7 - 8-Bit comparator test 2 results A>B

As Table 6 shows above, the 8-Bit comparator works as it should as the Actual results are the same as the Expected result being A>B. Also shown in Figure 55, AEQB LED is Lit indicating this is correct.

Test 3 is carried out on the 8-Bit Magnitude Comparator to test A is Less than B. As shown in figure 56 below the Binary Code is used and the Output ALTB Led has lit.



Good set of test results of 8 bit comparator which enables the PLD design to continue

Figure 57 - 8-Bit magnitude comparator multisim test 3

Test 3 was carried out on Multisim to test A is Less than B as shown above in figure 56. Using Binary code shown in Table 8 below, showing values used for the tests and also the expected and actual outcome.

Test 3				
	A	B	Expected	Actual
Binary	00001000	10110101	A<B	A<B
Value	8	181	A<B	A<B

Good use of table

Table 8 - 8-Bit Comparator test 3 results A<B

As Table 7 shows above, the 8-Bit comparator works as it should as the Actual results are the same as the Expected result being A>B. Also shown in Figure 56, AEQB LED is Lit indicating this is correct.

As the Simulated tests are all working as they should be the 8-Bit comparator has now been redesigned as shown in figure 57 below. This is done by using PLD mode so that the inputs and output switches and LEDs correspond with the FPGA Nexys 4 DDR board for practical testing.

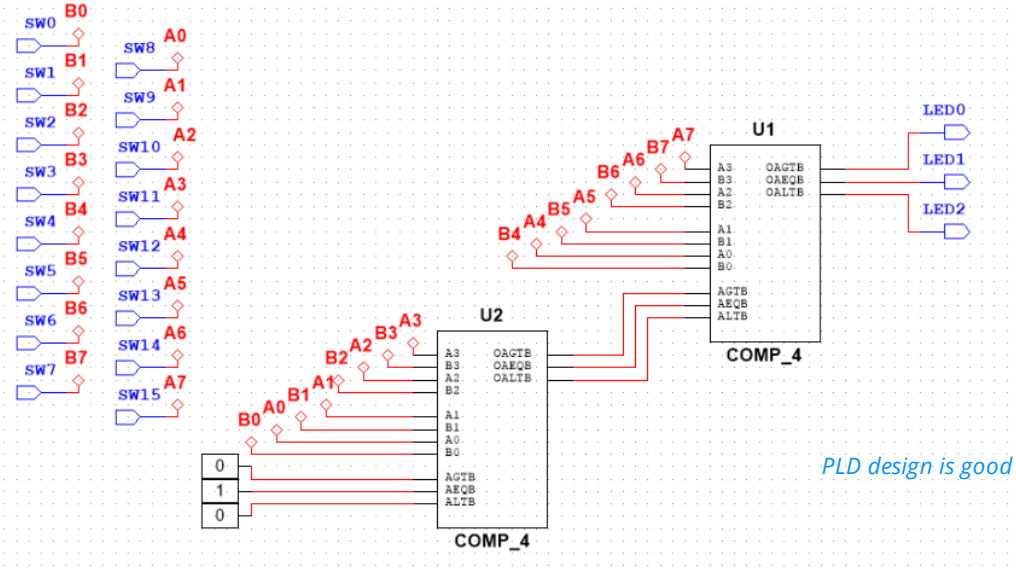
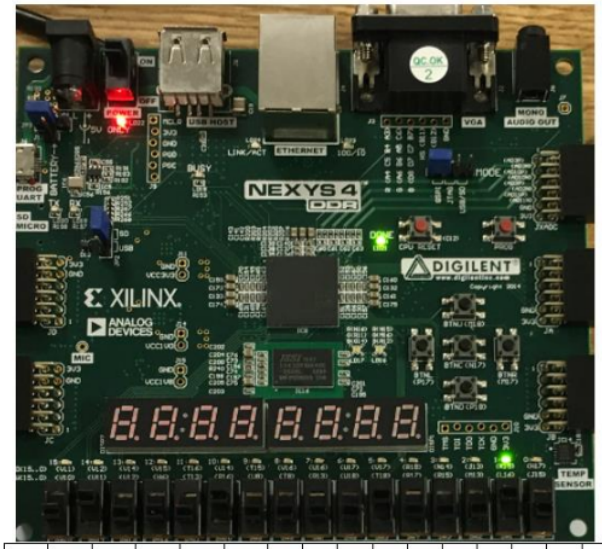


Figure 58 - 8-Bit comparator multsim PLD design

The board was then connected and the program downloaded ready for testing.

8-Bit Magnitude Comparator Practical tests

Practical Test 1 is carried out using the same values shown in Table 6, and the switches switched on the Nexys board to correspond as shown below in figure 58.



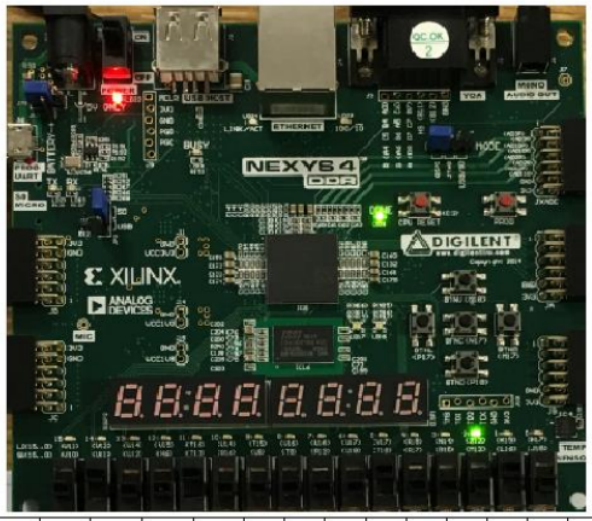
Good test result

	S15	S14	S13	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1	S0	
	SET B								SET A								
Test 1	1	1	0	0	1	0	0	0	1	1	0	0	1	0	0	0	LED 1 = AEQB
Test 2	1	0	1	0	1	0	1	0	0	1	0	1	0	1	0	0	LED 2 = AGTB
Test 3	0	0	0	0	1	0	0	0	1	0	1	1	0	1	0	1	LED 0 = ALTB

Figure 59 - Practical Test 1 Nexys Board

As shown above AEQB Led 1 is lit proving that the A is equal to B and is working as it should.

Practical Test 2 is carried out using the same values shown in Table 7, and the switches switched on the Nexys board to correspond as shown below in figure 59.



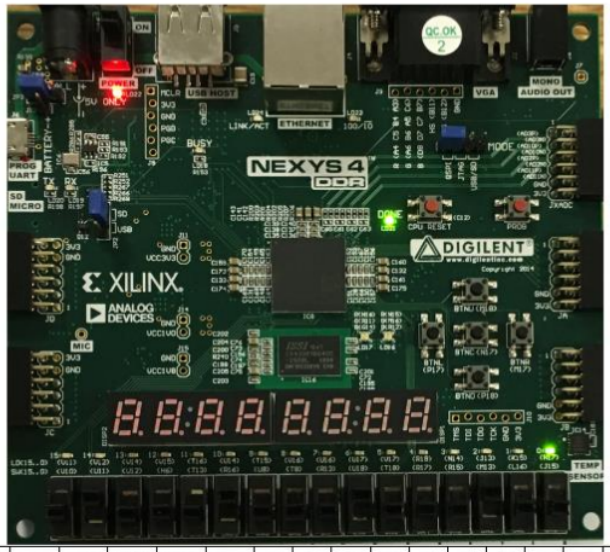
Good test result

	S15	S14	S13	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1	S0	
	SET B								SET A								
Test 1	1	1	0	0	1	0	0	0	1	1	0	0	1	0	0	0	LED 1 = AEQB
Test 2	1	0	1	0	1	0	1	0	0	1	0	1	0	1	0	0	LED 2 = AGTB
Test 3	0	0	0	0	1	0	0	0	1	0	1	1	0	1	0	1	LED 0 = ALTB

Figure 60 - Practical Test 2 Nexys Board

As shown above AGTB Led 2 is lit proving that the A is greater than B and is working as it should.

Practical Test 3 is carried out using the same values shown in Table 8, and the switches switched on the Nexys board to correspond as shown below in figure 60.



Good test result

	S15	S14	S13	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1	S0	
	SET B								SET A								
Test 1	1	1	0	0	1	0	0	0	1	1	0	0	1	0	0	0	LED 1 = AEQB
Test 2	1	0	1	0	1	0	1	0	0	1	0	1	0	1	0	0	LED 2 = AGTB
Test 3	0	0	0	0	1	0	0	0	1	0	1	1	0	1	0	1	LED 0 = ALTB

Figure 61 - Practical Test 3 Nexys board

As shown above ALTB Led 2 is lit proving that the A is Less than B and is working as it should.

All 3 Practical tests carried out above Prove the design and build of the 8-Bit magnitude Comparator works as it should. Also shown below in table 9 are the expected, simulated and Practical test results which prove the process.

8-Bit Magnitude comparator Test Comparison Result table							
	A		B				
	Bit	Value	Bit	Value	Expected	Simulated	Practical
Test 1	11001000	200	11001000	200	A=B	A=B	A=B
Test 2	10101010	170	01010100	84	A>B	A>B	A>B
Test 3	00001000	8	10110101	181	A<B	A<B	A<B

Good use of table to evaluate the overall test results

Table 9 - Practical test on Nexys board results

1.6 Evaluation

A combinational logic system was researched, designed, Implemented and tested using VHDL and IP integration and the Nexys 4 DDR FPGA development board.

Incorrect use of capital letters

This Was done by Designing a Half adder using the VHDL language in Xilinx Vivado, Using the Half adder duplicated a full adder was created as shown in the Hierarchy. This was then simulated and ensured working correctly before creating the 4-Bit adder and 4-Bit Comparator.

The 4-Bit adder was also created using the VHDL language in Xilinx Vivado, This was created by cascading 4 full adders. Simulated tests were carried out using bitstream to ensure it was successful before downloading to the FPGA Nexys 4 DDR board for practical testing. On the Nexys board 3 tests were carried out by using Switching the switches according to the Binary code to prove the system is working correct, which was successful.

As the 4-Bit adder tested Successful the 4-bit adder and 4-bit comparator were IP integrated and connected and added into an IP wrapper. This was then downloaded to the Nexys board and 3 Practical tests carried out which were successful.

The 8-bit magnitude Comparator was then Created in Multisim and simulated. Using the binary code to Input interactive 1/0 bits accordingly and testing each to light the correct Led. Which was proven to be successful proving the system was designed and implemented correctly before practical testing. It was then downloaded to the FPGA Nexys 4 DDR board and 3 further tests carried out to ensure working correctly, which also was proven to be successful.

Each of the stages were simulated and tested and all where successful, proving the design and implementation stages to be correct which now provides the working 8-Bit Magnitude Comparator block within the main assignment objective magnitude comparator.

Despite some grammatical

errors the evaluation covers the element task outcomes

2.0 Element 2

2.1 Introduction

This should be LabVIEW

Element 2 consists of designing, building and testing an instrument circuit in matlab which will replicate a Loadcell which measures 1000gms over a 0-5v range. This will be tested by using labview by firstly generating a signal using the ADC in the range of 0-5v that represents the load from 0- 1000 grams and converted to an 8 bit digital signal and output to the FPGA.
Secondly tested using a signal from a set value in labview, within its range of 0-1000gms and also converted to an 8 bit digital signal and output to the FPGA.

The labview interface will be designed and built for the 8 bit comparator using the ELVIS 11 development board and 3 tests carried out and analysed for three different set points as shown below.

- Below set value

- Equal to set value

- Greater to set value

Good informative introduction

2.2 Design Requirements

2.2.1 Load cells and Signal conditioning

In Figure,,,, below shows a unity gain amplifier which has a chosen 4v input on the negative side and a 6v input on the positive side of the amplifier. The unity gain amplifier construction as shown below is made up of 2 circuits, one side is the amplifiers which act as buffers and an amplifier on the right hand side which used as a differential which explains the 2 inputted voltages. These make up the Unity gain amplifier circuit which ensures the output to stay the same as the inputted magnitude.

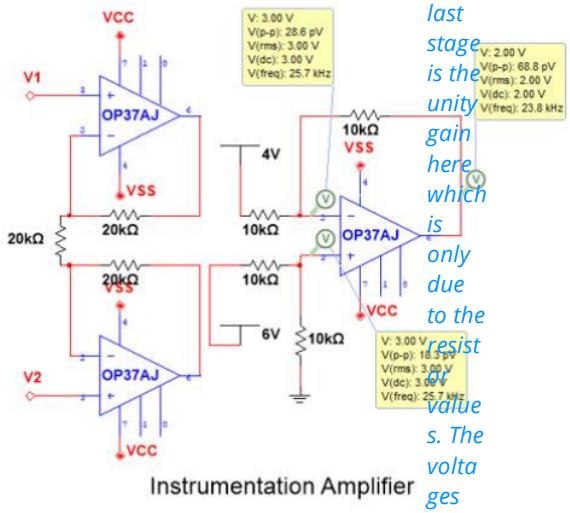
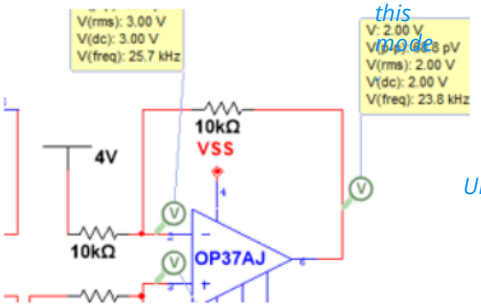


Figure 62 - Unity Gain Amplifier

Only the last stage is the unity gain here which is only due to the resist or value s. The volta ges prove the opera tion in this mode

Because the feedback resistors and input resistors are equal the gain is the difference between the 2 inputs as shown below in figure 63 with a unity gain of 2.



Unity gain is identified here

Figure 63 - Unity Gain Output voltage

As researched in Element 1 the amplifier shown in figure 62 can be used alongside the LCKD loadcell, which as researched the a loadcell works by the changes in resistance as the weight is increased on the loadcell face. As shown in figure 64 below is a multisim model of an instrumentation Amplifier and a circuit representing the LCKD loadcell LCKD-1KG.

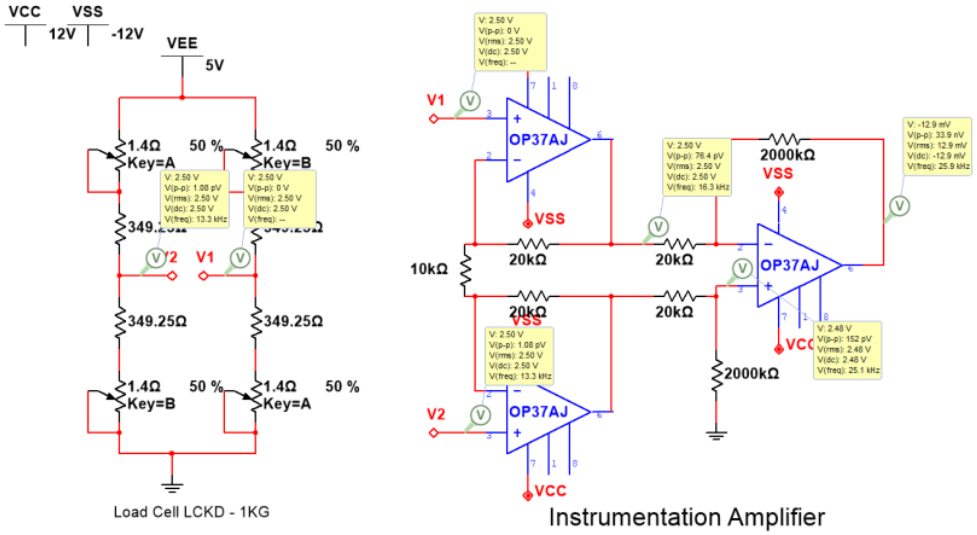


Figure 64 - Simulated load cell and Amplifier circuit

As shown in figure 64 the circuit is produced to simulate the operation of the loadcell and the instrument amplifier. The loadcell is altered to simulate a weight added to the face of the loadcell by altering the potentiometer values by increasing the resistance in one corner and decreasing the opposite corner in a diagonal format which will simulate the loadcell being loaded and the output weight being increased.

The gain required for the circuit shown in figure 64 above can also be calculated as shown in the calculations shown below.

Buffer gain = $1 + \frac{2 \times 20K}{10K} = 5$

Differential Amp Gain = $\frac{2000 \times 10^3}{20 \times 10^3} = 100$

Gain needed is identified by buffer gain and the diff amp gain

Amplifier Gain = 100 × 5 = 500

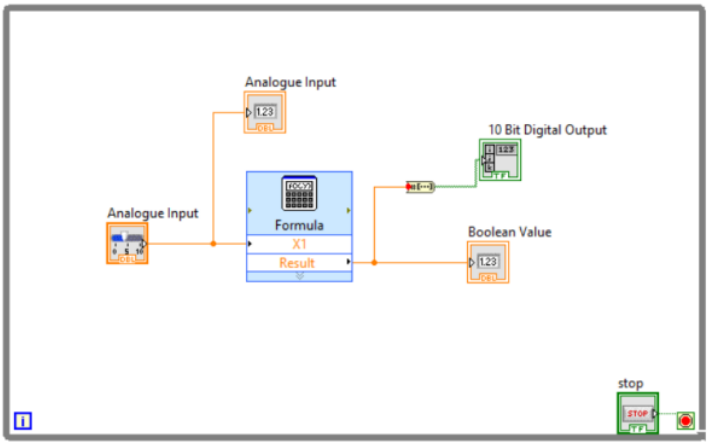
Using the circuit shown in figure 64 in multisim, the loadcell and the amplifier circuit will be tested and signal conditioning carried out in section 2.4 where the loadcell resistor values will be altered to simulate different ranges of load, with the potentiometer values set to 50% as an initial 0 gram output.

Good reference to test and analysis further in report

2.2.4 10 and 12 bit ADC

Using Labview, a 10 bit resolution analogue to digital converter is designed as shown below in figure 65 using the formula in the formula block :-

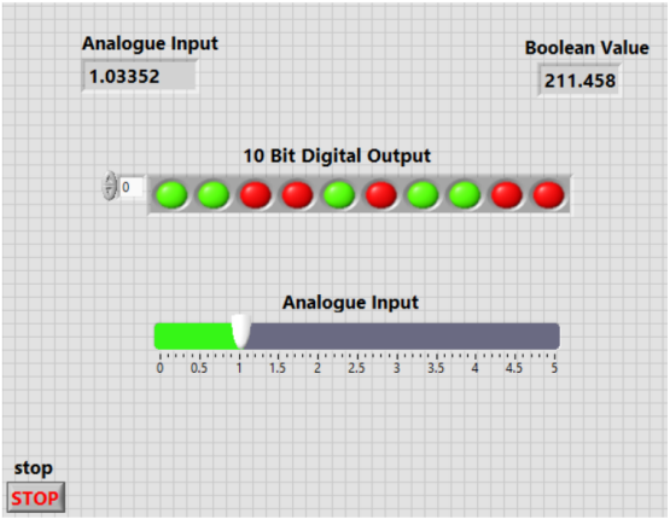
$$\left(\frac{x1}{5}\right) \times 2^{10} = \left(\frac{x1}{5}\right) \times 1024$$



G-code is correct with correct formula

Figure 65 - 10 Bit ADC

An operator screen was created with a slider to adjust the analogue input values from a range of 0 to 5 as shown below in figure 66 so testing could be carried out at various different analogue input values. A 10 bit ADC has a range from 0 to 1023 Boolean value which is altered by the analogue input value on the slider to give the desired output value which is shown in section 2.4 testing and analysis.

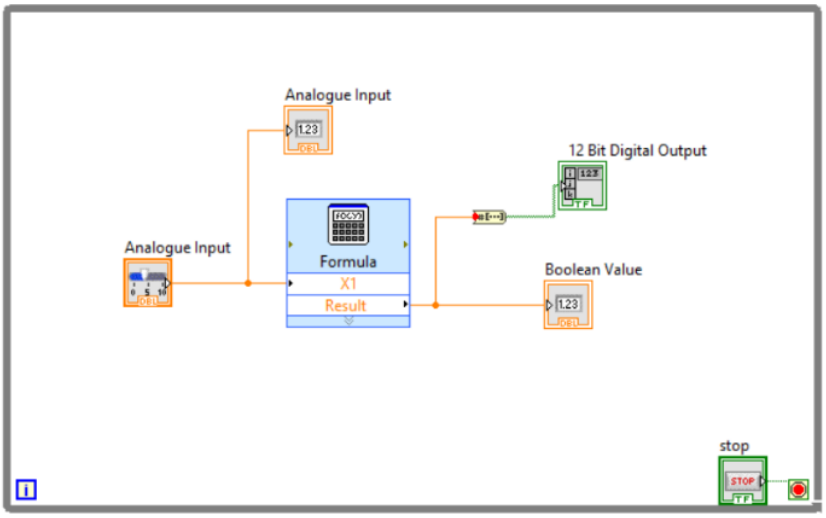


Test is good for 10 bit resolution

Figure 66 - 10 bit ADC front screen

Using Labview, a 12 bit resolution analogue to digital converter is designed as shown below in figure 67 by changing the formula in the formula block to :-

$$\frac{x1}{5} \times 2^{12} = \left(\frac{x1}{5}\right) \times 4096$$



G-code and formula are correct

Figure 67 - 12 Bit ADC

With the 12 bit ADC the formula shows, the possible output Boolean value is increased to 4096 with a range from 0 to 4095. The Front screen was altered to accommodate this by adding the 2 extra digital output LEDs as shown below in figure 68.

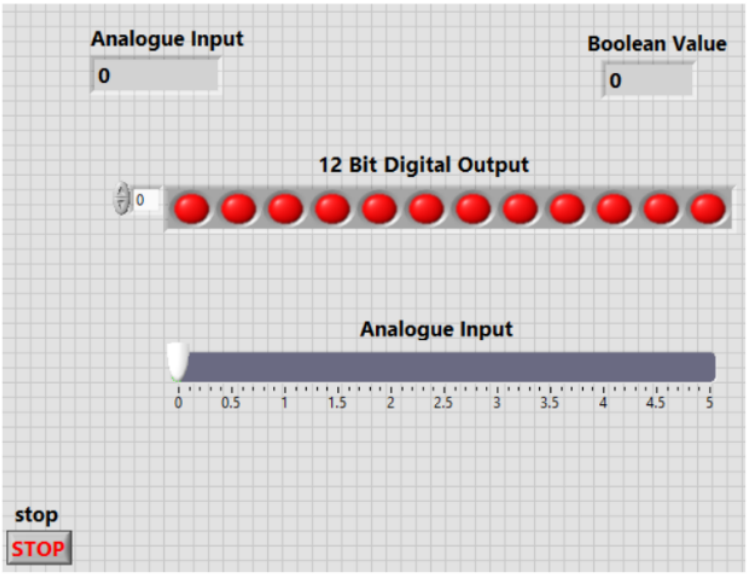


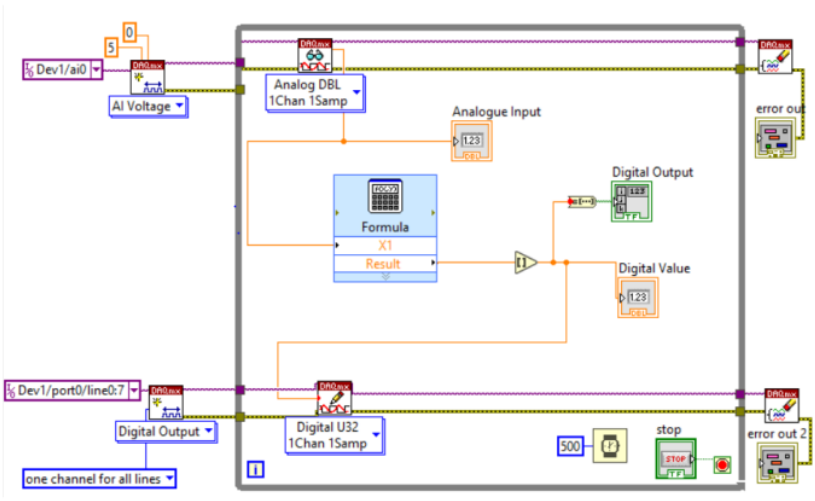
Figure 68 - 12 bit ADC front screen

2.3 Implementation

2.3.1 8 bit ADC implementation

As the testing shows in section 2.4, the 10 bit ADC and 12 bit ADC worked as they should which allows the 8 bit ADC to be implemented and tested on the Elvis II board.
As shown below in figure 69 an 8 bit ADC was created which has a Boolean value output of 256 with a range from 0 to 255 maximum value.

To allow the labview to be compatible with the Elvis II board extra components were added into the block diagram as shown in figure 69 below.



G-code is correct with all data i/o configured

Figure 69 - 8 bit ADC labview

As the 8 bit ADC is designed to be compatible and tested on the Elvis II board the front screen is designed to show the Digital output Led lights and input and output values but no adjustable slider as shown in figure 70 below.

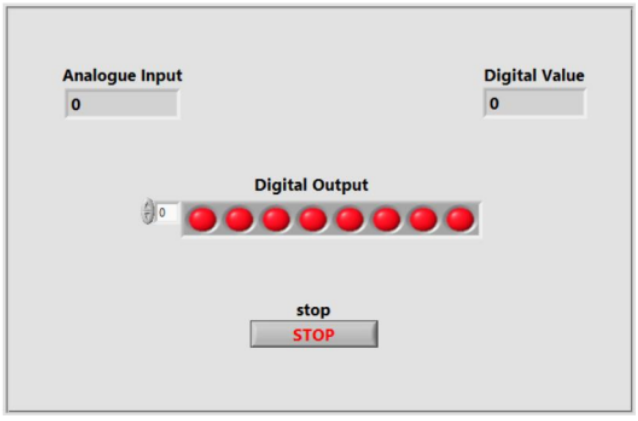


Figure 70 - 8 bit ADC front screen

This is because with the Elvis II board an Instrument control panel was downloaded with labview and the analogue input determined by using the potentiometer shown below in figure 71 which adjusts the input value for testing.



Figure 71 - 8 bit ADC instrument control panel labview

2.3.2 Magnitude comparator

Once the 8 bit ADC was fully tested and working as it should, a magnitude comparator was designed and implemented as shown in the labview block diagram in figure 72 below.

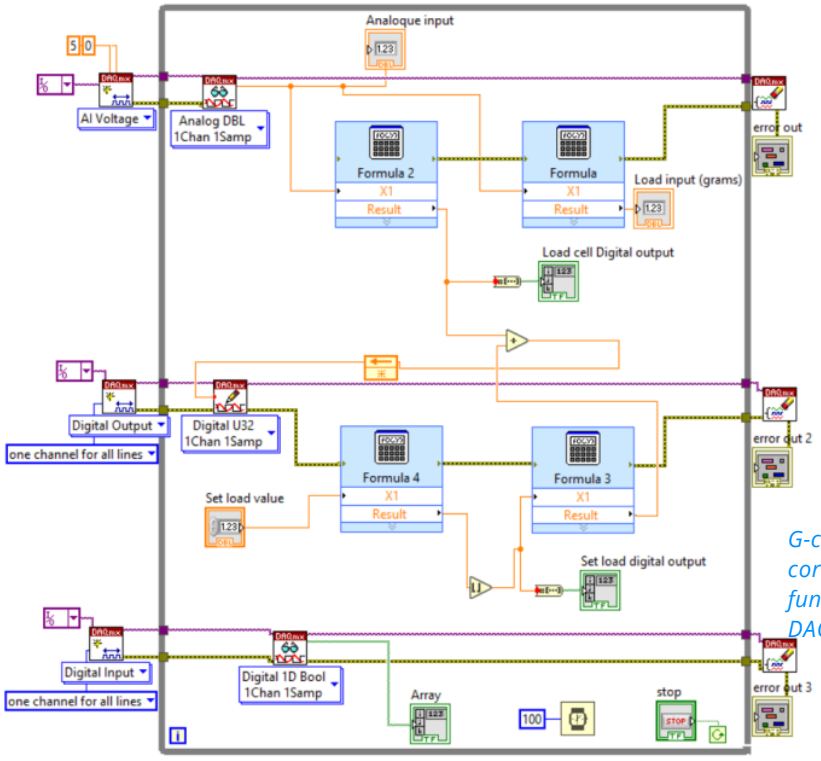


Figure 72 - Magnitude Comparator labview block diagram

G-code program looks correct with all the function blocks for the DAQ implemented

As shown in figure 72 there are 4 formula blocks with 4 different formulas used as shown below :-

Formula block 1 to scale 100 grams with 5V :- (X1/5) × 1000

Formula block 2 to scale 5V with 8 bit resolution :- (X1/5) × 256

Formula block 3 to shift bits over 8 places :- X1 × 256

Formula block 4 to scale input signal to grams (0-1000) :- (X1/1000) × 256

This is how the 16 bits get input to the FPGA single channel

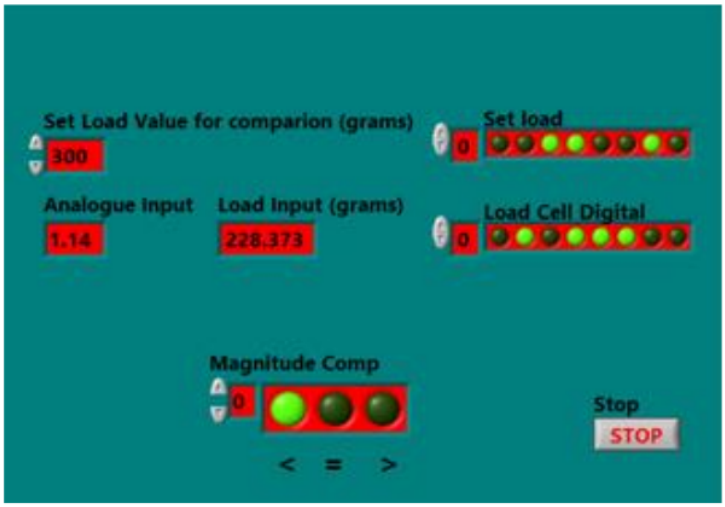
Formula block functions are identified

The lower block diagram within the circuit has no formula block but is used to return the digital input result from the FPGA Magnitude Comparator.

Good explanation for return data result

As shown below in figure 73 the screen was developed which shows the LED indicators and 3 different values. The Analogue input value shows the value which is selected via the pontentiometer for testing. The load input shown in grams which is representing a load value weight and a set load value.

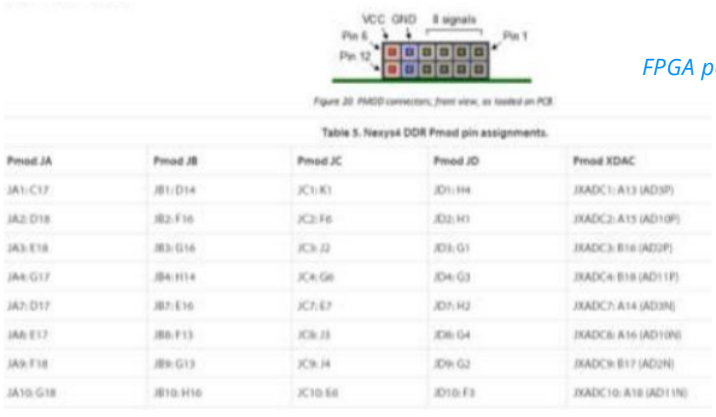
The LED indicators show the load cell digital output value, the set load digital output value and the Array value which indicated weither the output is greater than, less than or equal to.



Good design

Figure 73 - Magnitude comparator front screen labview

To implement and test the magnitude comparator the Elvis II board and the FPGA Nexys board are used using the PLD circuit designed in multisim in figure 55 element 1. The FPGA Nexys board and Elvis II are connected together following the pin allocations on the PMOD ports as shown below in figure 74.



FPGA ports are identified

Table 5. Nexys4 DDR Pmod pin assignments.

Pmod JA	Pmod JB	Pmod JC	Pmod JD	Pmod XDAC
JA1: C17	JB1: D14	JC1: K1	JD1: H4	JXADC1: A13 (AD5P)
JA2: D18	JB2: F16	JC2: F6	JD2: H1	JXADC2: A15 (AD10P)
JA3: E18	JB3: G16	JC3: J2	JD3: G1	JXADC3: B16 (AD2P)
JA4: G17	JB4: H14	JC4: G6	JD4: G3	JXADC4: B18 (AD11P)
JA7: D17	JB7: E16	JC7: E7	JD7: H2	JXADC7: A14 (AD3N)
JA8: E17	JB8: F13	JC8: J3	JD8: G4	JXADC8: A16 (AD10N)
JA9: F18	JB9: G13	JC9: J4	JD9: G2	JXADC9: B17 (AD2N)
JA10: G18	JB10: H16	JC10: K6	JD10: F3	JXADC10: A18 (AD11N)

Figure 74 - PMOD Pin allocation

2.4 Testing and Analysis

2.4.1 Load cells and Signal conditioning

Load cell testing and signal conditioning testing carried out over a range of resistance percentage ranges from 50% to 100% and values recorded. Below shows 3 tests carried out and the rest shown in appendix 5.1.

Resistor values all set to 50% which shows a 0v output (as close as) as shown in figure 75 below.

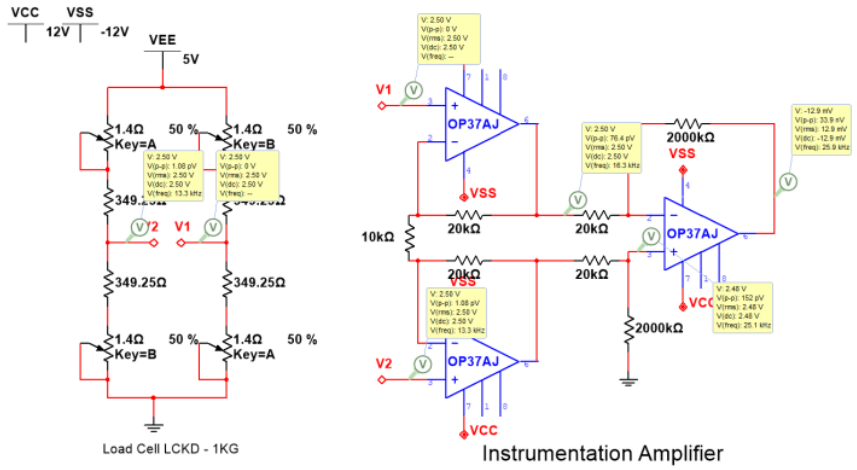


Figure 75 -50%,50%, 50%, 50% loadcell test

Resistor values set to 70%, 30%, 70% and 30% with an output of 1.99v as shown in figure 76 below.

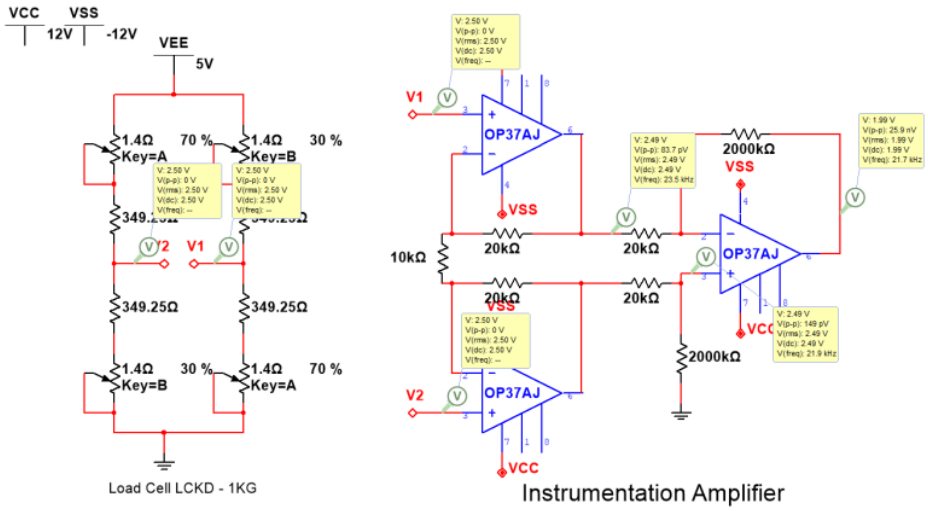


Figure 76 - 70%, 30%, 70%, 30% loadcell test

Resistor values set to 100%, 0% and 100% and 0% which give an output of 5.00V as shown in figure 77 below.

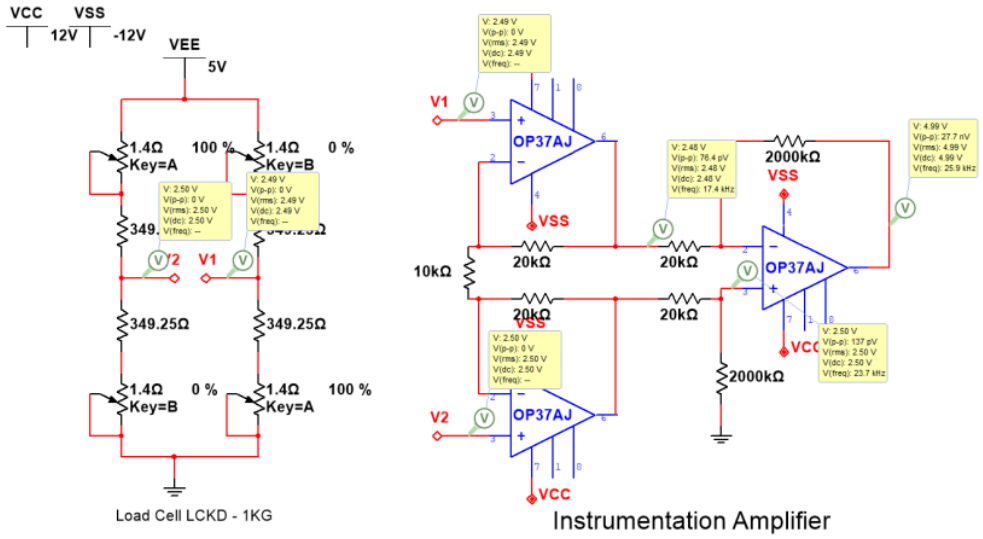


Figure 77 - 100%, 0%, 100%, 0 % loadcell test

All tests carried out are shown in table 10 below.

Signal Conditioning simulated results		
% Resistance	Grams	Voltage
50	0	0.0129
55	100	0.487
60	200	0.987
65	300	1.49
70	400	1.99
75	500	2.49
80	600	2.99
85	700	3.49
90	800	3.99
95	900	4.49
100	1000	4.99

Table 10 - Load cell test table

Good test results and table of resultant values. Good reference to further test results in appendix

Using the results in table 10 above a graph was plotted to show the response with the output voltage compared with the loadcell weight in grams, as shown in figure 78 below.

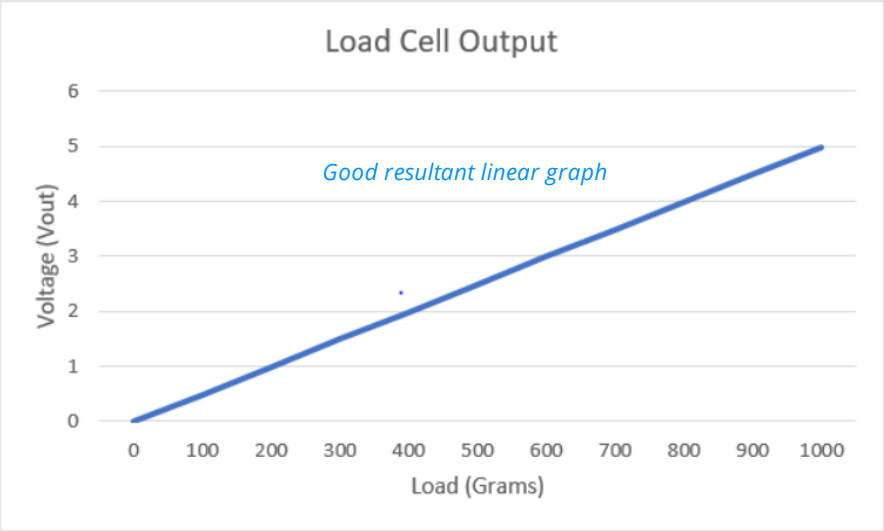


Figure 78 - Load cell output Linear graph

Which shows the graph being linear and showing as the load increases the voltage output increases proportionally.

2,4,2 10 bit and 12 bit ADC testing

To test the 10 bit ADC, the slider on the main front screen was firstly set to 2.5 which is an analogue input signal of 2.5v. As shown in figure 79 below it proves that the correct digital output LED illuminates and the Boolean value corresponds with a value of 511.5.

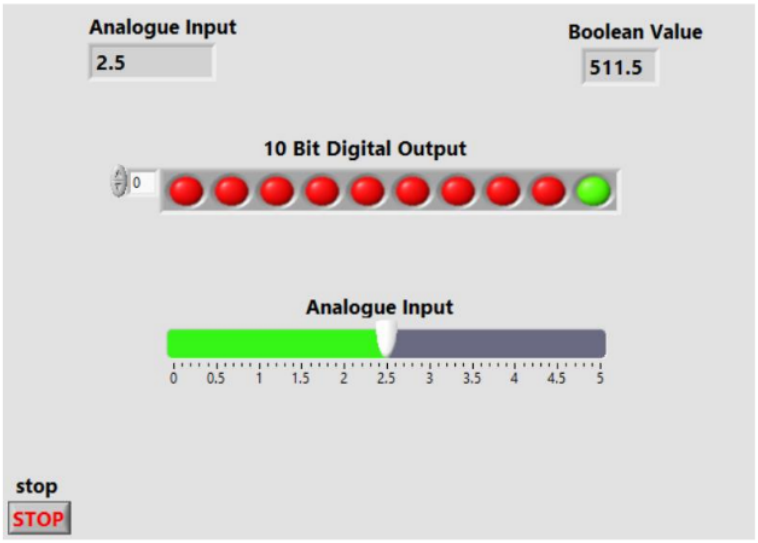


Figure 79 - 10 bit ADC 2.5v input

The slider was then adjusted to input a 5v signal as shown below in figure 80, which shows all the digital LED lit corresponding to the input signal and Boolean value of 1023.

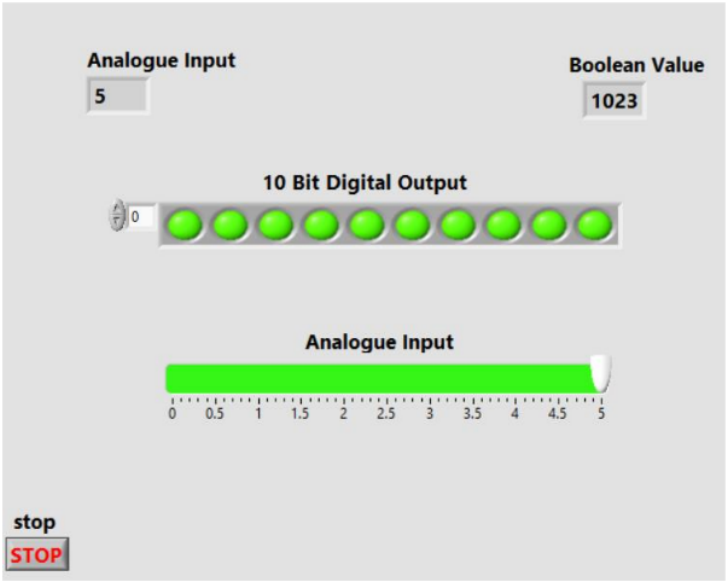


Figure 80 - 10 bit ADC 5.0v input

Good set of results for 10 bit ADC with max value stable

To test the 12 bit ADC, the slider on the main front screen was firstly set to 2.5 which is an analogue input signal of 2.5v. As shown in figure 81 below it proves that the correct digital output LED illuminates and the Boolean value corresponds with a value of 2047.5.

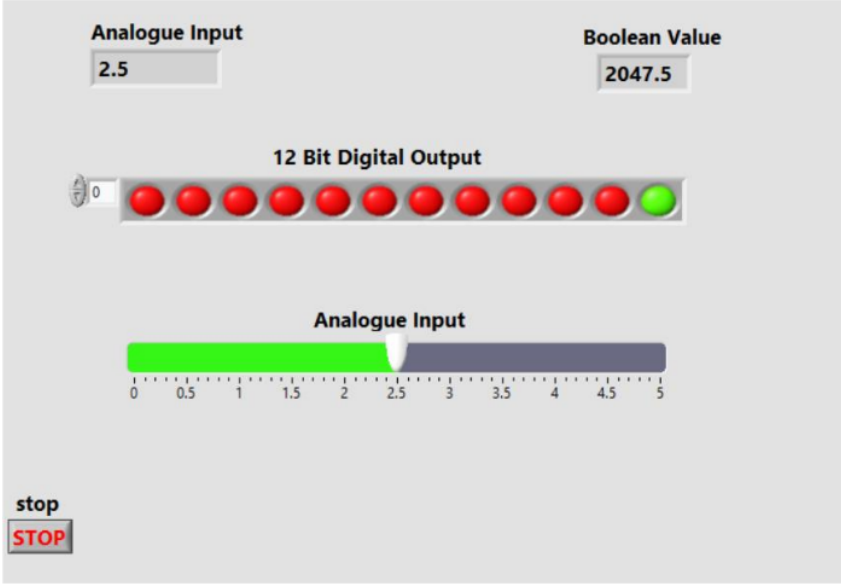


Figure 81 - 12 bit ADC 2.5v input

The slider was then adjusted to input a 5v signal as shown below in figure 82, which shows all the digital LED lit corresponding to the input signal and Boolean value of 4095.

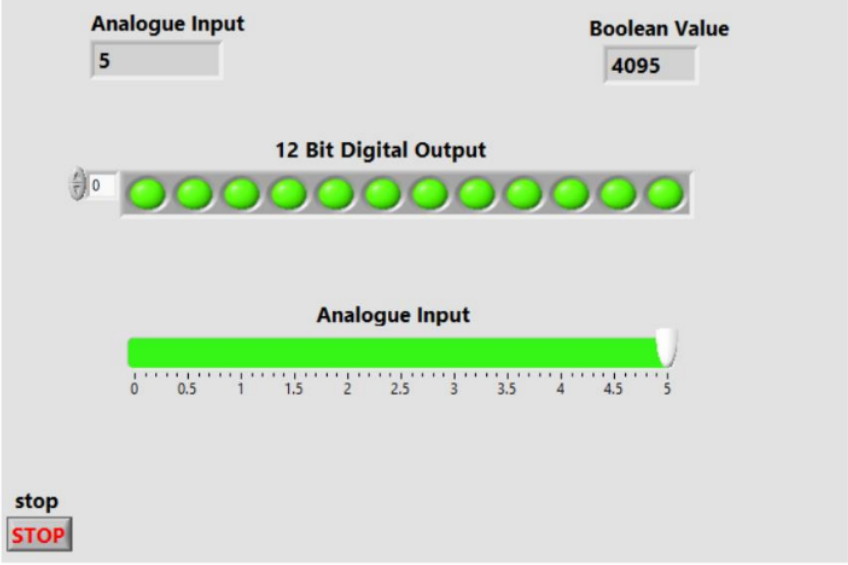


Figure 82 - 12 bit ADC 5v input

Goods

2.4.3 8 bit ADC testing

To test the 8 bit ADC the Elvis II board was used alongside the front screen showing the digital output indicator LEDs and Digital value. The instrument control potentiometer was set to 2.5 volts and as shown in figure 83 the Digital output LEDs correspond to the Digital value of 127.

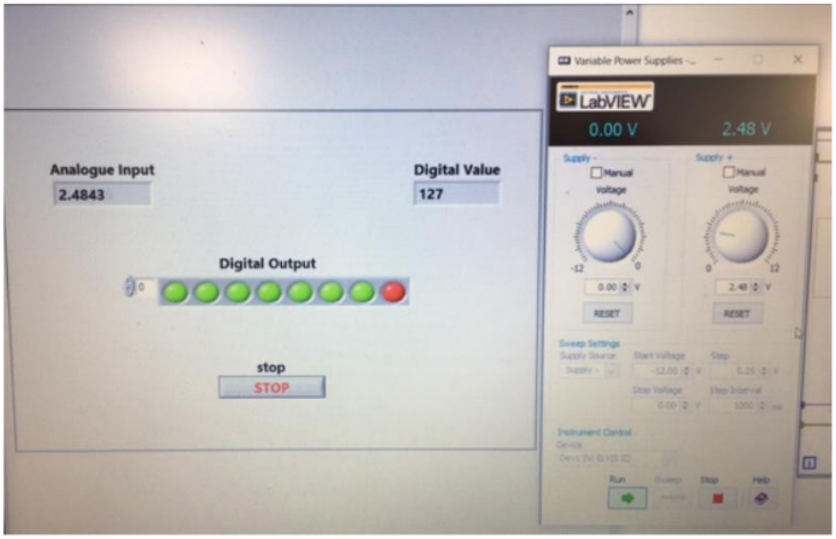


Figure 83 - 8 bit ADC testing 2.5v

As shown below in figure 84 the Elvis II board corresponds to the Digital output value and Led indicators.

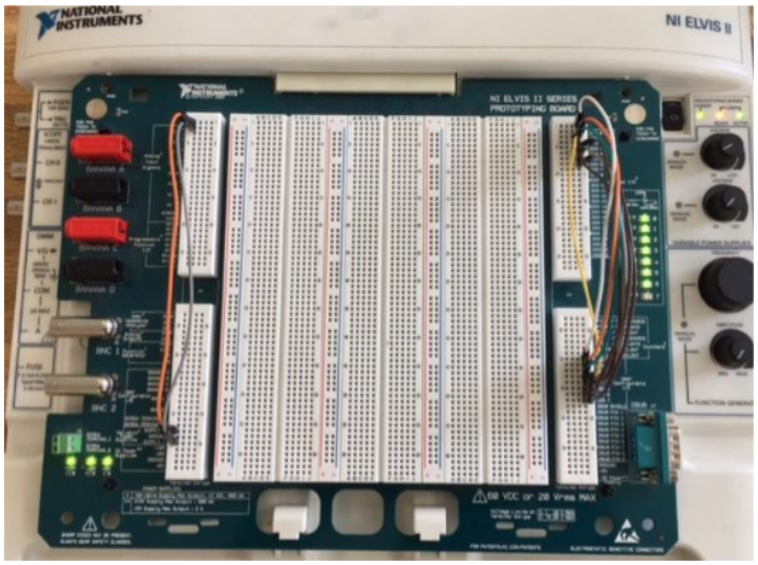


Figure 84 - 8 bit ADC testing Elvis II board 2.5v

The Potentiometer was then adjusted to 5.00v which as shown below in figure 85 the Digital value shows 255 and the Led indicators correspond.

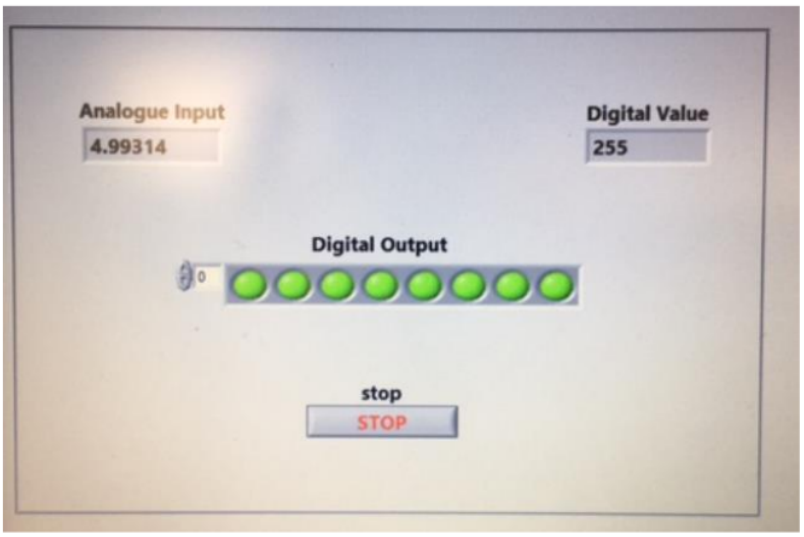


Figure 85 - 8 bit ADC testing 5v

As shown below in figure 86 the Elvis II board corresponds to the Digital output value and Led indicators.

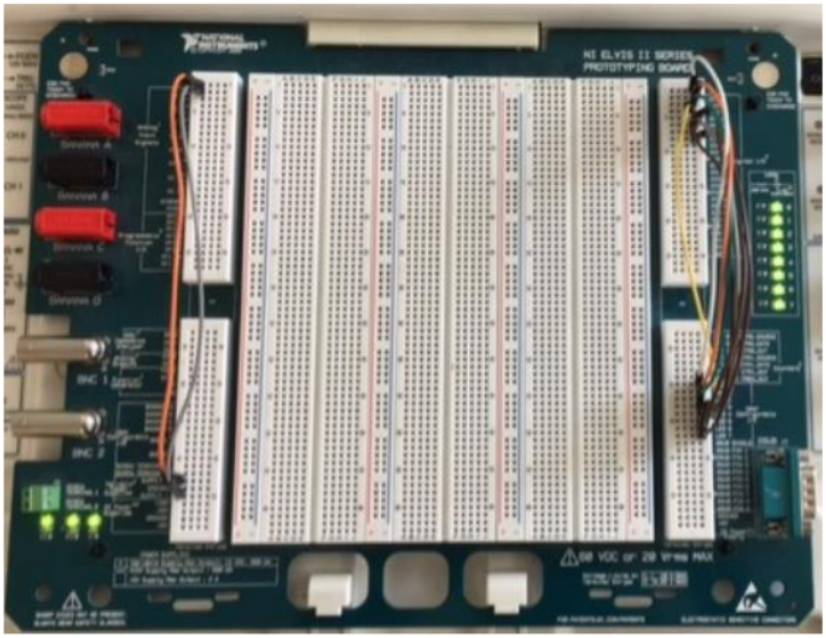


Figure 86 - 8 bit ADC testing Elvis II board 5v

Good set of results for the 8 bit comparator with virtual input

2.4.4 Magnitude comparator

To test the magnitude comparator the FPGA Nexys board was connected to the Elvis II board following the Pinout shown in figure 74 as shown below in figure 87.



Good image of equipment setup

Figure 87 - Magnitude Comparator Nexys/ Elvis II board

Three tests were carried out, ensuring the correct Led indicator lit on both the front screen and the Elvis II board, corresponding to the input to show the possible outputs which are either less than, equal to or greater than.

Firstly the set load value was set to 300 grams, the potentiometer on the Elvis II board was then adjusted to select a load input value of 228.373 grams, which is less than the set load value of 300. As shown the magnitude comparator Indication LED lights up correctly showing less than, on both the front screen shown in figure 88 and the Elvis II board as shown in figure 89 below, proving the system working as it should.

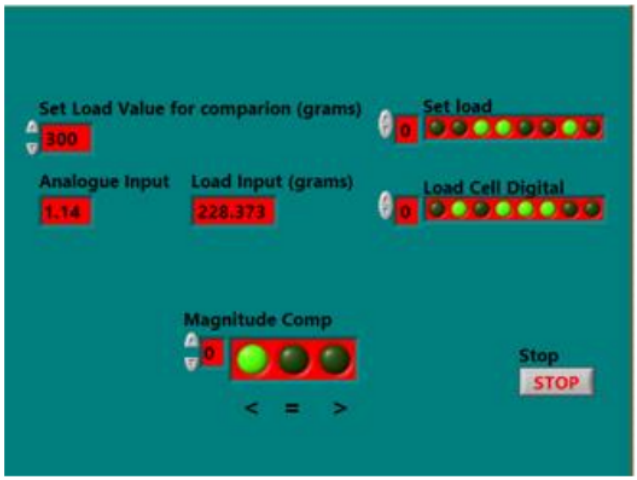


Figure 88 - Magnitude comparator less than test front screen

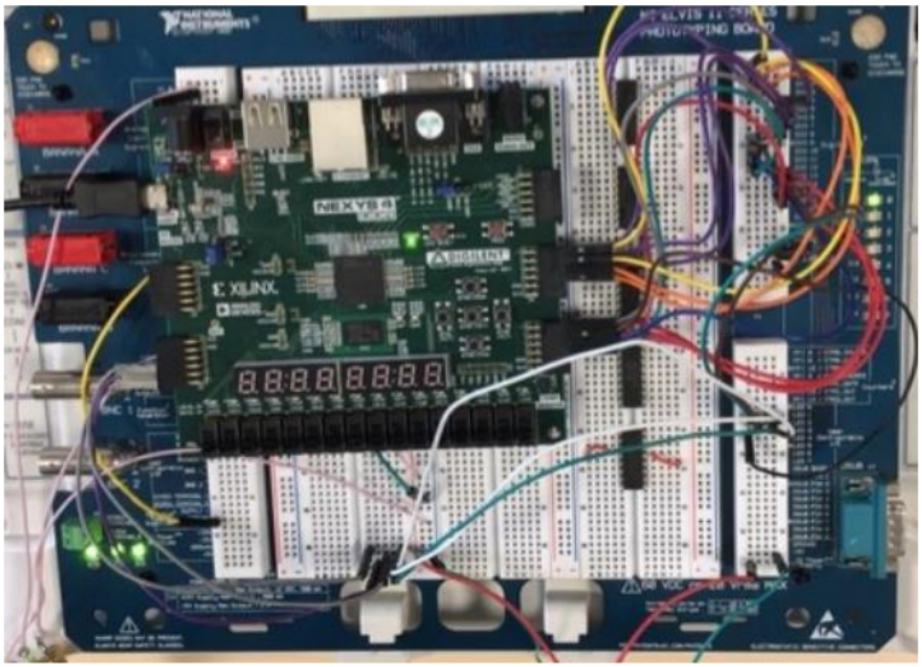


Figure 89 - Magnitude comparator less than test Elvis II board

The set load value remained at 300 grams and the potentiometer on the Elvis II board was then adjusted to select a load input value of 515.622 grams, which is more than the set load value of 300. As shown the magnitude comparator Indication LED lights up correctly showing greater than, on both the front screen shown in figure 90 and the Elvis II board as shown in figure 91 below, proving the system working as it should.

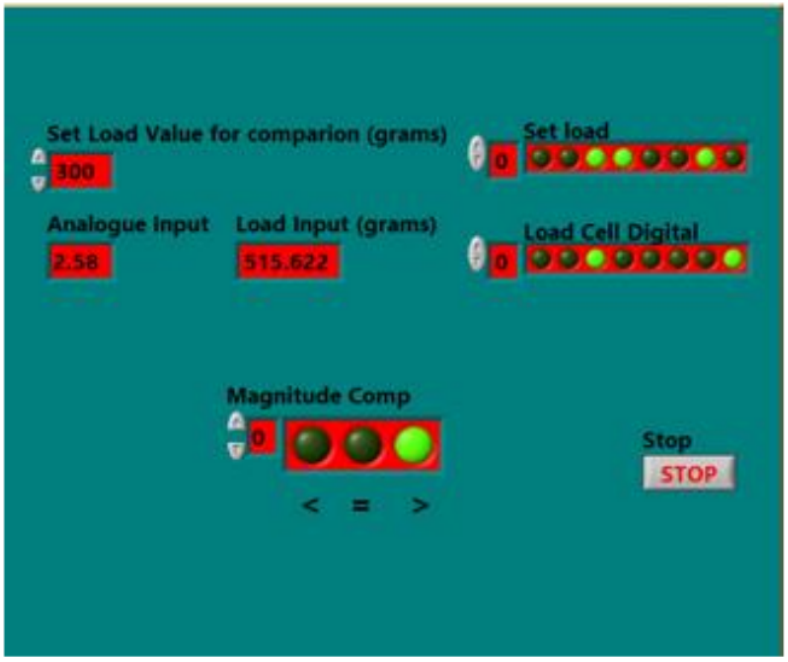


Figure 90 - Magnitude Comparator front screen greater than test

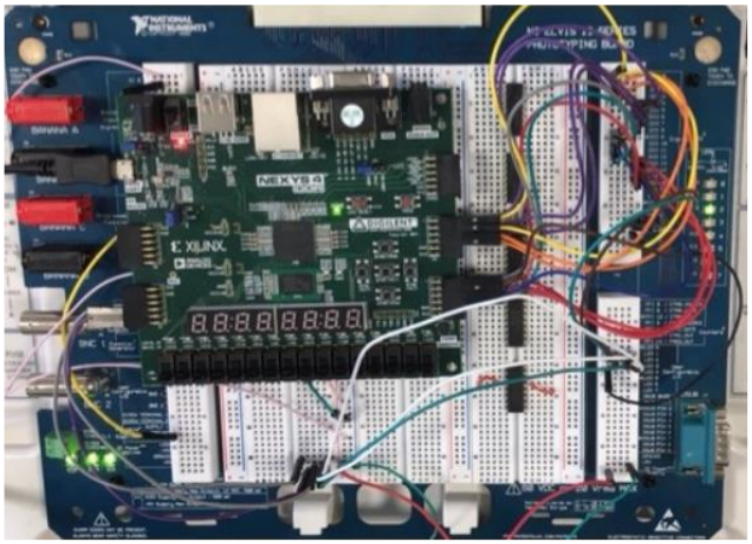


Figure 91 - Magnitude comparator Elvis II board greater than test

The set load value remained at 300 grams and the potentiometer on the Elvis II board was then adjusted to select a load input value of 298.201 grams, which is more or less equal to the set load value of 300. As shown the magnitude comparator Indication LED lights up correctly showing Equal to, on both the front screen shown in figure 92 and the Elvis II board as shown in figure 93 below, proving the system working as it should.

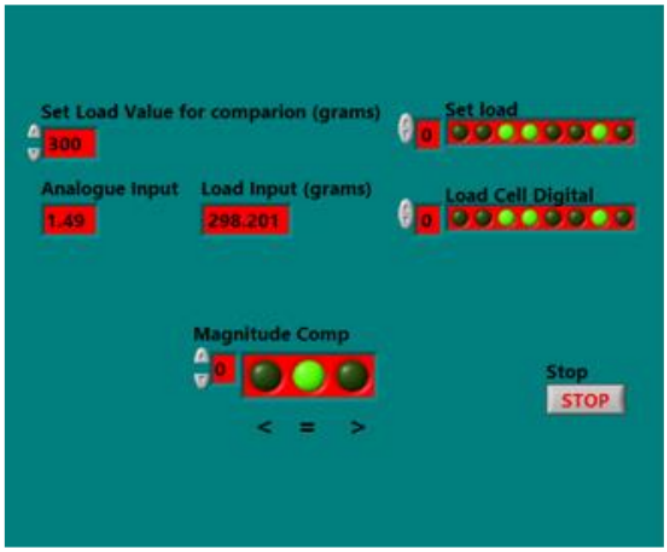


Figure 92 - Magnitude comparator front screen test

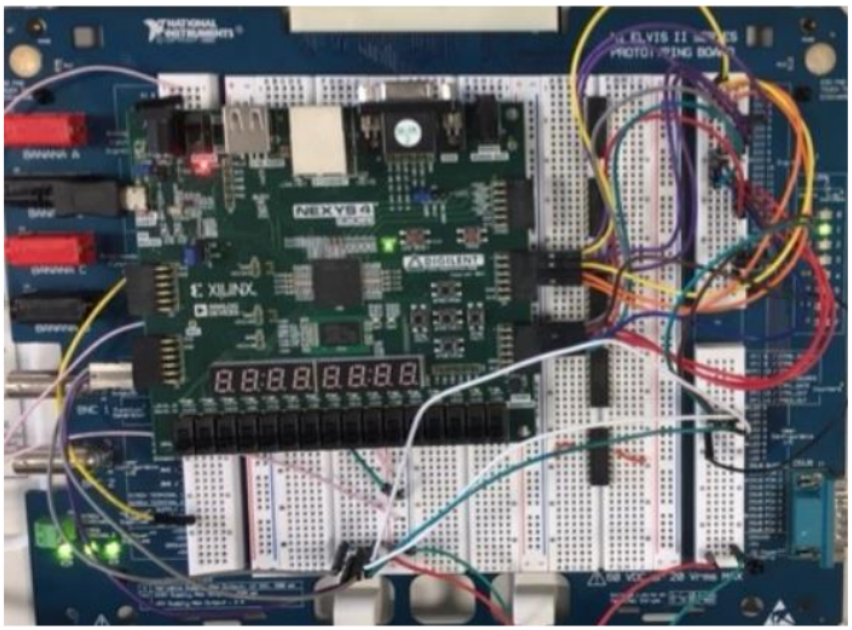


Figure 93 - Magnitude comparator Elvis II equal to test

A good set of results which indicate the correct operation of the system

2.5 Evaluation

Within element 2 an instrument circuit was designed and tested using multisim, simulating a load cell which measured 1000 grams weight load over a 0-5v range. This was tested across a range of different resistor percentages which simulated different loads. A table was produced and as shown in figure 78 a graph was produced showing it was linear, as the load increases the voltage increases proportionally.

Using Labview 3 ADC circuits were designed and tested which generated a signal using the range 0-5V, representing the load from 0 – 1000 grams.
Firstly a 10 bit ADC was designed using the correct formula and tested by adjusting the input from 2.5 volts to 5.0 volts and ensuring the Led indicators corresponded with the analogue input value and the Boolean value.
The formula was changed for the 12 bit ADC but was also designed and tested the same way as the 10 bit ADC.

The 8 bit ADC was designed to be tested with the Elvis II board. The instrument control panel software was used to adjust the input voltage using a potentiometer instead of the slider used with the 10 and 12 bit. The 8 bit ADC was tested by also selecting a 2.5v input and a 5.0v input ensuring the LED indicator lights on the front screen and the Elvis II board correspond to the input value and Boolean value.

comparator is on the FPGA. LabVIEW

The Magnitude comparator was then designed in labview. The FPGA nexys board was connected to the Elvis II board following the correct pin out and was tested by selecting a set point value of 300 grams and by adjusting the potentiometer it was tested over 3 different values which illuminated the Magnitude comparator LEDs corresponding to the analogue input value wither the load input value is less than, greater than or equal to the set point value.

All design, implementation and testing was carried out and all proved to be successful, all values and indication LEDs corresponded to the selected input value and minimal errors throughout Element 2.

With the exception of a minor error / confusion issue the evaluation is good

3.0 Element 3

3.1 Introduction

In Element 3 the Labview design in Element 2 will be adapted to output the actual load cell value in grams over its full range. The comparison values will be used and produced in the form of data logging files.
This will then be used to produce a graph showing actual load over the range for a period of time.

Good introductio n

3.2 Design Requirements

The magnitude Comparator circuit constructed in element 2 is modified to meet requirements of element 3, with the 5 added write to measure blocks added as shown below in figure 94.

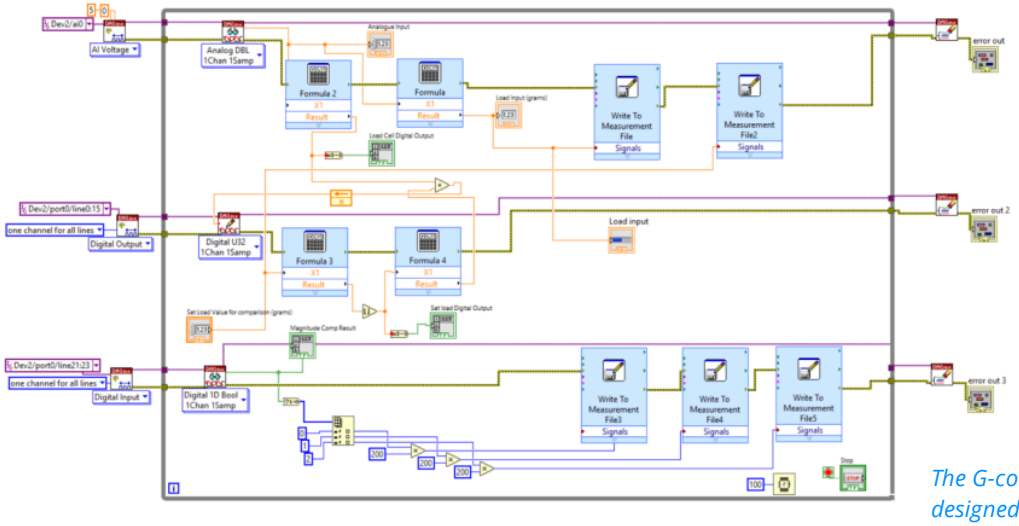


Figure 94 - Element 3 labview block diagram

The G-code is neatly designed and has no errors.

These write to measure blocks are added to record data automatically to a csv text file. Each write to measure file has its own function as shown below :-

File 1 :- Used to log the time line and load in grams
File 2 :- Logs the test value
File 3, 4 and 5 :- Is used to log and scale comparator condition values by using the information data, wither the Input load is less than the set load, equal to the set load or greater than the set load

The Front screen is designed with a Load input slider added as shown below in figure 95.

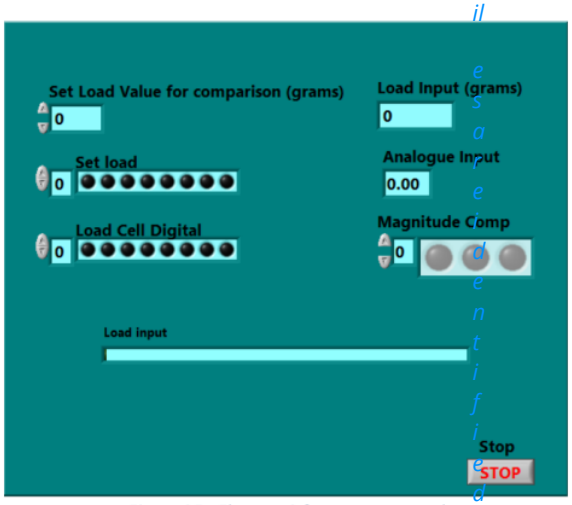


Figure 95 - Element 3 front screen panel

Good design of front panel

Write to file saved identified and explain

3.3 Implementation

The labview design from Element 2 is altered and the write to measure files added as shown in figure 94 above. These files are configured to record the data as a text file by selecting text (LVM).

Firstly file 1 and 2 as shown in figure 96 are configured using the configuration window as shown in appendix 5.2.

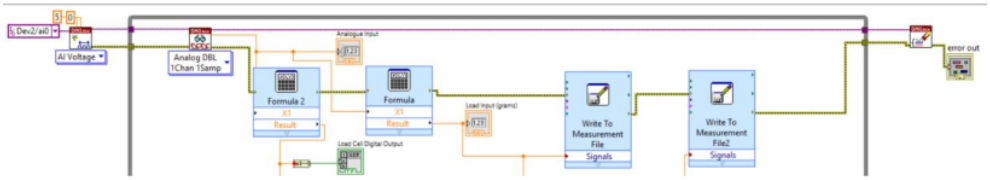


Figure 96 - file 1 and 2 write to measure files

File 3,4 and 5 as shown in figure 97 below are configures using the configuration window as shown in appendix 5.3.

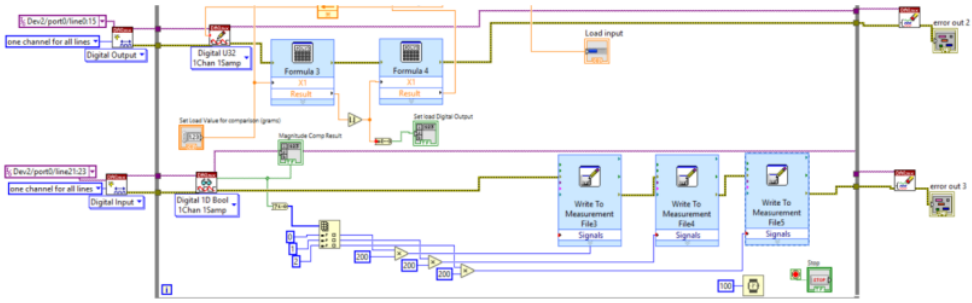


Figure 97 - File 3, 4 and 5 write to measure files

All write to measure files are configured the same way automatically create the lvm text file which records the values to be plotted on the excel graph. Except for file 1 which is configured to produce a time column for the analogue input as the x value.

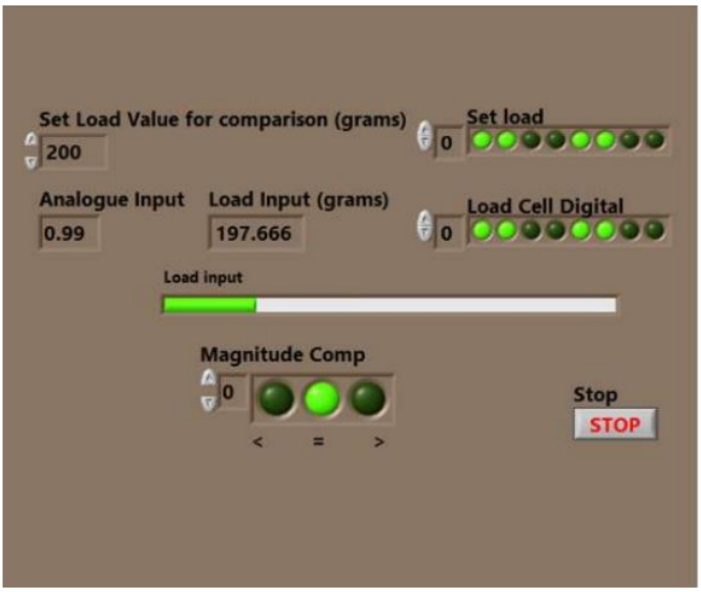
A good breakdown of the design implementation

3.4 Testing and Analysis

Testing the magnitude comparator with the added load cell value and automatic data logging is carried out at 3 different applied loads, showing the front screen indication and logged data in graph form in excel.

Firstly the set point was set to 200 grams and as shown below in figure 98. the potentiometer was then adjusted to change the load input to equal the set load value which as shown in figure 98 below the magnitude comparator equal to led indicator is lit and the set load and load cell digital indicators are corresponding.

With the exception of grammatical errors the explanations are good



Good test result

Figure 98 – 200 grams load input, front screen , equal to

The potentiometer is then adjusted to set the load input to be less than as shown in appendix 5.4 and adjusted to be greater than as also shown in appendix 5.4 . During this testing, all the data values are logged as shown in appendix 5.5. Using this data an excel graph was produced as shown below in figure 99.

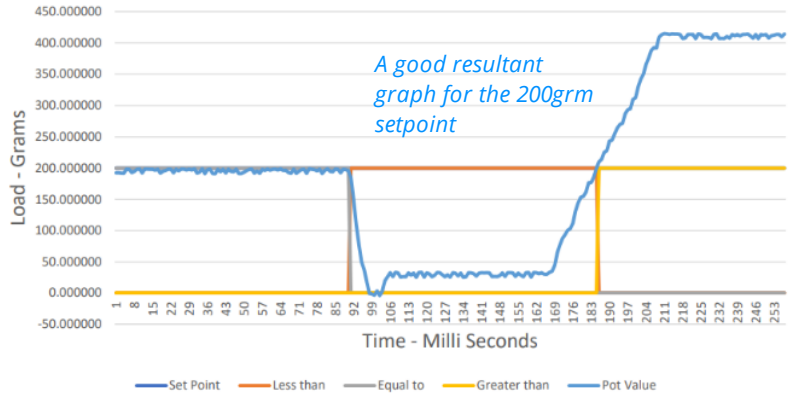
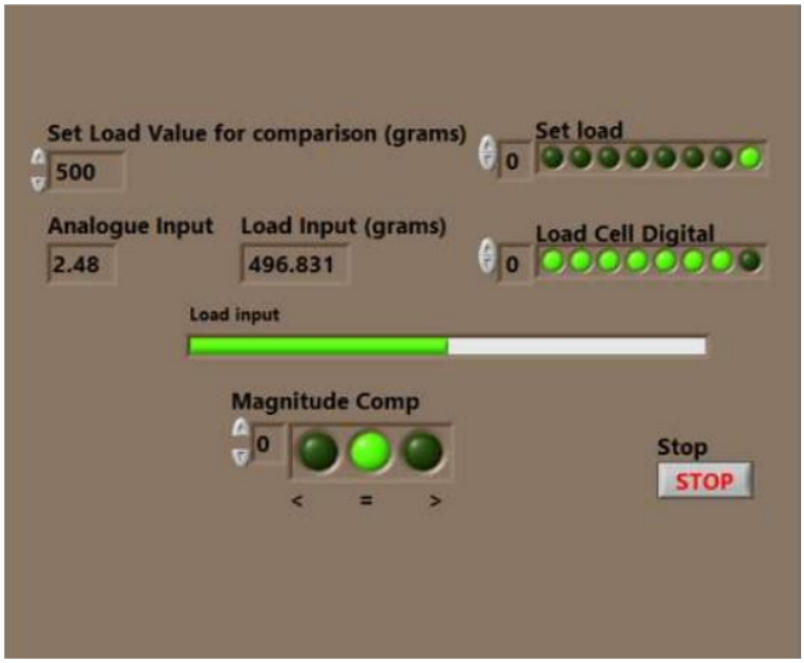


Figure 99 - 200 grams data log graph

As shown in figure 99 above, the graph shows the data over 253 mili seconds, It can be seen that the dark blue line is the 200 gram set point value and the potentiometer value is the light blue line. As the potentiometer is set to equal the gray line shows that the load input is equal to the setpoint, and as the potentiometer is set to less than the orange line rises to 200 grams. As the potentiometer is set to greater than 200 the light blue line rises and the less than (orange line) and the equal to (gray line) both go to zero and the Greater than line which is the yellow line rises to 200 grams. This proves that the magnitude comparator is working as it is designed to do.

Good explanation of graph

The set value was then increased to 500 grams and the potentiometer adjusted to change the load input to equal the set load value. As shown in figure 100 below the magnitude comparator equal to led indicator is lit and the set load and load cell digital indicators are corresponding.



Good test result despite the small error indicated

Figure 100 - 500 grams load input, front screen , equal to

The potentiometer is then adjusted to set the load input to be less than as shown in appendix 5.6 and adjusted to be greater than as also shown in appendix 5.6. During this testing, all the data values are logged as shown in appendix 5.7. Using this data an excel graph was produced as shown below in figure 101.

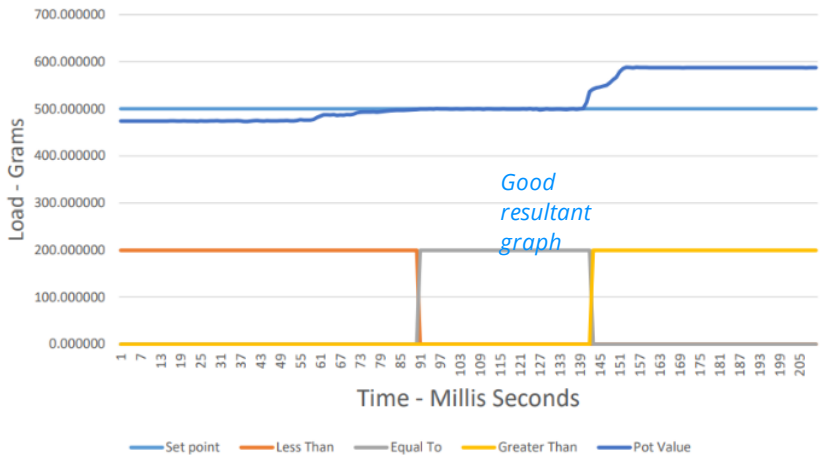
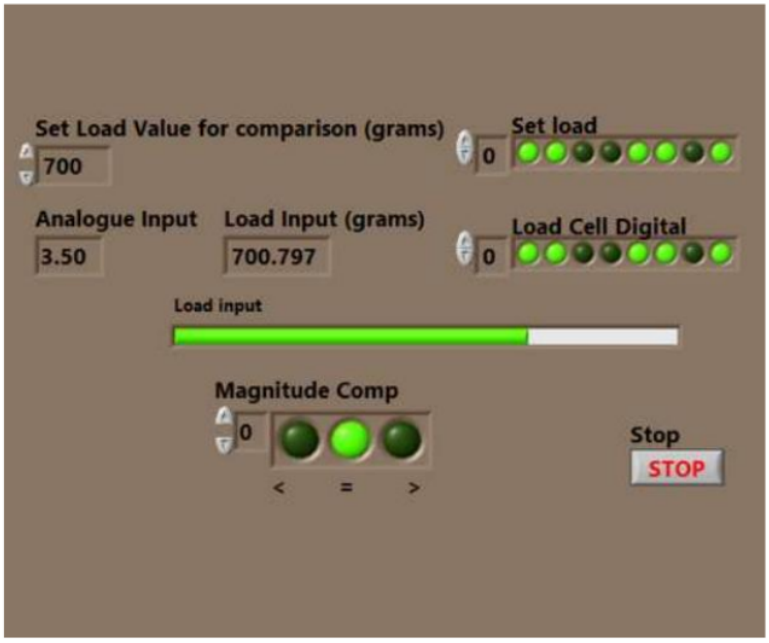


Figure 101 - 500 grams data log graph

In the graph above shown in figure 101 for the 500 grams set point, it can be seen by looking at the light blue line the set point value is 500 grams, The potentiometer is firstly set to less than the set point value which shows the orange line at 200 grams. When the potentiometer is set to equal to, the orange line which is less than goes to 0 grams and the grey equal to line rises to 200 grams. When the potentiometer is risen to over 500 grams it can be seen as the yellow greater to line rises from 0 to 200 grams. These tests prove that the magnitude comparator is working as it is designed to do.

The set value was then increased to 700 grams and the potentiometer adjusted to change the load input to equal the set load value. As shown in figure 102 below the magnitude comparator equal to led indicator is lit and the set load and load cell digital indicators are corresponding.



Good test result

Figure 102 - 700 grams load input, front screen, equal to

The potentiometer is then adjusted to set the load input to be less than as shown in appendix 5.8 and adjusted to be greater than as also shown in appendix 5.8. During this testing, all the data values are logged as shown in appendix 5.9. Using this data an excel graph was produced as shown below in figure 103.



Figure 103 - 700 grams data log graph

In the graph above shown in figure 103 for the 700 grams set point, it can be seen by looking at the light blue line the set point value is 700 grams, The potentiometer is firstly set to less than the set point value which shows the orange line at 200 grams. When the potentiometer is set to equal to, the orange line which is less than goes to 0 grams and the grey equal to line rises to 200 grams. When the potentiometer is risen to over 700 grams it can be seen as the yellow greater to line rises from 0 to 200 grams. These tests prove that the magnitude comparator is working as it is designed to do.

3.5 Conclusion and Recommendations

In Element 3 the magnitude comparator circuit in element 2 was re designed and further functions added to output the actual load cell value in grams. It was proven that the system worked as it should through 3 different load values by selecting a greater to than value, less than value and an equal to value for each. The data from each was successfully logged automatically and values obtained to produce a graph for each on excel, which proved also that the magnitude comparator design and implementation was successful as the correct comparator value was selected coinciding with the difference between load and set point value.

Although proven to be a success it could be recommended that to improve the resolution and accuracy of the system the number of bits could be increased from an 8 bit to a 16 bit. Allowing the set point value and load value to be a lot closer and accurate.

A reasonable evaluation

4.0 Citation List

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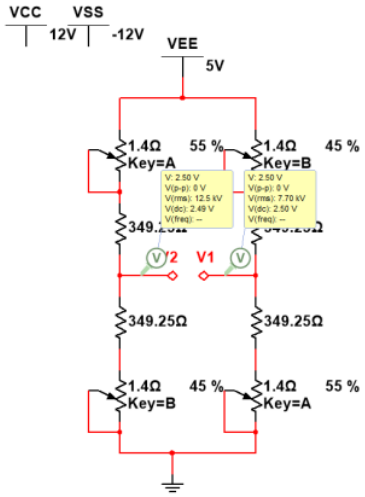
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A good number of releva

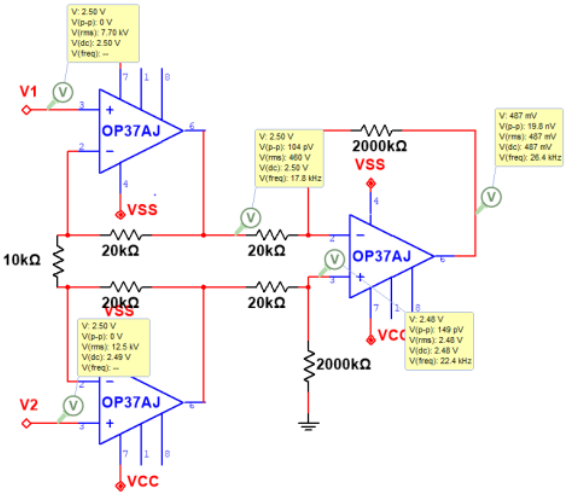
5.0 Appendix

5.1 Load cell and signal conditioning testing

Resistor values set to 55%, 45%, 55% and 45%

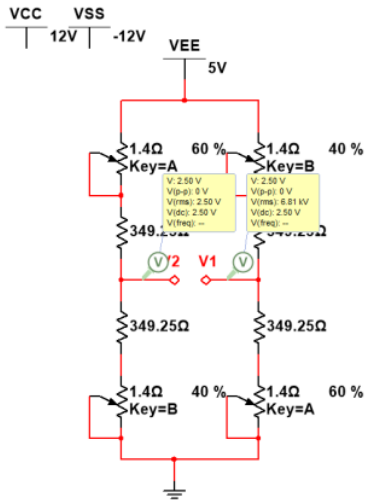


Load Cell LCKD - 1KG

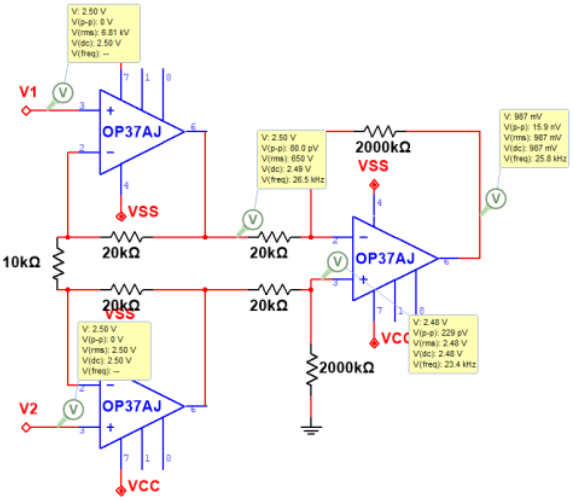


Instrumentation Amplifier

Resistor values set to 60%,40% 60% and 40%

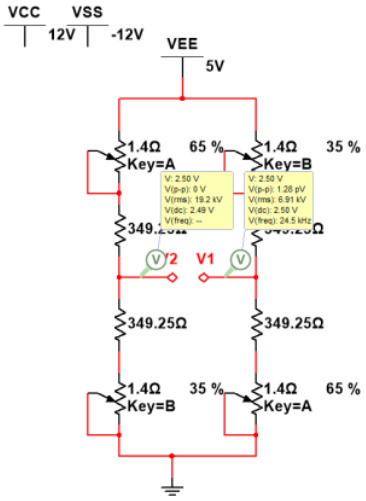


Load Cell LCKD - 1KG

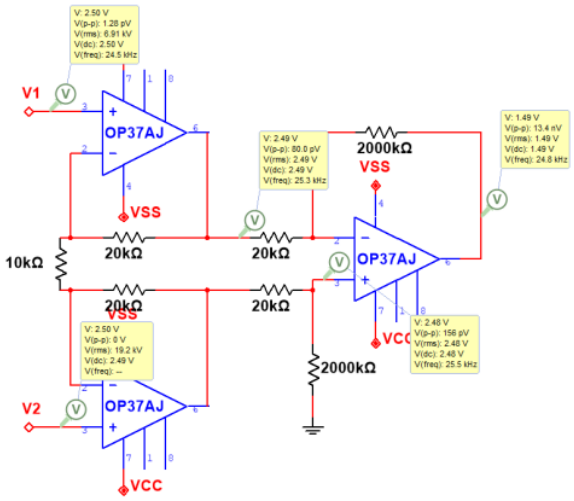


Instrumentation Amplifier

Resistor values set to 65%, 35%, 65% and 35%

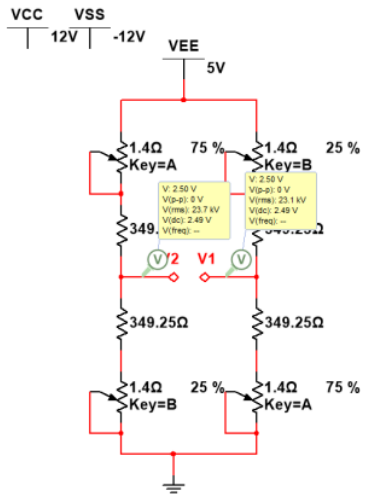


Load Cell LCKD - 1KG

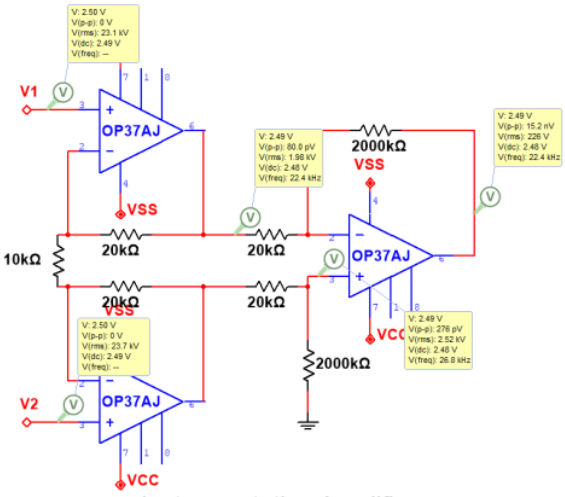


Instrumentation Amplifier

Resistor values set to 75%, 25% 75% and 25%

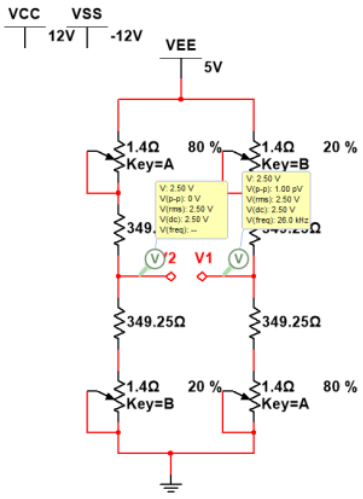


Load Cell LCKD - 1KG

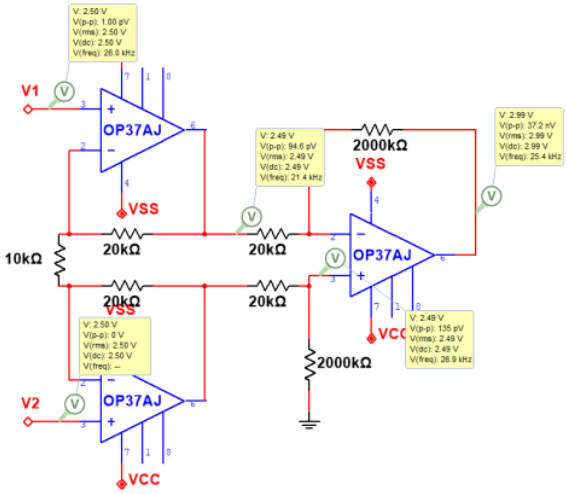


Instrumentation Amplifier

Resistor values set to 80%, 20% 80% and 20%

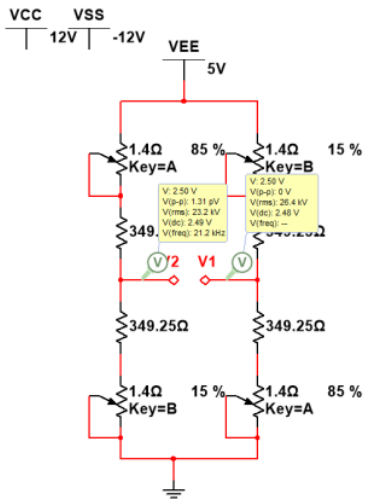


Load Cell LCKD - 1KG

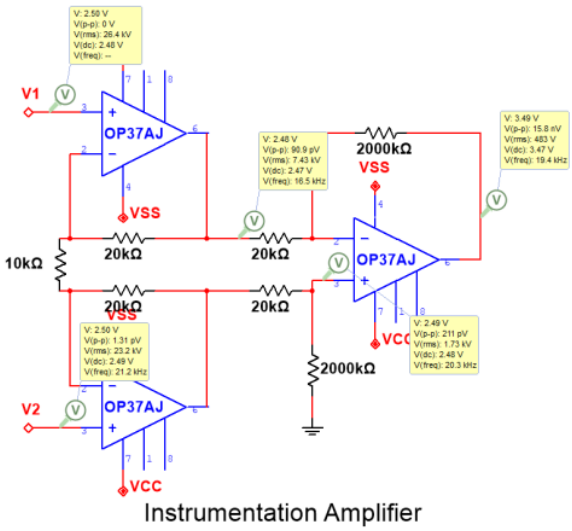


Instrumentation Amplifier

Resistor values set to 85%, 15% 85% and 15%

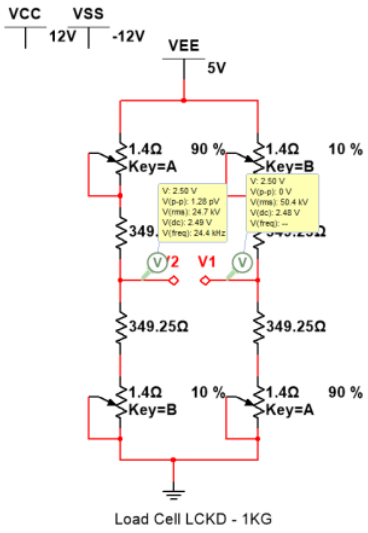


Load Cell LCKD - 1KG

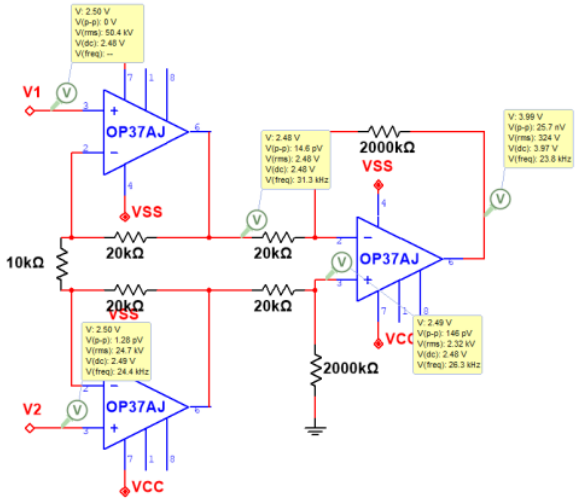


Instrumentation Amplifier

Resistor values set to 90%, 10% and 90% and 10%

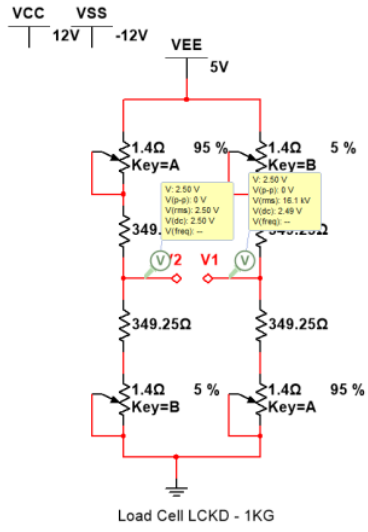


Load Cell LCKD - 1KG

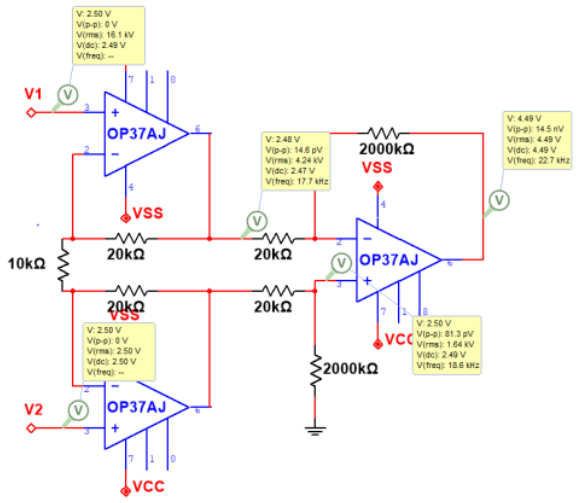


Instrumentation Amplifier

Resistor values set to 95%, 5% and 95% and 5%



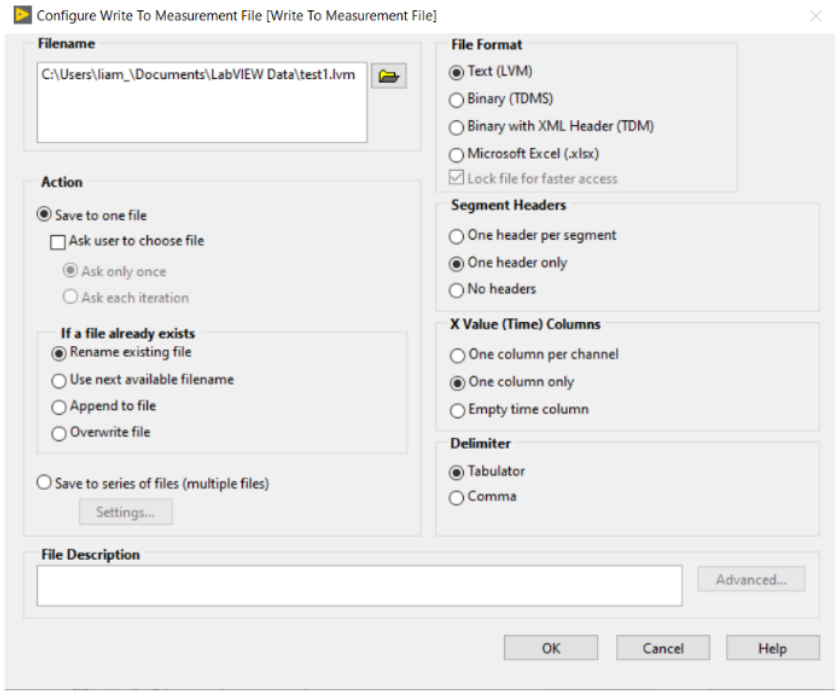
Load Cell LCKD - 1KG

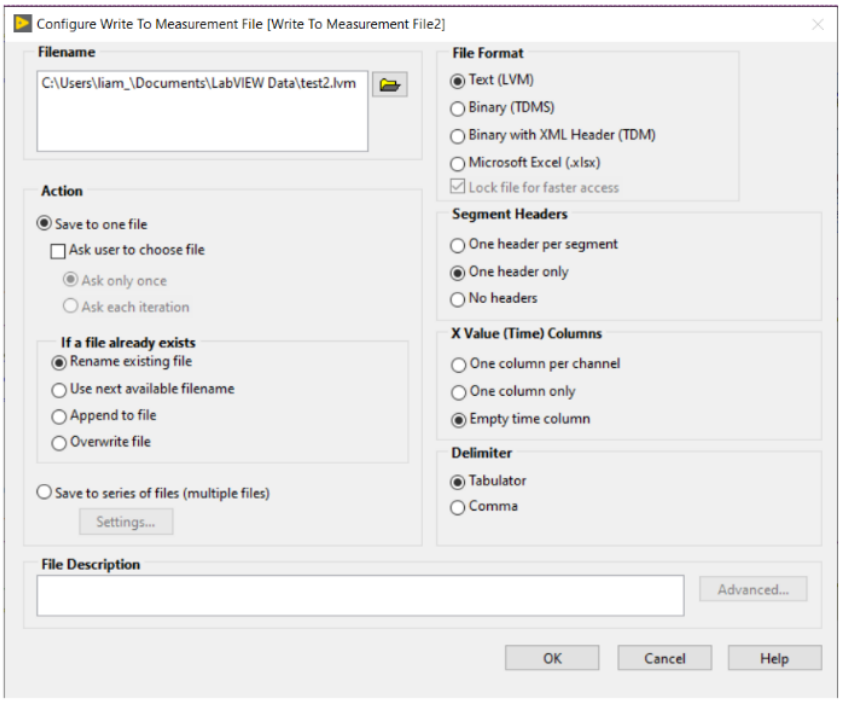


Instrumentation Amplifier

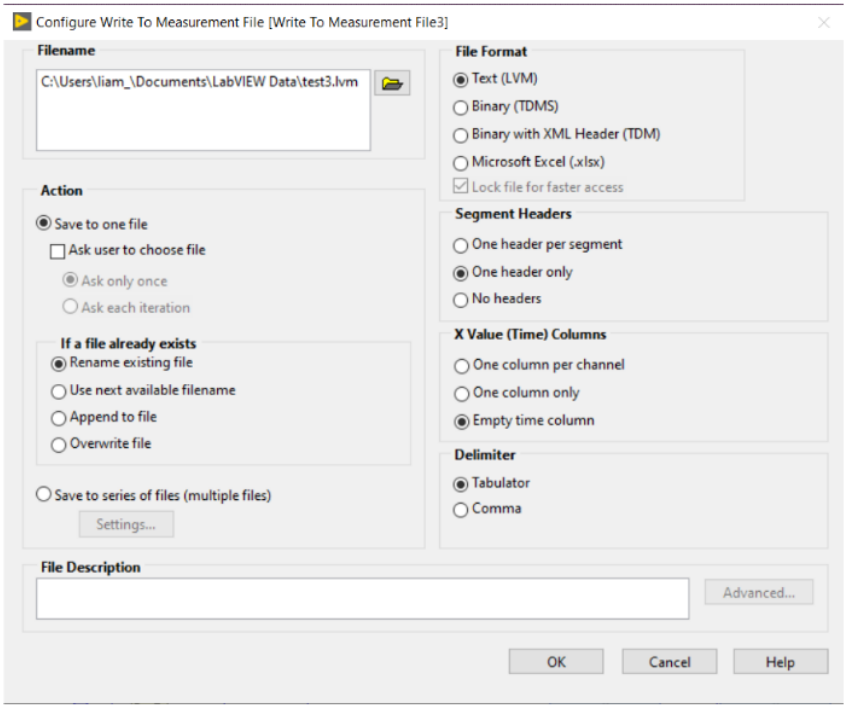
Full set of test results for instrument amplifier

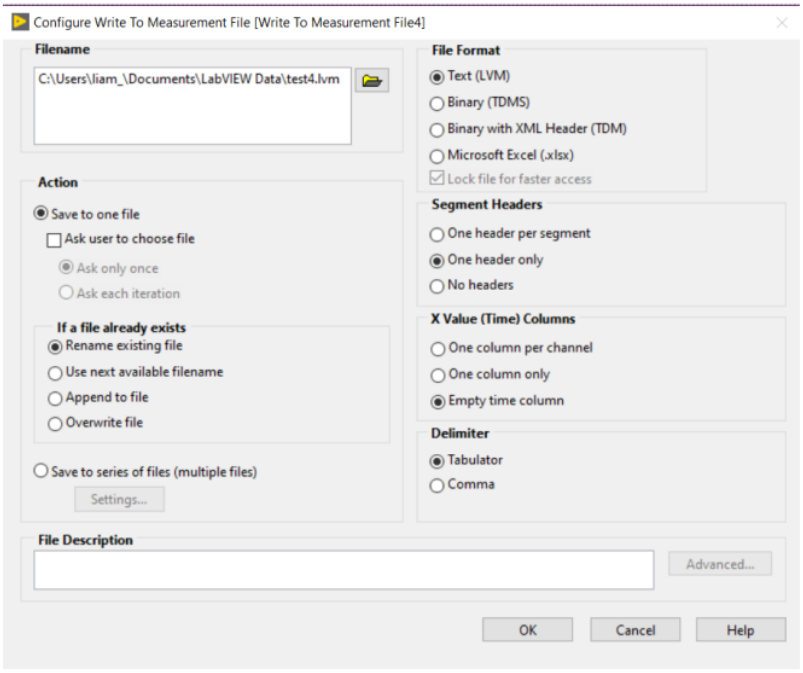
5.2 Element 3 write to file command window, file 1 and 2

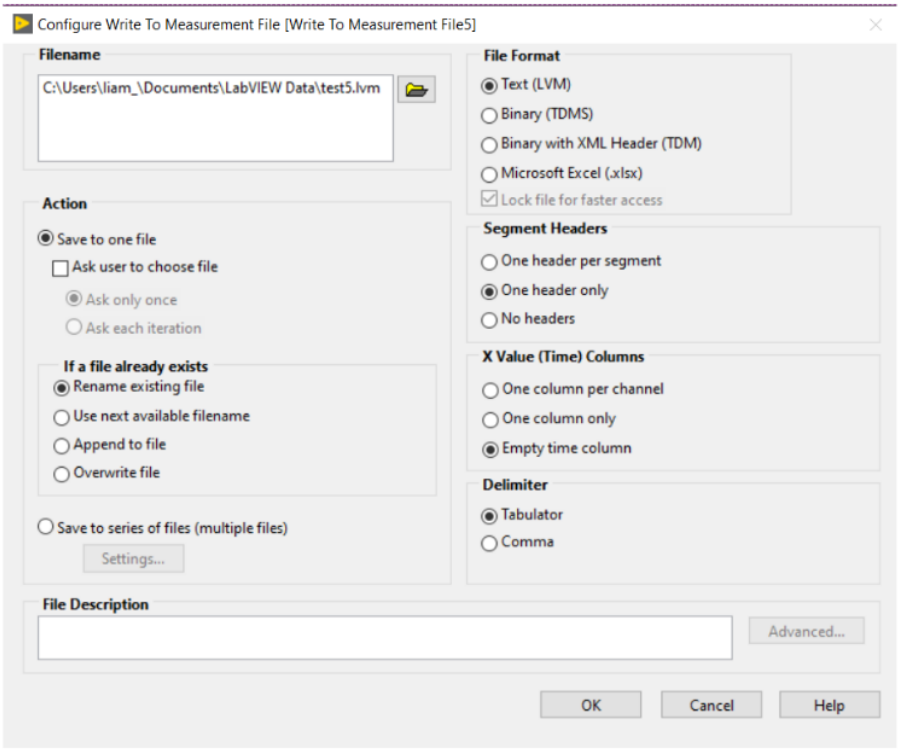




5.3 Element 3 write to file command window, file 3,4,5



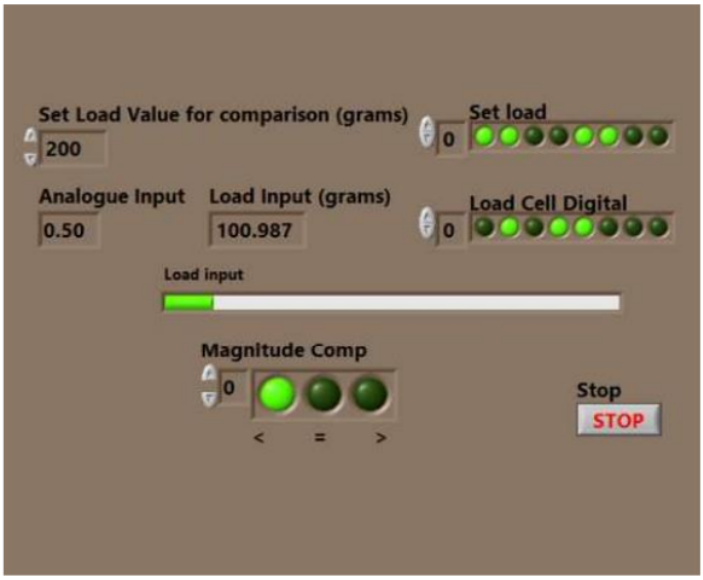




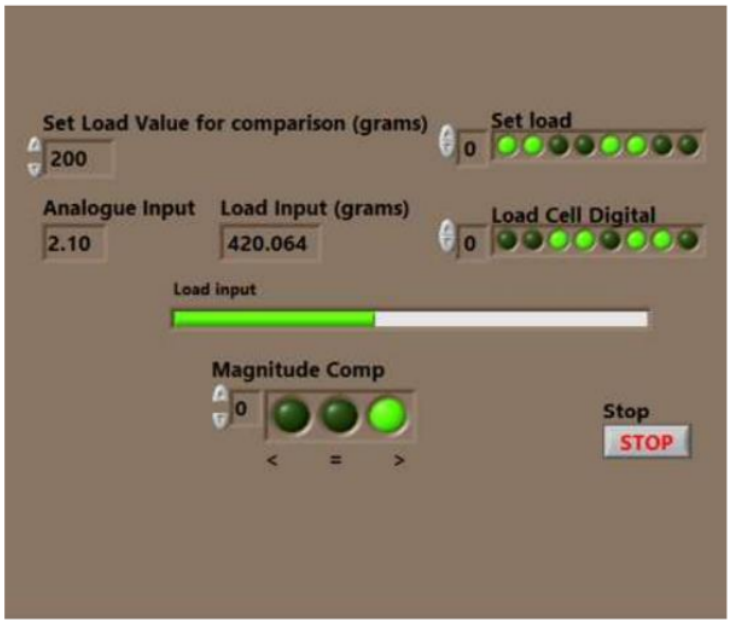
Full set of 'write file' configurations

5.4 200 grams front screen test

Less than :-



Greater than :-



These results complete the set for the tests for 200grm setpoint.

5.5 200 grams data values

Set Point	Less than	Equal to	Greater than	X Axis	Pot Value
200.000000	0.000000	200.000000	0.000000	0.000000	192.430951
200.000000	0.000000	200.000000	0.000000	0.097350	192.398832
200.000000	0.000000	200.000000	0.000000	0.197093	191.724320
200.000000	0.000000	200.000000	0.000000	0.297626	191.499483
200.000000	0.000000	200.000000	0.000000	0.397429	198.405196
200.000000	0.000000	200.000000	0.000000	0.497087	198.180359
200.000000	0.000000	200.000000	0.000000	0.597285	192.720028
200.000000	0.000000	200.000000	0.000000	0.698545	194.839921
200.000000	0.000000	200.000000	0.000000	0.798225	198.180359
200.000000	0.000000	200.000000	0.000000	0.898552	198.726392
200.000000	0.000000	200.000000	0.000000	0.998129	192.206114
200.000000	0.000000	200.000000	0.000000	1.099135	198.340957
200.000000	0.000000	200.000000	0.000000	1.199143	198.276718
200.000000	0.000000	200.000000	0.000000	1.301150	198.212479
200.000000	0.000000	200.000000	0.000000	1.401920	198.148239
200.000000	0.000000	200.000000	0.000000	1.500231	196.542259
200.000000	0.000000	200.000000	0.000000	1.600502	198.437316
200.000000	0.000000	200.000000	0.000000	1.700259	191.949157
200.000000	0.000000	200.000000	0.000000	1.801206	195.257475
200.000000	0.000000	200.000000	0.000000	1.901672	196.317422
200.000000	0.000000	200.000000	0.000000	2.001525	198.276718
200.000000	0.000000	200.000000	0.000000	2.102111	198.212479
200.000000	0.000000	200.000000	0.000000	2.201138	192.527310
200.000000	0.000000	200.000000	0.000000	2.301167	198.244598
200.000000	0.000000	200.000000	0.000000	2.401952	195.739269
200.000000	0.000000	200.000000	0.000000	2.501900	198.308837
200.000000	0.000000	200.000000	0.000000	2.600604	198.244598
200.000000	0.000000	200.000000	0.000000	2.703089	196.831336
200.000000	0.000000	200.000000	0.000000	2.803117	198.469435
200.000000	0.000000	200.000000	0.000000	2.904122	197.024053
200.000000	0.000000	200.000000	0.000000	3.005118	198.951229
200.000000	0.000000	200.000000	0.000000	3.102766	191.852799
200.000000	0.000000	200.000000	0.000000	3.202669	193.683615
200.000000	0.000000	200.000000	0.000000	3.302786	198.886990
200.000000	0.000000	200.000000	0.000000	3.402776	191.114048
200.000000	0.000000	200.000000	0.000000	3.503130	197.634326
200.000000	0.000000	200.000000	0.000000	3.603071	198.244598
200.000000	0.000000	200.000000	0.000000	3.703496	191.210407

200.000000	0.000000	200.000000	0.000000	3.803513	191.114048
200.000000	0.000000	200.000000	0.000000	3.903330	198.116120
200.000000	0.000000	200.000000	0.000000	4.004052	194.165409
200.000000	0.000000	200.000000	0.000000	4.104085	198.212479
200.000000	0.000000	200.000000	0.000000	4.205225	192.302473
200.000000	0.000000	200.000000	0.000000	4.303626	198.244598
200.000000	0.000000	200.000000	0.000000	4.403838	194.904160
200.000000	0.000000	200.000000	0.000000	4.504271	194.165409
200.000000	0.000000	200.000000	0.000000	4.604270	198.276718
200.000000	0.000000	200.000000	0.000000	4.704301	191.403124
200.000000	0.000000	200.000000	0.000000	4.805322	191.403124
200.000000	0.000000	200.000000	0.000000	4.907335	193.458778
200.000000	0.000000	200.000000	0.000000	5.006581	195.867748
200.000000	0.000000	200.000000	0.000000	5.106506	197.698565
200.000000	0.000000	200.000000	0.000000	5.206447	198.244598
200.000000	0.000000	200.000000	0.000000	5.306218	191.724320
200.000000	0.000000	200.000000	0.000000	5.406469	195.289595
200.000000	0.000000	200.000000	0.000000	5.508477	191.499483
200.000000	0.000000	200.000000	0.000000	5.607586	198.212479
200.000000	0.000000	200.000000	0.000000	5.707567	196.349542
200.000000	0.000000	200.000000	0.000000	5.806913	198.790631
200.000000	0.000000	200.000000	0.000000	5.907992	196.702857
200.000000	0.000000	200.000000	0.000000	6.007920	198.084000
200.000000	0.000000	200.000000	0.000000	6.107162	198.533675
200.000000	0.000000	200.000000	0.000000	6.209170	196.959814
200.000000	0.000000	200.000000	0.000000	6.309176	199.079708
200.000000	0.000000	200.000000	0.000000	6.407139	196.381661
200.000000	0.000000	200.000000	0.000000	6.508151	196.895575
200.000000	0.000000	200.000000	0.000000	6.609173	193.169702
200.000000	0.000000	200.000000	0.000000	6.708763	191.595842
200.000000	0.000000	200.000000	0.000000	6.809294	198.308837
200.000000	0.000000	200.000000	0.000000	6.911302	191.499483
200.000000	0.000000	200.000000	0.000000	7.011694	194.807801
200.000000	0.000000	200.000000	0.000000	7.111634	197.634326
200.000000	0.000000	200.000000	0.000000	7.211314	198.084000
200.000000	0.000000	200.000000	0.000000	7.311157	191.435244
200.000000	0.000000	200.000000	0.000000	7.411088	198.951229
200.000000	0.000000	200.000000	0.000000	7.511170	198.212479
200.000000	0.000000	200.000000	0.000000	7.613163	197.537967
200.000000	0.000000	200.000000	0.000000	7.712132	195.578671
200.000000	0.000000	200.000000	0.000000	7.812496	198.244598

200.000000	0.000000	200.000000	0.000000	7.912792	191.210407
200.000000	0.000000	200.000000	0.000000	8.014096	196.670738
200.000000	0.000000	200.000000	0.000000	8.114496	198.983349
200.000000	0.000000	200.000000	0.000000	8.216503	194.743562
200.000000	0.000000	200.000000	0.000000	8.316058	194.326007
200.000000	0.000000	200.000000	0.000000	8.415054	198.694273
200.000000	0.000000	200.000000	0.000000	8.515084	198.019761
200.000000	0.000000	200.000000	0.000000	8.615530	192.527310
200.000000	0.000000	200.000000	0.000000	8.715313	198.051881
200.000000	0.000000	200.000000	0.000000	8.815045	197.409489
200.000000	0.000000	200.000000	0.000000	8.916033	196.124705
200.000000	200.000000	0.000000	0.000000	9.016215	185.107686
200.000000	200.000000	0.000000	0.000000	9.115108	150.450689
200.000000	200.000000	0.000000	0.000000	9.214462	108.438389
200.000000	200.000000	0.000000	0.000000	9.317133	77.828556
200.000000	200.000000	0.000000	0.000000	9.415518	50.655533
200.000000	200.000000	0.000000	0.000000	9.515092	37.775657
200.000000	200.000000	0.000000	0.000000	9.616117	19.178539
200.000000	200.000000	0.000000	0.000000	9.715106	-0.960298
200.000000	200.000000	0.000000	0.000000	9.817119	-1.570566
200.000000	200.000000	0.000000	0.000000	9.918141	-3.754681
200.000000	200.000000	0.000000	0.000000	10.018146	3.150979
200.000000	200.000000	0.000000	0.000000	10.119118	-4.364949
200.000000	200.000000	0.000000	0.000000	10.218625	2.540711
200.000000	200.000000	0.000000	0.000000	10.318630	19.820926
200.000000	200.000000	0.000000	0.000000	10.419255	26.437516
200.000000	200.000000	0.000000	0.000000	10.519755	32.700794
200.000000	200.000000	0.000000	0.000000	10.619708	26.501755
200.000000	200.000000	0.000000	0.000000	10.719654	33.535898
200.000000	200.000000	0.000000	0.000000	10.819077	32.604436
200.000000	200.000000	0.000000	0.000000	10.920391	25.730890
200.000000	200.000000	0.000000	0.000000	11.020385	26.630232
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200.000000	200.000000	0.000000	0.000000	11.220667	32.540198
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200.000000	200.000000	0.000000	0.000000	11.723169	33.503779
200.000000	200.000000	0.000000	0.000000	11.822512	25.730890
200.000000	200.000000	0.000000	0.000000	11.922485	32.379601

200.000000	200.000000	0.000000	0.000000	12.024469	31.126945
200.000000	200.000000	0.000000	0.000000	12.122249	26.244800
200.000000	200.000000	0.000000	0.000000	12.223512	28.717992
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200.000000	200.000000	0.000000	0.000000	12.822850	25.730890
200.000000	200.000000	0.000000	0.000000	12.926033	32.700794
200.000000	200.000000	0.000000	0.000000	13.023429	32.026287
200.000000	200.000000	0.000000	0.000000	13.124415	27.625933
200.000000	200.000000	0.000000	0.000000	13.224442	32.154765
200.000000	200.000000	0.000000	0.000000	13.326449	25.506054
200.000000	200.000000	0.000000	0.000000	13.428437	26.084203
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200.000000	200.000000	0.000000	0.000000	14.132918	32.540198
200.000000	200.000000	0.000000	0.000000	14.233478	32.732914
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200.000000	200.000000	0.000000	0.000000	14.734059	28.428917
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200.000000	200.000000	0.000000	0.000000	15.134138	32.732914
200.000000	200.000000	0.000000	0.000000	15.234126	32.604436
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200.000000	200.000000	0.000000	0.000000	15.434286	32.283243
200.000000	200.000000	0.000000	0.000000	15.534545	28.814350
200.000000	200.000000	0.000000	0.000000	15.634486	26.180561
200.000000	200.000000	0.000000	0.000000	15.734686	32.668675
200.000000	200.000000	0.000000	0.000000	15.835149	33.118346
200.000000	200.000000	0.000000	0.000000	15.935174	25.666651
200.000000	200.000000	0.000000	0.000000	16.034500	33.086227

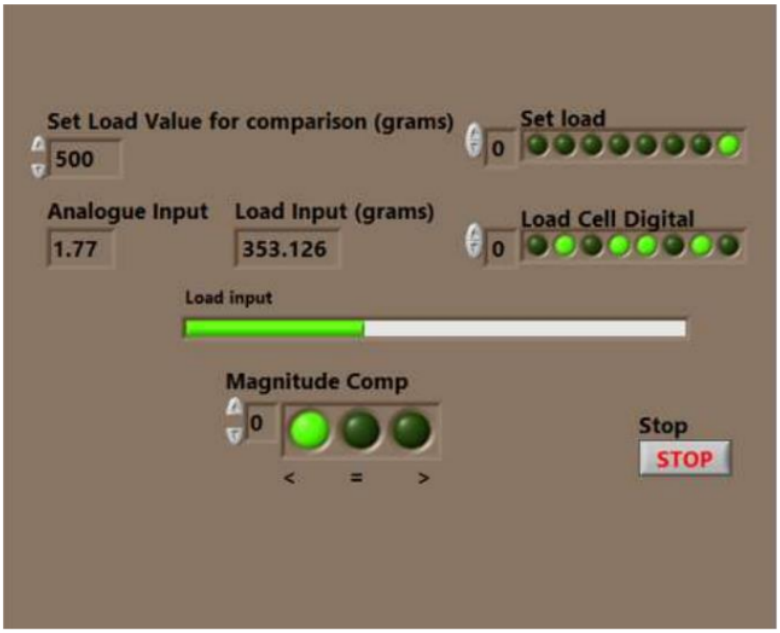
200.000000	200.000000	0.000000	0.000000	16.134486	32.893511
200.000000	200.000000	0.000000	0.000000	16.234393	31.159064
200.000000	200.000000	0.000000	0.000000	16.334589	32.765033
200.000000	200.000000	0.000000	0.000000	16.434515	30.484557
200.000000	200.000000	0.000000	0.000000	16.535306	30.227602
200.000000	200.000000	0.000000	0.000000	16.636318	33.375301
200.000000	200.000000	0.000000	0.000000	16.736340	35.173987
200.000000	200.000000	0.000000	0.000000	16.835345	44.392251
200.000000	200.000000	0.000000	0.000000	16.936352	64.466877
200.000000	200.000000	0.000000	0.000000	17.036934	77.378884
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200.000000	200.000000	0.000000	0.000000	17.838106	153.277207
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200.000000	200.000000	0.000000	0.000000	18.040409	161.917362
200.000000	200.000000	0.000000	0.000000	18.139260	176.756597
200.000000	200.000000	0.000000	0.000000	18.239008	177.013553
200.000000	200.000000	0.000000	0.000000	18.339146	185.782197
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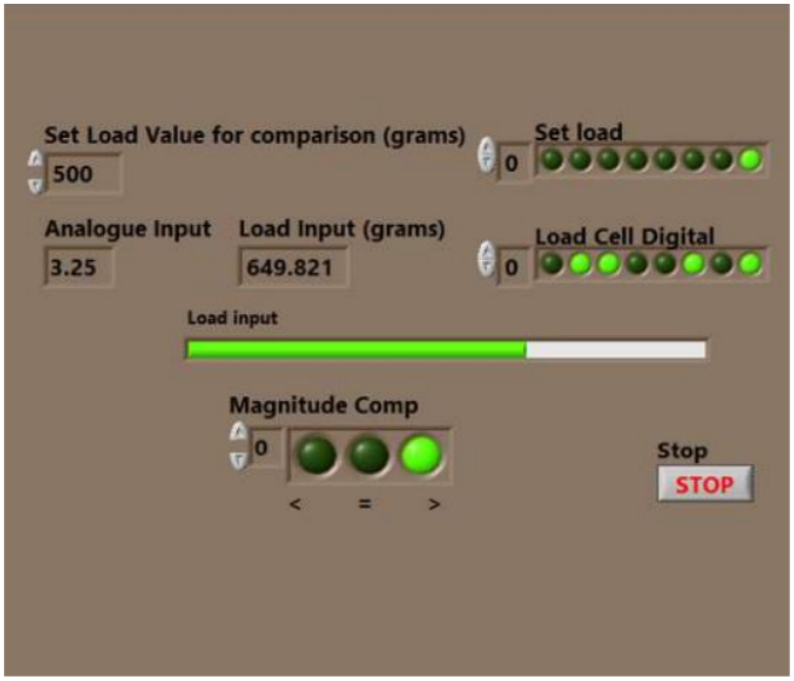
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5.6 200grams front screen test

Less than :-



Greater than :-



5.7 200 grams data values

Set point	Less Than	Equal To	Greater Than	X Axis	Pot Value
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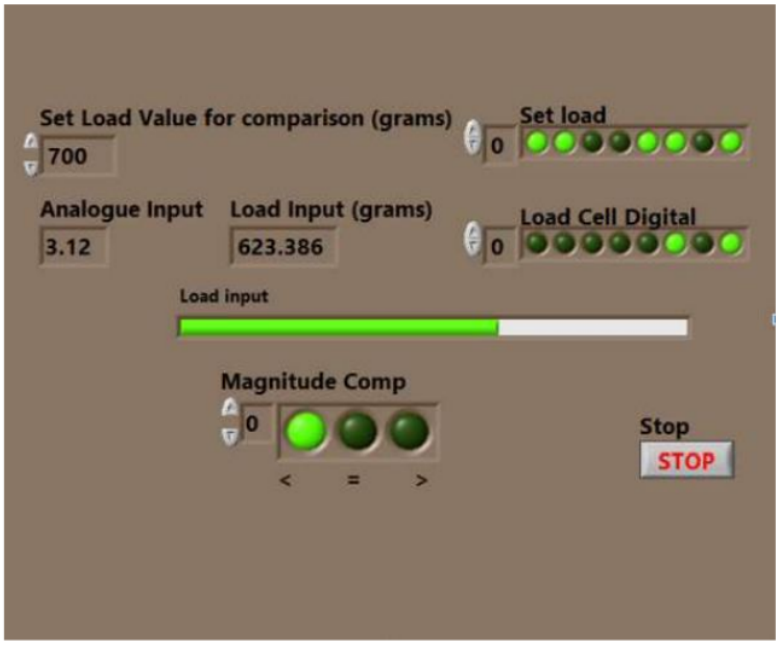
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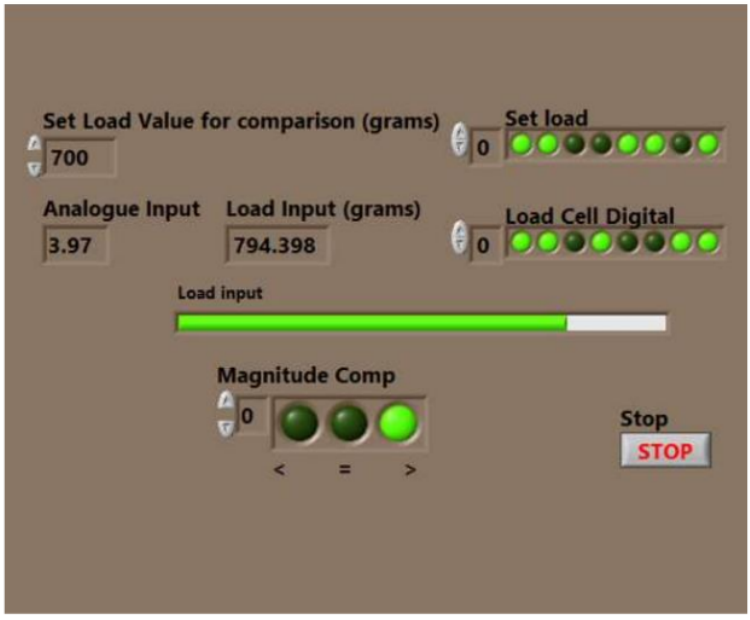
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500.000000	0.000000	0.000000	200.000000	20.447399	587.250375
500.000000	0.000000	0.000000	200.000000	20.546661	587.314616
500.000000	0.000000	0.000000	200.000000	20.646942	587.443098
500.000000	0.000000	0.000000	200.000000	20.748205	587.186134
500.000000	0.000000	0.000000	200.000000	20.848464	587.282495
500.000000	0.000000	0.000000	200.000000	20.947728	587.218254
500.000000	0.000000	0.000000	200.000000	21.046992	587.314616

5.8 700 grams front screen test

Less than :-



Greater than :-



5.9 700 grams data values

Set Point	Less than	Equal to	Greater than	X Axis	Pot Value
700.000000	200.000000	0.000000	0.000000	0.203626	587.282495
700.000000	200.000000	0.000000	0.000000	0.301827	587.218254
700.000000	200.000000	0.000000	0.000000	0.403073	587.250375
700.000000	200.000000	0.000000	0.000000	0.504344	587.282495
700.000000	200.000000	0.000000	0.000000	0.602605	587.250375
700.000000	200.000000	0.000000	0.000000	0.703874	587.250375
700.000000	200.000000	0.000000	0.000000	0.803137	587.346737
700.000000	200.000000	0.000000	0.000000	0.906412	587.186134
700.000000	200.000000	0.000000	0.000000	1.005684	587.314616
700.000000	200.000000	0.000000	0.000000	1.104972	587.378857
700.000000	200.000000	0.000000	0.000000	1.206211	587.346737
700.000000	200.000000	0.000000	0.000000	1.307481	587.282495
700.000000	200.000000	0.000000	0.000000	1.405741	587.282495
700.000000	200.000000	0.000000	0.000000	1.506009	587.410978
700.000000	200.000000	0.000000	0.000000	1.606275	587.057651
700.000000	200.000000	0.000000	0.000000	1.706542	587.218254
700.000000	200.000000	0.000000	0.000000	1.807814	587.410978
700.000000	200.000000	0.000000	0.000000	1.907073	587.667942
700.000000	200.000000	0.000000	0.000000	2.009348	587.764304
700.000000	200.000000	0.000000	0.000000	2.107628	587.314616
700.000000	200.000000	0.000000	0.000000	2.207875	587.635822
700.000000	200.000000	0.000000	0.000000	2.307141	587.667942
700.000000	200.000000	0.000000	0.000000	2.407405	587.314616
700.000000	200.000000	0.000000	0.000000	2.507674	587.218254
700.000000	200.000000	0.000000	0.000000	2.606936	587.571581
700.000000	200.000000	0.000000	0.000000	2.708206	587.250375
700.000000	200.000000	0.000000	0.000000	2.807469	587.378857
700.000000	200.000000	0.000000	0.000000	2.907737	587.507339
700.000000	200.000000	0.000000	0.000000	3.007000	586.993410
700.000000	200.000000	0.000000	0.000000	3.108270	587.828545
700.000000	200.000000	0.000000	0.000000	3.209551	587.507339
700.000000	200.000000	0.000000	0.000000	3.307801	586.897048
700.000000	200.000000	0.000000	0.000000	3.408094	587.218254
700.000000	200.000000	0.000000	0.000000	3.509509	587.250375
700.000000	200.000000	0.000000	0.000000	3.608601	587.186134
700.000000	200.000000	0.000000	0.000000	3.708869	587.218254
700.000000	200.000000	0.000000	0.000000	3.810141	586.897048
700.000000	200.000000	0.000000	0.000000	3.910406	587.282495

700.000000	200.000000	0.000000	0.000000	4.009669	587.346737
700.000000	200.000000	0.000000	0.000000	4.110938	586.961290
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700.000000	200.000000	0.000000	0.000000	4.312474	586.672204
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700.000000	200.000000	0.000000	0.000000	5.214874	587.218254
700.000000	200.000000	0.000000	0.000000	5.317147	587.571581
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Raw data example from text files

1809812

GRADEMARK REPORT

FINAL GRADE

68/100

GENERAL COMMENTS

Instructor

PAGE 1

PAGE 2

PAGE 3

Text Comment. A good level of detail in the table of contents

PAGE 4

PAGE 5

PAGE 6

Text Comment. Good list of figures

PAGE 7

Text Comment. Avoid the first person terms

Text Comment. The 4 bit adder and 4 bit comparator are the initial designs

PAGE 8

Text Comment. The program environment is Vivado from Xilinx

Text Comment. Good example and correct statement that it does make possible the interface with LabVIEW.

Text Comment. Good example of IP design

PAGE 9

PAGE 10

PAGE 11

Text Comment. Explanation covers the main relevant DAQ components needed for the system

PAGE 12

PAGE 13

Text Comment. Comparators are covered in good detail.

PAGE 14

PAGE 15

Text Comment. Good work here. You have identified the relationship with resolution and sample rate which is determined by the conversion process.

PAGE 16

Text Comment. Good explanation of the transducer load cell which is relevant to the task

PAGE 17

Text Comment. The stages of signal conditioning have been identified here and backed up with a good explanation and images.

PAGE 18

Text Comment. Hierarchy and inheritance have been identified

PAGE 19

PAGE 20

Text Comment. 4 bit adder design is explained with good images

PAGE 21

PAGE 22

Text Comment. Code is neat and tidy with a good explanation

PAGE 23

Text Comment. Source hierarchy is explained in good detail

Text Comment. Code is neat and tidy with no errors

PAGE 24

Text Comment. IP design is good and backed up with an explanation

PAGE 25

Text Comment. Good design using PLD

PAGE 26

Text Comment. 8 bit magnitude comparator using cascading IC's in PLD design mode is correct and ready for implementation with FPGA.

PAGE 27

Text Comment. Good set of test data

Text Comment. Very good test results using the virtual bus method. The carry out bit is set to logic 1 for the overflow bit.

PAGE 28

Text Comment. No test has been carried out for the 4 bit comparator using Vivado

PAGE 29

Text Comment. This needs a heading to explain what is being tested and its purpose. This is the 4 bit adder and 4 bit comparator test using FPGA.

Text Comment. Good test result

Text Comment. Good use of table. The set value is compared against the sum of A+B. The A=B term is misleading.

PAGE 30

Text Comment. Good test result

PAGE 31

Text Comment. Good test result

PAGE 32

Text Comment. Good test results showing all 3 states

Text Comment. Test data is very good

PAGE 33

PAGE 34

Text Comment. These tests are repeats of the above tests.

PAGE 35

Text Comment. The table is good and shows the test data with results.

PAGE 36

PAGE 37

PAGE 38

Text Comment. Good set of test results of 8 bit comparator which enables the PLD design to continue

Text Comment. Good use of table

PAGE 39

Text Comment. PLD design is good

PAGE 40

Text Comment. Good test result

PAGE 41

Text Comment. Good test result

PAGE 42

Text Comment. Good test result

Text Comment. Good use of table to evaluate the overall test results

PAGE 43

Text Comment. Incorrect use of capital letters

Text Comment. Despite some grammatical errors the evaluation covers the element task outcomes

PAGE 44

PAGE 45

Text Comment. This should be LabVIEW

Text Comment. Good informative introduction

PAGE 46

Text Comment. Only the last stage is the unity gain here which is only due to the resistor values. The voltages prove the operation in this mode.

Text Comment. Unity gain is identified here

PAGE 47

Text Comment. Gain needed is identified by buffer gain and the diff amp gain

Text Comment. Good reference to test and analysis further in report

PAGE 48

Text Comment. G-code is correct with correct formula

Text Comment. Test is good for 10 bit resolution

PAGE 49

Text Comment. G-code and formula are correct

PAGE 50

Text Comment. G-code is correct with all data i/o configured

PAGE 51

PAGE 52

Text Comment. G-code program looks correct with all the function blocks for the DAQ implemented

Text Comment. This is how the 16 bits get input to the FPGA single channel

Text Comment. Formula block functions are identified

Text Comment. Good explanation for return data result

PAGE 53

Text Comment. Good design

Text Comment. FPGA ports are identified

PAGE 54

PAGE 55

Text Comment. Good test results and table of resultant values. Good reference to further test results in appendix

PAGE 56

Text Comment. Good resultant linear graph

PAGE 57

Text Comment. Good set of results for 10 bit ADC with max value stable

PAGE 58

Text Comment. Good set of results for 12 bit ADC with max value stable

PAGE 59

PAGE 60

Text Comment. Good set of results for the 8 bit comparator with virtual input

PAGE 61

Text Comment. Good image of equipment setup

PAGE 62

PAGE 63

PAGE 64

Text Comment. A good set of results which indicate the correct operation of the system

PAGE 65

Text Comment. comparator is on the FPGA. LabVIEW handles data transfer

Text Comment. With the exception of a minor error / confusion issue the evaluation is good

PAGE 66

PAGE 67

Text Comment. Good introduction

PAGE 68

Text Comment. The G-code is neatly designed and has no errors.

Text Comment. Write files are identified and explained

Text Comment. Good design of front panel

PAGE 69

Text Comment. A good breakdown of the design implementation

PAGE 70

Text Comment. With the exception of grammatical errors the explanations are good

Text Comment. Good test result

PAGE 71

Text Comment. A good resultant graph for the 200grm setpoint

Text Comment. Good explanation of graph

PAGE 72

Text Comment. Good test result despite the small error indicated

PAGE 73

Text Comment. Good resultant graph

PAGE 74

Text Comment. Good test result

PAGE 75

Text Comment. Good resultant graph

PAGE 76

Text Comment. A reasonable evaluation

PAGE 77

PAGE 78

Text Comment. A good number of relevant sources

PAGE 79

PAGE 80

PAGE 81

PAGE 82

PAGE 83

Text Comment. Full set of test results for instrument amplifier

PAGE 84

PAGE 85

PAGE 86

Text Comment. Full set of 'write file' configurations

PAGE 87

Text Comment. These results complete the set for the tests for 200grm setpoint.

PAGE 88

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PAGE 109

Text Comment. Raw data example from text files

GRADING FORM: CSG-RUBIC

LIAM GEORGE	**0**

RESEARCH-INFORMED LITERATURE

Research section has covered all requirements with a minor error. Good relevant sources used. **6/10**

KNOWLEDGE AND UNDERSTANDING

E1-Design and use of magnitude comparator with digital inputs has been created with good explanations. There are some minor confusions in the explanations . Test methods followed a logical sequence. 7/10 E2- The LabVIEW design for the analogue load cell input is explained and the design is a good. The 16 bit word operation for the FPGA is partly explained. The shift and add parts are missing and this is the key to how the data bits are organised for the FPGA. The design is operational but needs to be explained. 6.5/10 E3- Dat logging has ben fully explained and a good knowledge of this section is demonstrated. 7.5/10 **21/30**

ANALYSIS

E1-Test and results are very comprehensive . The evaluation has minor errors / confusions. The main sections are covered. 3/5 E2-The results from LabVIEW are comprehensive and detailed. There are some minor confused points made in the evaluation. 6.5/10 E3-Results from the data logging section are detailed and a reasonable evaluation for this section. 7.5/10

17/25

PRACTICAL APPLICATION AND DEP.

E1-Prototypes for the comparator have been designed using logical methods. PLD design methods used were successfully implemented using the FPGA board. 3/5 E2-Design and build of LabVIEW interface for FPGA followed a good development sequence. The development sections were tested at designated stages to prove design. The data was shifted right and added successfully. 3.5/5 E3-Data logging using LabVIEW methods has ben designed and tested for operational requirements. 7.5/10

14/20

SKILLS FOR PROFESSIONAL PRAC.

Report is in a good logical sequence and presented well. There are grammatical errors.

10/15