

UWTSD Timetable 2017/2018



Programme timetable - BENG_CSESH_L6 (3), BENG Computer Systems & Electronics L6 (3) (Wk 23, wk starting 29/01/2018)

	09:00AM	10:00AM	11:00AM	12:00PM	01:00PM	02:00PM	03:00PM	04:00PM
Mo 29/01/2018								
Tue 30/01/2018								
We 31/01/2018	PLCs & Control Gary Jones MH506 (SW)							
Thu 01/02/2018	Digital Systems Synthesis Gary Jones MH506 (SW)					Embedded Microcontrollers Gareth Jones MH503 (SW); ZFACESA1_LS90 (LRA/MBL09/MH503/MT107/LRB)		
Fri 02/02/2018								