

PSDE 4004 - Assignment 2

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by Callum Williams

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PSDE4004

ASSIGNMENT 2 – DIGITAL

CIRCUIT DESIGN

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Introduction, aims and objectives.

The first task of this electronic report is to acquire vital information about both combinational and sequential logic so an important analysis between the two can be made.

After completion of the analysis the next task is to research the use of a Finite State Machine and why it is used as a design tool for electronic systems, once completed the final task in the research section is to compare FPGA's and ASIC's and the difference between the two highlighting the positive and negatives of both programmable circuits. To make it clear there are 3 objectives in mind for this specific task –

- Differences between combinational and sequential logic
- Explanation on the use of Finite State Machine as a design tool
- Compare FPGA's and ASIC's

When carrying out tasks there should be referencing from the websites and books information is acquired from preventing from any copyright issues.

Once the research section is completed the next step is to design the circuit this circuit should have the ability to count from 0 – 59 and display it on the seven segment that is on the nexys test board which contains a FPGA (Field-programmable gate array) the FPGA should also have a stop/reset functions programmed on to it, these features should be added during the designing stage. Once the program is installed on to the nexys board it will also be used for the practical testing during the assignment.

Before any practical testing various circuits are going to be made on multisim where they will be tested until they give the required results to meet the specification. These will be tested in PLD mode and after finally finishing the testing and assembly stages on multisim the circuits will be combined and uploaded on to the Digilent Nexys 4 test board.

Once the designing and uploading onto the nexys board is complete the final step is to test the circuit, if this works correctly the device should count up to 59. With the results acquired a conclusion will be written with recommendations on what could be improved with the assignments specification and what could be added to improve the design.

Research

A) COMBINATIONAL LOGIC & SEQUENTIAL LOGIC RESEARCH

COMBINATIONAL LOGIC

Electronis Course Quotes "A combinational logic circuit implement logical functions where its outputs depend only on its current combination of input values." (2017)

A combinational logic circuits output is constantly relying on its input, if at any time the input is changed this will affect the output.

A combinational circuit is made of multiple logic gates these gates are called NAND, NOT and NOR, all of these gates have a different output depending on their input , here are some truth tables to show the outputs variation depending on the inputs.

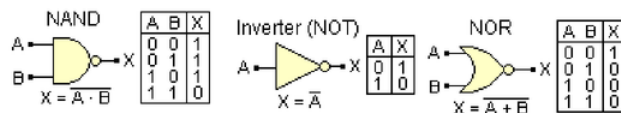
A & B – Inputs

X –

Outputs

1 = ON

0 = OFF

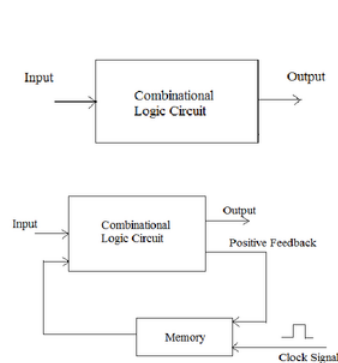


A combinational circuit is made out of different combinations of these gates to achieve a more complex circuit (hence the name combinational) that have more inputs and outputs.

Combinational circuits are often used in multiplexers and demultiplexers.

SEQUENTIAL LOGIC RESEARCH

A Sequential logic circuit's output does not only vary on its current input but also from the status of its previous inputs this makes it different from combinational logic circuits that primarily depend on their current input to determine their output state.



Here are some pictures I found Online the top circuit diagram is of a combinational logic circuit.

The second picture is that of a sequential logic circuit.

As you can see they share similar designs, the only difference is that the sequential logic circuit also has a memory feature that feeds directly back to the input side of the circuit linked in with clock pulses. Sequential logic circuits are used in Random Access Memory (RAM) because of their ability to remember previous inputs.

This type of Logic is used in Finite Machines.

B) FINITE MACHINES

Hanson Quotes "The circuit's function is broken down into a collection of states and rules which determine when the system moves from one state to another state. This concept can be committed to paper by drawing what is called a state diagram" (2015)

A finite machine is a system in which makes transitions from state to state based on the conditions of their inputs, these can also be displayed on truth tables the same way as logic gates.

When a finite machine is in a certain state its current state and the variation of the input are both used to determine the next state of a finite machine, this then happens again and circles back to its previous state one way or another (very similar to a traffic light process)

In digital circuits, logic gates are used to make finite machine circuits they are very similar to sequential logic circuits and also have memory and can remember their previous input.

A good example of a finite machine in circuits would be traffic lights

imagine all colours of the traffic light were states and the button on the traffic light was in input when the button is not pressed nothing will happen and traffic will continue as normal but when the button is pressed it sends a signal to the circuit and uses the current state of the traffic light and the input signal to determine what light to display next.

C) FPGA and ASICS

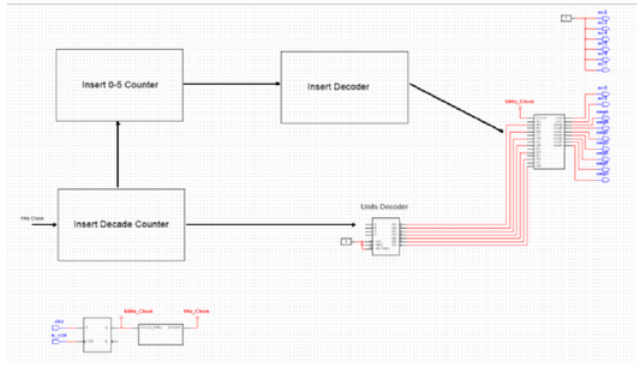
Atlanta quotes 'The Application Specific Integrated Circuit is a unique type of IC that is designed with a certain purpose in mind. This type of ICs are very common in most hardware nowadays since building with standard IC components would lead to big and bulky circuits. An FPGA (Field Programmable Gate Array) is also a type of IC, but it does not have the programming built into it during the production. As the name implies, the IC can be programmed by the user as long as they have the right tools and proper knowledge. An ASIC can no longer be altered after it gets out of the production line. That is why the designers need to be totally sure of their design, especially when making large quantities of the same ASIC. The programmable nature of an FPGA allows the manufacturers to correct mistakes and to even send out patches or updates after the product has been bought. Manufacturers also take advantage of this by creating their prototypes in an FPGA so that it can be thoroughly tested and revised in the real world before actually sending out the design to the IC foundry for ASIC production.' (2015)

comparing both ASICs and FPGA is simple, an FPGA is a device which can be manipulated once it comes of the production line and in to the hands of the public and an ASICS device is something that has a fixed version in which cannot be manipulated once it becomes available to the public, both have their advantages and disadvantages.

Design method

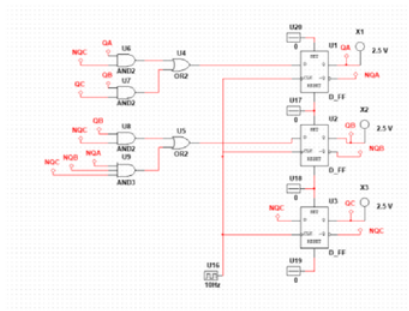
The design of the counter circuit contained multiple sub circuits to get it working, the 3 major circuits needed to reach the specification of the assignment were the 0-5 counter, Decade Counter and the decoder circuit. All these circuits were made individually and then eventually combined in PLD mode. Here is each circuit displayed individually with a brief description about each one.

Initial Design



Here is a basic overview of how the sub circuits should be connect along with the circuits previously mention there are a few decoders and a clock pulse device when all these circuits are linked together it should be able to deliver the 0-59 counter that is desired from the assignment

0-5 Counter

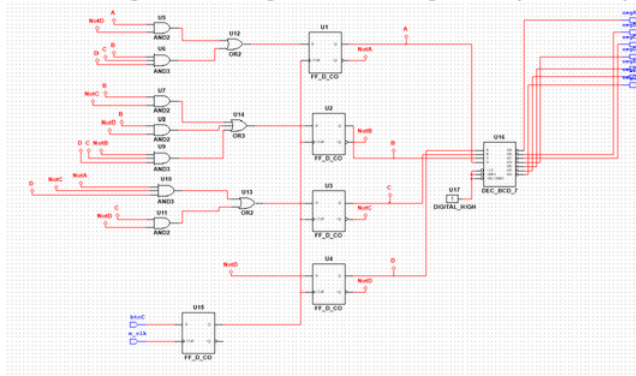


Here is the 1-5 counter circuit, this is the first circuit that was made, it uses a series of AND & OR gates with various different inputs, when inputs were activate in a particular order the circuit would count from 1-5 in binary using the LED's that are situated after the flip-flop gates as seen in the diagram to the left. This was edited slightly so it could fit in to the 0-59 counter circuit this was done by removing the LED's and replacing them with wireless connectors.

This circuit was simulated by replacing the inputs with switches and then changing the input from on to off manually changing the signal going through the logic gates causing lights to go on and off and count in binary.

Decade Counter

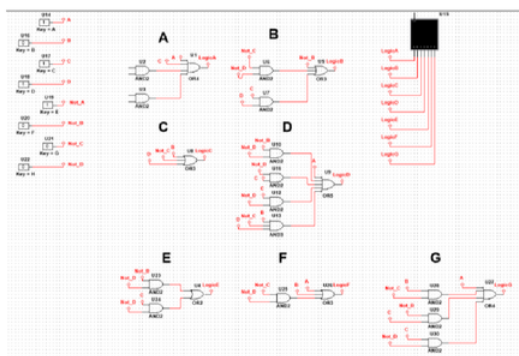
The decade counter counts from 1-10 similar to the 0-5 counter it is made up of a series of AND & OR gates, these gates are arranged in a particular pattern so when certain inputs are



activated it gives a specific output depending on them, this output travels through a flip-flop gate and eventually into a decoder that determines what it should display on the display screen on the nexys board.

To test this circuit the program was uploaded onto the nexys boards FPGA where it would work in combination with the buttons and display on the board, when certain buttons were pressed the display screen would display a number from 0-10 as desired.

Decoder



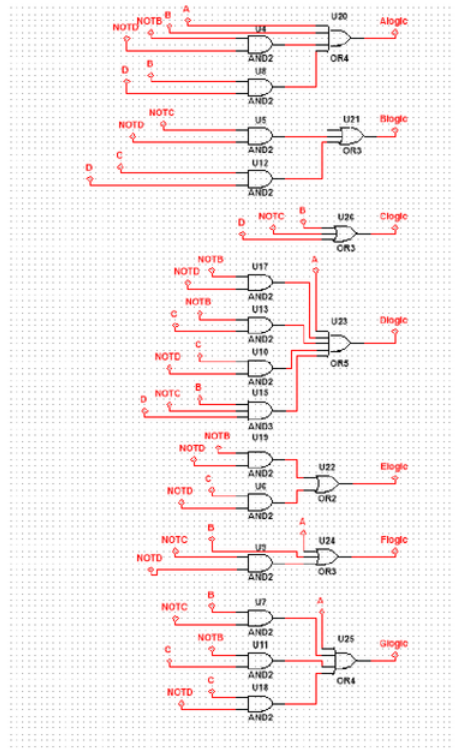
the decoder circuit simply does what it says in the name it 'decodes' this meaning it takes an input signal/vale and translates into something completely different, in this instance it is used to change a signal into something the multiplexer can read and use to determine the output signal it should sent to the digital display screen on the nexys board.

To test this circuit a digital display screen was used in simulation to display different numbers depending on what inputs were changed.

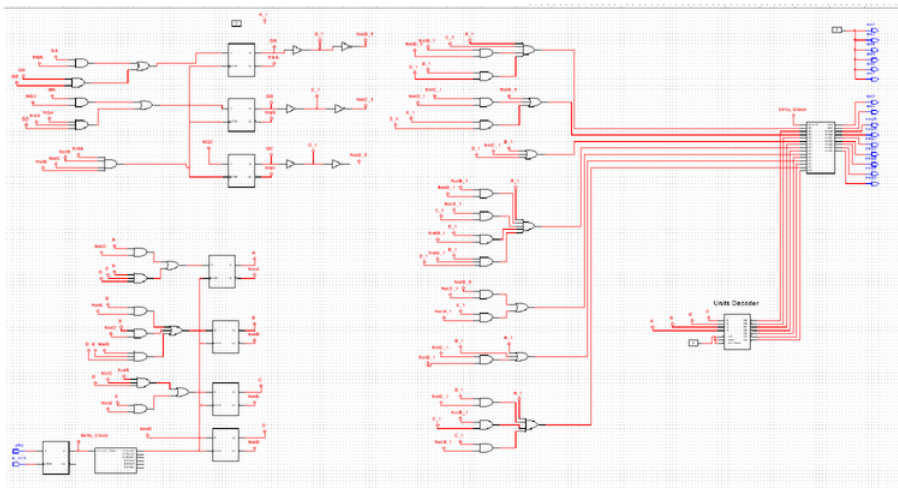
Similar to the previous circuits written about it uses a series of AND&OR gates to determine the overall output signal to send to the multiplexer that is too be connected in the final circuit.

Decoder V2

Due to the decoders previous format it had to be changed so it could be integrated into the combined 0-59 counter circuit so shown on the left is the edited version of the decoder circuit ready to be applied into the combined circuit.



Combined Circuit



Here is a picture of the circuits fully complete and combined into one bigger circuit along with the decoders and the clock pulse circuits, once this was done the next step was to test the circuit on the nexys board the ideal result from this would be a fully operational circuit that can count from 0-59 successfully. As the picture above displays it used all the previous circuits that have been mentioned above in conjunction with each other ultimately linked to one common output, when this is uploaded onto the FPGA on the nexys board it should give it the ability to count from 0-59 on the digital display on the board.

Analysis of results

Simulation Results

0-5 counter circuit

The 0-5 counter worked as expected, when certain inputs were changed the lights that were required to light up displaying a binary number lit up as expected, this was the first success of the assignment meaning that one of the 3 main circuits needed to build the complete counter worked, when the circuit lit up the testing order was to get the numbers to count from 0-5 this was successful and the lights responded to the correct inputs and there were no anomaly's.

Decade Counter

The decade counter was tested differently to the 0-5 counter, in this instance it was uploaded to the FPGA on the nexys board with the programme developed in PLD mode on multisim, the aims of this was to make the digital display count from 0-10 on the nexys board. When testing the decade counter the button was pressed 10 times, each individual time made the display number go up by 1, once at 10 the next time the button was pressed the decade counter reset ready to count back up to 10 again. This is what was required to meet the specification required for the combination circuit that would be build further on.

Decoder

The decoder has the ability to change one code into another, this was a requirement for the multiplexer in the combined circuit to work to test this out and make sure it had the ability to work in the circuit it was tested on multisim simulation using a digital 'digital display' feature on the programme, the display was hooked up to the combination of AND&OR gates, once connected the inputs that represented A,B,C,D,NA,NB,NC,ND where pressed in different combinations to get different results. When testing the decoder, it done as required but it needed editing so it cold fit into the combination circuit.

Combination circuit

The combined circuit was put together using all of the circuits previously mentioned, the objective of this circuit was to count from 0-59, this was the final stage of testing, to carry out this test the circuit was uploaded to a nexys board. Similar to the decade counter the digital display on the board is used to display the values required. Once the circuit was uploaded to the test board buttons were pressed and the circuit counted from 0-59. This was as expected and what was required for the assignment to meet full specification.

Conclusions

Conclusion & Recommendations

The final circuit was required to count from 0-59 in which it did, this was required to make the assignment a success however a few recommendations are still to be made as they would speed up the process. The first recommendation would be to design every circuit in PLD mode as when it comes to adding the circuit into the final combined circuit it would be a simple case of dragging and dropping the required circuits into place, however this was not possible as some of the circuits were built in the multisim design mode which could not be copied, this was an issue as rebuilding the circuit in PLD mode consumed time , time in which is essential to perfecting an assignment.

The final recommendation to be made would be to make all the on-page connectors have the same name on original design circuits as they would on the combined circuits, this would save having to change the name off all the connectors when they are copied across from a design to the final combined circuit.

However, the assignment was a success as the specification was met but next time a picture to display the nexys board working would have been ideal. Besides that, all that was required to be achieved was achieved and the nexys board did as required once the circuit was finished.

References & bibliography

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GRADEMARK REPORT

FINAL GRADE

GENERAL COMMENTS

Instructor

40/100

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GRADING FORM: CSG-RUBIC

CALLUM WILLIAMS

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RESEARCH-INFORMED LITERATURE



There was evidence of further reading and research however you need to include in text referencing

2

using Harvard. Your interpretation and understanding of the additional research was good. Your references were appropriate to the task, but the reference list was very short and limited to a small range of sources.

KNOWLEDGE AND UNDERSTANDING



The knowledge and understanding of the subject demonstrated by this assignment was generally satisfactory. However the report lacked a lot of the required detail and there were many gaps in your knowledge of the basic principles. Additionally, your understanding of the higher level concepts was not shown. Further work - There were a few omissions and misunderstandings throughout the task, which could be read up on for future reference. Explanations need to be written in much more detail and written in a more logical and clearer way.

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ANALYSIS



There was a brief testing section, but you should have tested each block as you built it. When building complex circuits you should test each block to ensure it meets the specification, otherwise when you test the overall circuit you will have big problems fault finding. Further work – you could have included a more detailed evaluation of the circuit performance.

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PRACTICAL APPLICATION AND DEP.



Your application of practical skills for this task were generally OK, you used the resources available in MultiSim appropriately when designing the circuit

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and you used appropriate options for testing and evaluating the circuit performance - albeit to a limited fashion. Testing generally lacked a lot of the required detail however and you should have included a comprehensive set of results for each stage.

SKILLS FOR PROFESSIONAL PRAC.



In this assignment you have demonstrated skills in working individually and also collaboratively. In general, the report was presented poorly. The diagrams, graphs and screenshots were too small to be legible and your text formatting was inconsistent. Your report structure and presentation needs to be improved with better use of diagrams, references and sentence structure.

2