

LEVEL 4 ASSESSMENT SPECIFICATION

Student name:	Harry Owen	Student ID number:	
Programme:	HNC Electrical/Electronic Engineering		
Module:	Electronics 1		
Module code:	PSDE4004	Contribution to Overall Module Assessment (%):	25%
Lecturer:	Jason Pointer	Internal Verifier:	Steve Roberts
Assignment Title:	Digital	Word count (or equivalent):	1500
Submission deadline:	11/04/19	Return date of provisional marks & written feedback:	
Submission method:	All written assessments, where practical and possible, must be submitted via Turnitin unless otherwise instructed by the Lecturer. (Please DO NOT put this assessment specification into Turnitin or it will match many similarities with other students' submissions.) Alternative submission method (if applicable): Late submission of the assessment will result in a late penalty mark. Penalties for late submission: Up to one week late, maximum mark of 40%. Over one week late, 0%. Only the Extenuating Circumstances Panel may approve a change to submission dates.		
Academic honesty / referencing:	Academic honesty is required. In the main body of your submission you must give credit to authors on whose research and ideas your work is based. Append to your submission a reference list that indicates the books, articles, etc. that you have used, cited or quoted in order to complete this assessment.		

Module Learning Outcomes (from module syllabus)

1. Demonstrate an understanding of semi-conductor components and characteristics and their application in analogue and **digital** electronic circuits.
2. To design, simulate, build, test and evaluate analogue and **digital** electronic circuits using information gained from datasheets.

STUDENT FEEDBACK FORM

This section details the *extent* to which the assessment criteria are demonstrated by you, which in turn determines your mark. The marks available for each category of skill are shown. Lecturers will use the space provided to comment on the achievement of the task(s), including those areas in which you have performed well and areas that would benefit from development/improvement.

Generic Assessment Criteria	Marks available	Marks awarded
1. Engagement with Literature Skills	10	2.5
Little evidence of reading including a lack of referencing to any source material. Information must have been gathered for debouncing.		
2. Knowledge and Understanding Skills	30	21.4
Achieved 63% for the combinational logic. Achieved 80% for the sequential logic. Excellent knowledge and understanding of the basic underlying concepts and principles of digital systems, especially sequential systems.		
3. Cognitive and Intellectual Skills	10	4.5
Limited attempt at evaluation of the underlying concepts and principles, tending towards description.		
4. Practical Application Skills	40	29
Achieved 70% for the combinational logic. Achieved 75% for the sequential logic. An excellent application of practical and simulation work to obtain all of the required results.		
5. Transferable Skills for Life and Professional Practice	10	5.5
Mostly coherent, organised and accurate work, in a suitable structure and is for the most part clearly expressed.		

Assessment Mark (Assessment marks are subject to ratification at the Exam Board. These comments and marks are to give feedback on module work and are for guidance only until they are confirmed.)

Late Submission Penalties (tick if appropriate)

Up to 1 week late (40% Max)

Over 1 week late (0%)

63%



References

Used for the title picture -

https://www.google.co.uk/url?sa=i&rct=j&q=&esrc=s&source=images&cd=&cad=rja&uact=8&ved=2ahUKEwit7MGUwfzhAhVGxIUkHZqICYcQjRx6BAgBEAU&url=https%3A%2F%2Fwww.assignmenthelp.net%2Fassignment_help%2FDigital-Systems&psig=AOvVaw17epL_ebJHDqiZg2Xm_Lr-&ust=1556874908483073

<https://learn.sparkfun.com/tutorials/analog-vs-digital/all> - Used for information when explain the difference between a digital and analogue system.

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Heading

Should be on a new page.

In this assignment I will be looking to demonstrate an understanding of semi-conductor components and their characteristics along with their application in analogue and digital electronic circuits. I will also look to design, simulate, build, test and evaluate analogue and digital electronic circuits using information gained from datasheets. This will be done through practical and computer based exercises.

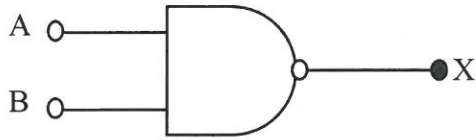
To quickly start this assignment off I want to explain what a digital system is and what the difference is between digital and analogue. Analog and digital signals are used to transmit information, usually through electric signals. In both these technologies, the information, such as any audio or video, is transformed into electric signals. The difference between analogue and digital technologies is that in analogue technology, information is translated into electric pulses of varying amplitude. In digital technology, translation of information is into binary format (zero or one) where each bit is representative of two distinct amplitudes.

*You should have looked at digital systems in detail i.e.
What is logic, different gates etc.*

Task 1 - Combinational Logic

Using Multisim construct and test the following circuits using NAND gates. For each circuit complete a truth table and measure the logic value at each point indicated in the truth table. Write down the simplified Boolean expression and check that the measured values agree with the expected values.

(a)



A	B	X
0	0	1
0	1	1
1	0	1
1	1	0

$$X = \bar{A} \cdot \bar{B} + \bar{A} \cdot B + A \cdot \bar{B}$$

$$X = \bar{A} \cdot B$$

This should be written in a past tense.

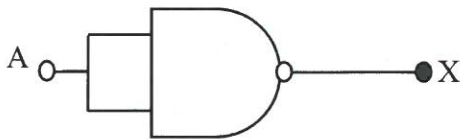
	A	B	C	D	E	F	G	H
000	0	0						1
001	0	1						1
002	1	0						1
003	1	1						0

Conversions:

- $\rightarrow$ $\rightarrow$ $\rightarrow$
- $\rightarrow$ $\rightarrow$ $\rightarrow$
- $\rightarrow$ $\rightarrow$ $\rightarrow$
- $\rightarrow$ $\rightarrow$ $\rightarrow$
- $\rightarrow$ $\rightarrow$ $\rightarrow$
- $\rightarrow$ $\rightarrow$ $\rightarrow$
- $\rightarrow$ $\rightarrow$ $\rightarrow$

A'+B'

(b)



A	X
0	1
1	0

$$X = \bar{A}$$

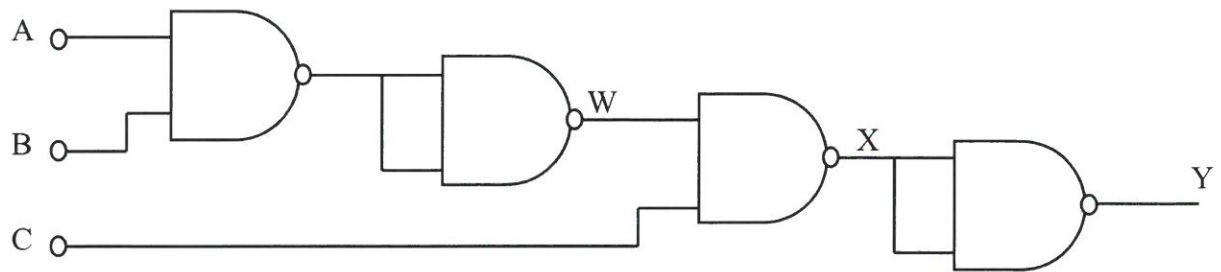
	A	B	C	D	E	F	G	H
000	0							1
001	1							0

Conversions:

- $\rightarrow$ $\rightarrow$ $\rightarrow$
- $\rightarrow$ $\rightarrow$ $\rightarrow$
- $\rightarrow$ $\rightarrow$ $\rightarrow$
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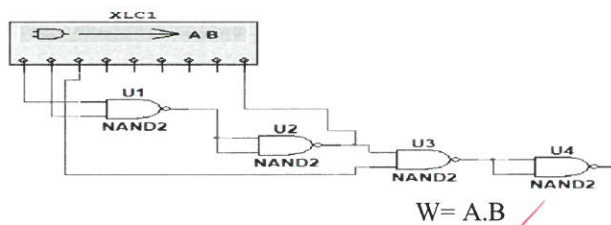
A'

(c)



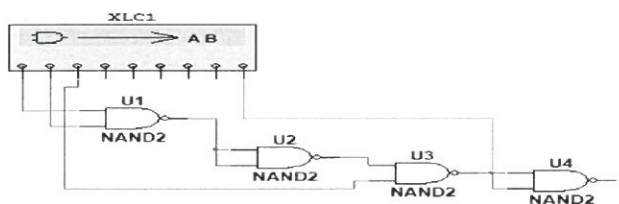
A	B	C	W	X	Y
0	0	0	0	1	0
0	0	1	0	1	0
0	1	0	0	1	0
0	1	1	0	1	0
1	0	0	0	1	0
1	0	1	0	1	0
1	1	0	1	1	0
1	1	1	1	0	1

State the logic function for W, X and Y and simplify.

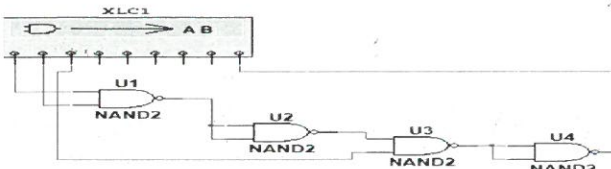


Logic Converter-XLC1

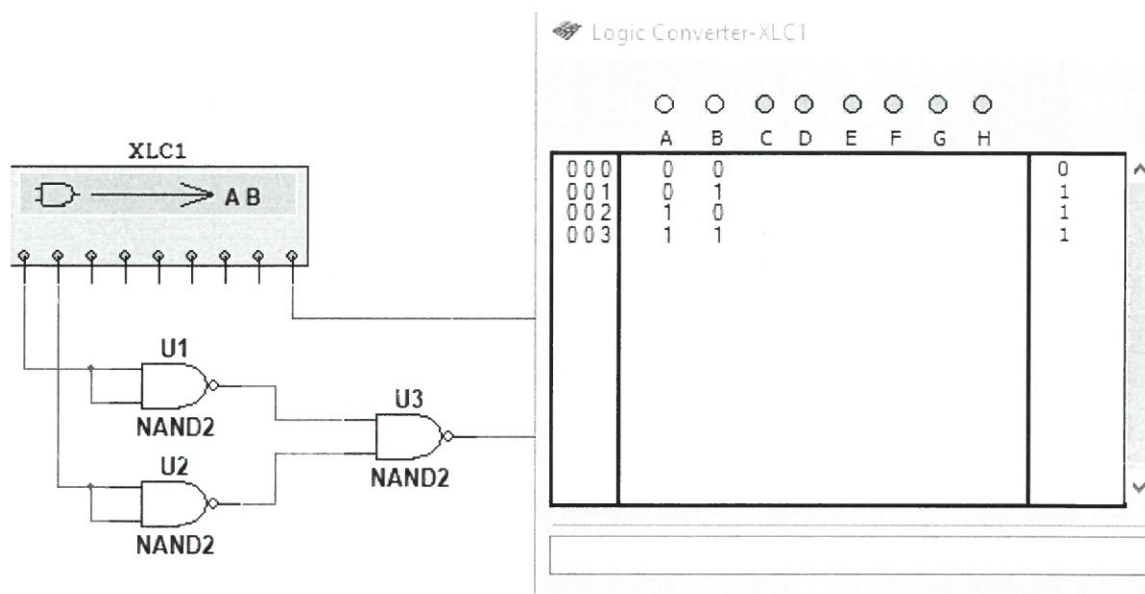
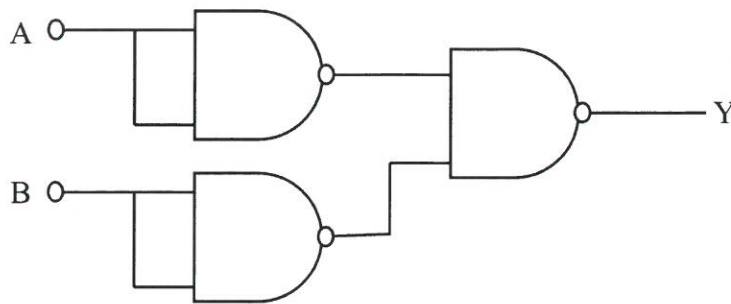
A	B	C	D	E	F	G	H
0	0	0	1	0	0	0	0

[illegible]

No expression

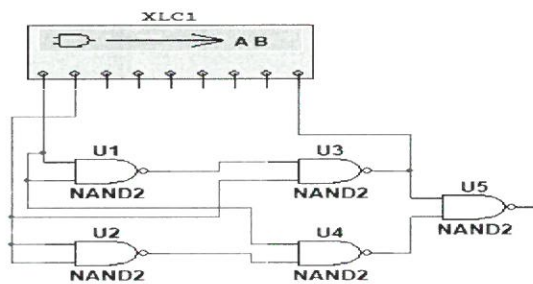
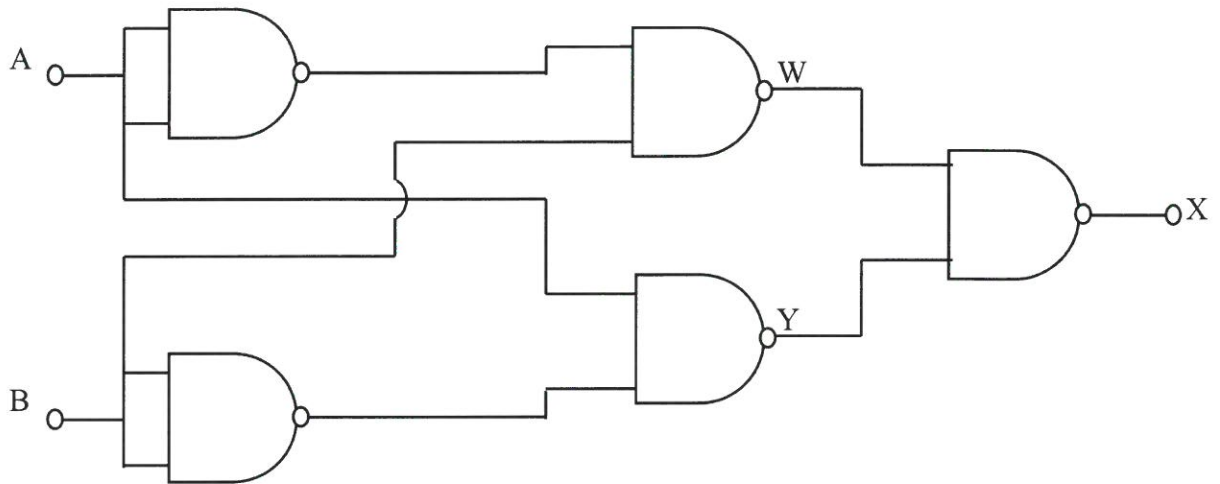
[illegible]
$$Y=A.B.C$$

- (d) What will be the output of the circuit below? If A of circuit (b) is connected to Y what will be the new output.



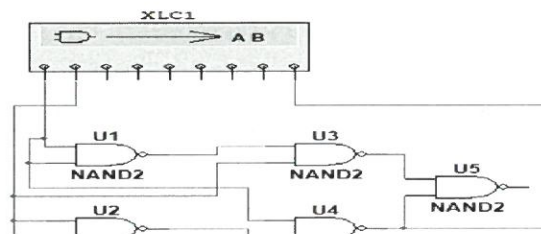
The circuit arrangement above is the same as a single OR gate. If the addition of another NAND gate was to be added at the end of the above circuit, it would result in a NOR gate.

- (e) Construct the following circuit and measure the logic values at W, Y and X. Determine the output equation and confirm that the theoretical values agree with the measured values.



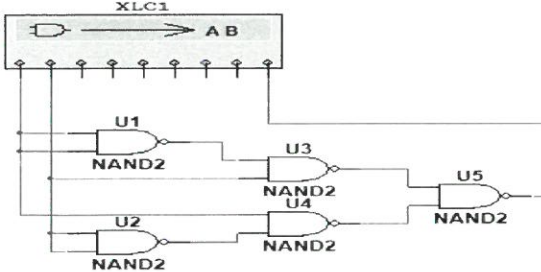
Logic Converter-XLC1

	A	B	C	D	E	F	G	H
0000	0	0	0	0	0	0	0	0
0001	0	0	0	0	0	0	0	1
0010	0	0	0	1	0	0	0	0
0011	0	0	0	1	0	0	0	1



Logic Converter-XLC1

	A	B	C	D	E	F	G	H
0000	0	0	0	0	0	0	0	0
0001	0	0	0	0	0	0	0	1
0010	0	0	0	1	0	0	0	0
0011	0	0	0	1	0	0	0	1



Logic Converter-XLC1

	A	B	C	D	E	F	G	H
0000	0	0	0	0	0	0	0	0
0001	0	0	0	0	0	0	0	1
0010	0	0	0	1	0	0	0	0
0011	0	0	0	1	0	0	0	1

A'B+AB'

$$X = \bar{A}.B + A.\bar{B} \text{ (This is the same as an XOR gate.)}$$

- (f) Simplify the following Boolean equations, ONLY using the LAWS OF BOOLEAN ALGEBRA and DeMORGANS THEOREM. Verify your findings by constructing the logic circuits using NAND gates.

i) $F = A(A + \bar{B})$

$F = A.A + A.\bar{B} = A + A.\bar{B} = A.(1 + \bar{B}) = A.1 = A$
(No logic needed, its simply a straight input to output)

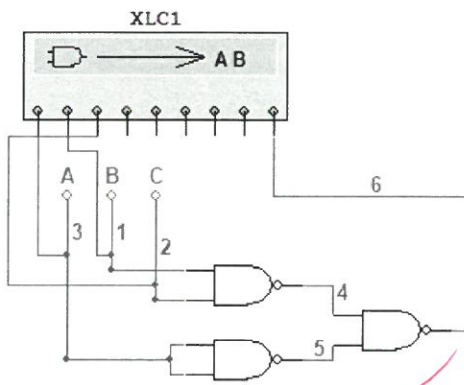
good.

ii) $F = (A + B)(C + A)$

$F = A.C + A.A + B.C + A.B = A.C + A + B.C + A.B = A(C + 1 + B) + B.C = A + B.C$

Using DeMorgans theorem $\bar{F} = \overline{A + B.C} = \bar{A} + \overline{B.C} = \bar{A} + \bar{B}. \bar{C}$ Type equation here.

Not completed.



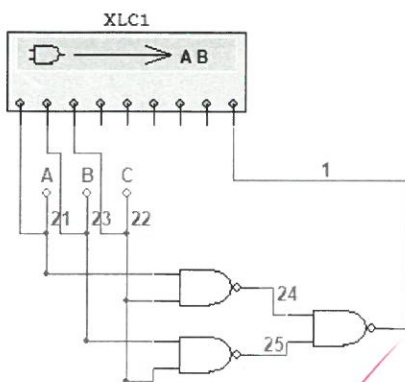
	A	B	C	D	E	F	G	H	Out
000	0	0	0						0
001	0	0	1						0
002	0	1	0						1
003	0	1	1						1
004	1	0	0						1
005	1	0	1						1
006	1	1	0						1
007	1	1	1						1

BC+A

iii) $F = (A + B)C$

$F = A.C + B.C$

Using DeMorgans theorem $\bar{F} = \overline{A.C + B.C} = \overline{A.C} . \overline{B.C} = (\bar{A} . \bar{C}) . (\bar{B} . \bar{C}) = (\bar{A} . \bar{B} . \bar{C})$



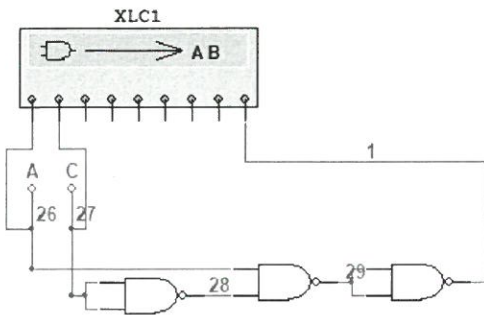
	A	B	C	D	E	F	G	H	Out
000	0	0	0						0
001	0	0	1						0
002	0	1	0						1
003	0	1	1						1
004	1	0	0						1
005	1	0	1						1
006	1	1	0						1
007	1	1	1						1

AC+BC

$$\text{iv) } F = (\bar{A} + \bar{B} + \bar{C})(A + \bar{B} + \bar{C})(A + C)(B + \bar{C})$$

$$F = (\bar{B} + \bar{C})(A + C)(B + \bar{C}) = \bar{C} \cdot (A + C) = A \cdot \bar{C} + C \cdot \bar{C} = A\bar{C} + 0 = A\bar{C}$$

(Unable to do DeMorgans therom due to this logic being ineffective when converted)



Logic Converter-XLC1

Out

	A	B	C	D	E	F	G	H
000	0	0	0					0
001	0	0	1					0
002	0	1	1					0
003	0	1	0					1
004	1	0	0					1
005	1	0	1					0
006	1	1	0					1
007	1	1	1					0

Conversions

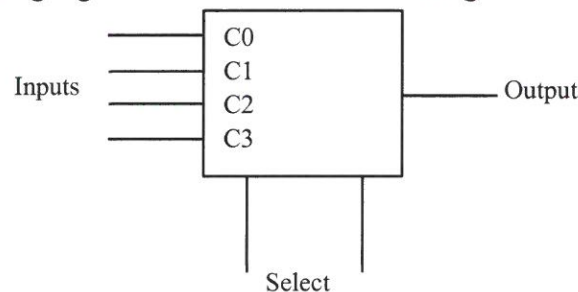
☐ $\rightarrow$ $\overline{101}$
☐ $\rightarrow$ $A|B$
☐ $\rightarrow$ $\overline{101}$ $\rightarrow$ $A|B$
☐ $\rightarrow$ $\overline{101}$
☐ $\rightarrow$ $\overline{101}$
☐ $\rightarrow$ $\overline{101}$

AC'

You are missing the DeMorgan.

Task 2 - Multiplexer

An arrangement where several inputs can be connected but only one output, under the influence of a select input, will have access to the output. The block diagram below shows a 4-to-1 multiplexer, produce a truth table and the Boolean equation to representation the multiplexer. Use this information to design the 4-to-1 multiplexer using logic gates and test its function using Multisim.

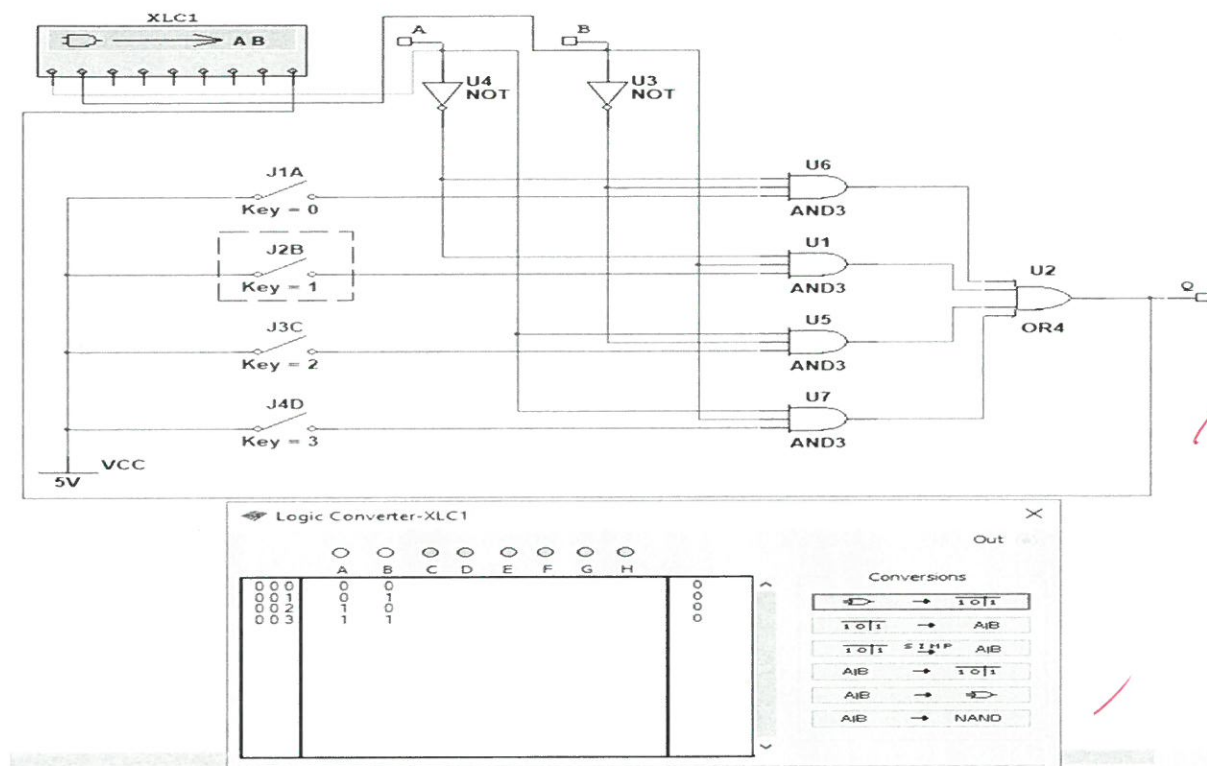


A multiplexer is a combinational logic circuit designed to switch one of several input lines through to a single common output by the application of a control signal.

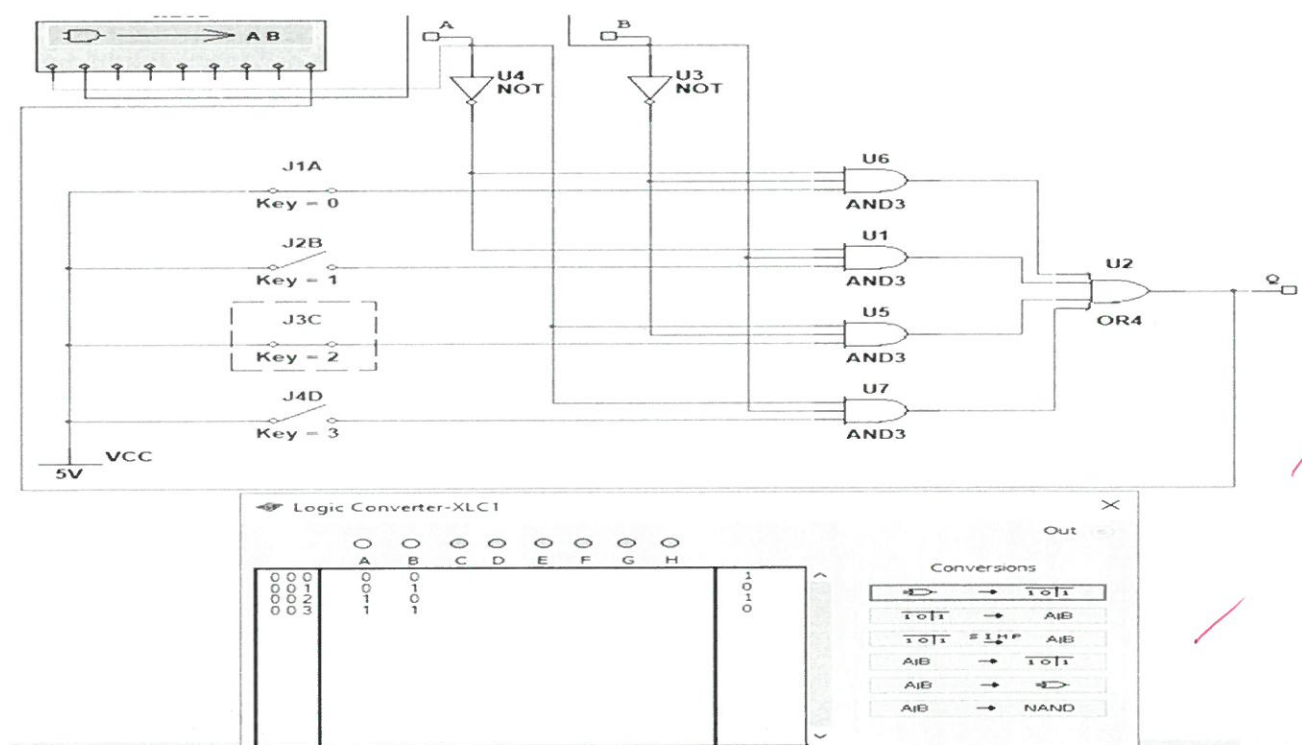
A	B	Q
0	0	C1
1	0	C2
0	1	C3
1	1	C4

Above shows the truth table for a 4-1 multiplexer. Below states the Boolean equation for the circuit.

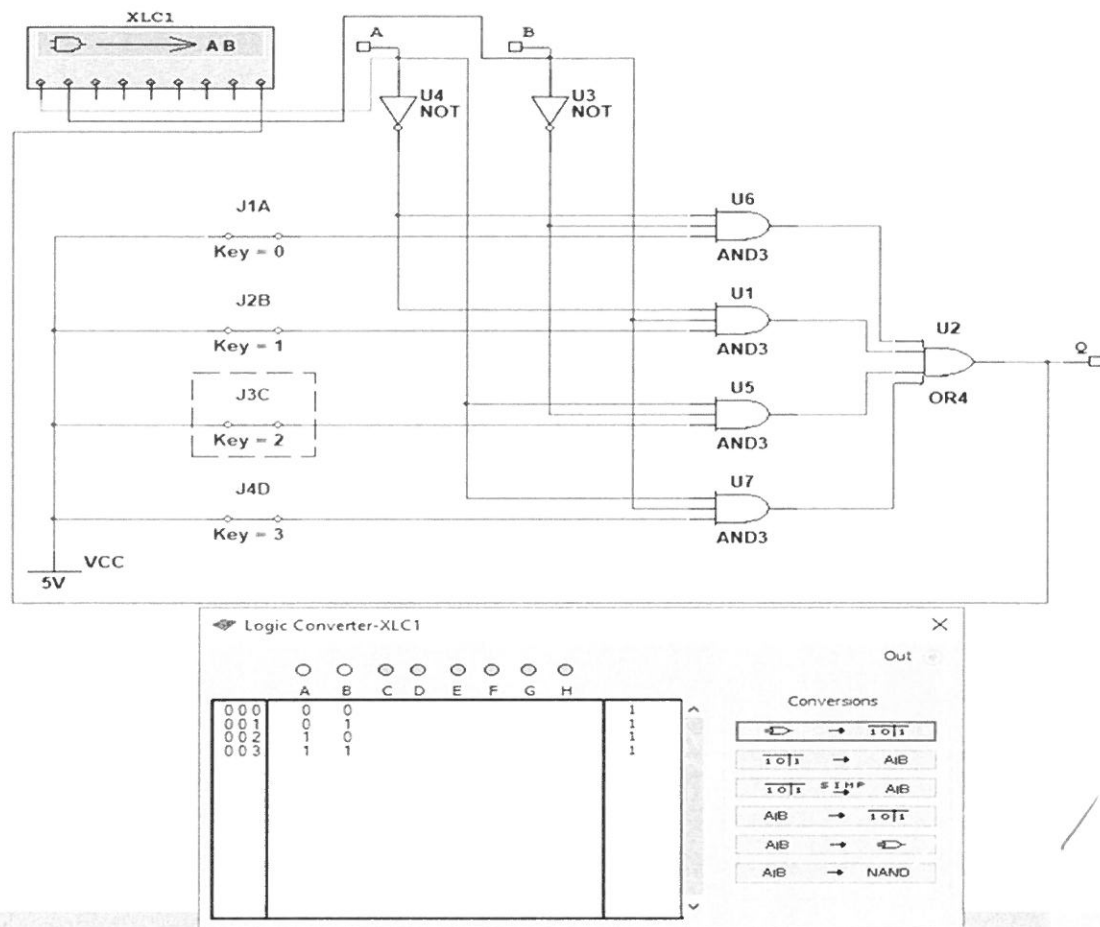
$$Q = \bar{A} \cdot \bar{B} \cdot C1 + A \cdot \bar{B} \cdot C2 + \bar{A} \cdot B \cdot C3 + A \cdot B \cdot C4$$



This shows the circuit with the 4 input signal switches open. This shows there is no output to Q when all switches are open.



This shows the circuit with random switches open and some closed. This gave an output to Q.



This shows that when all switches are closed and signal is present that there is an output on Q. This gives evidence to support my truth table and Boolean expression.

Task 3 - Sequential Logic

The truth table of the D-type and J-K Flip-Flop

- (a) Construct the following debouncing circuit, and connect the clock of a D-type flip-flop to the output. Monitoring the clock, Q and QBAR outputs with LEDs and complete Table 1.

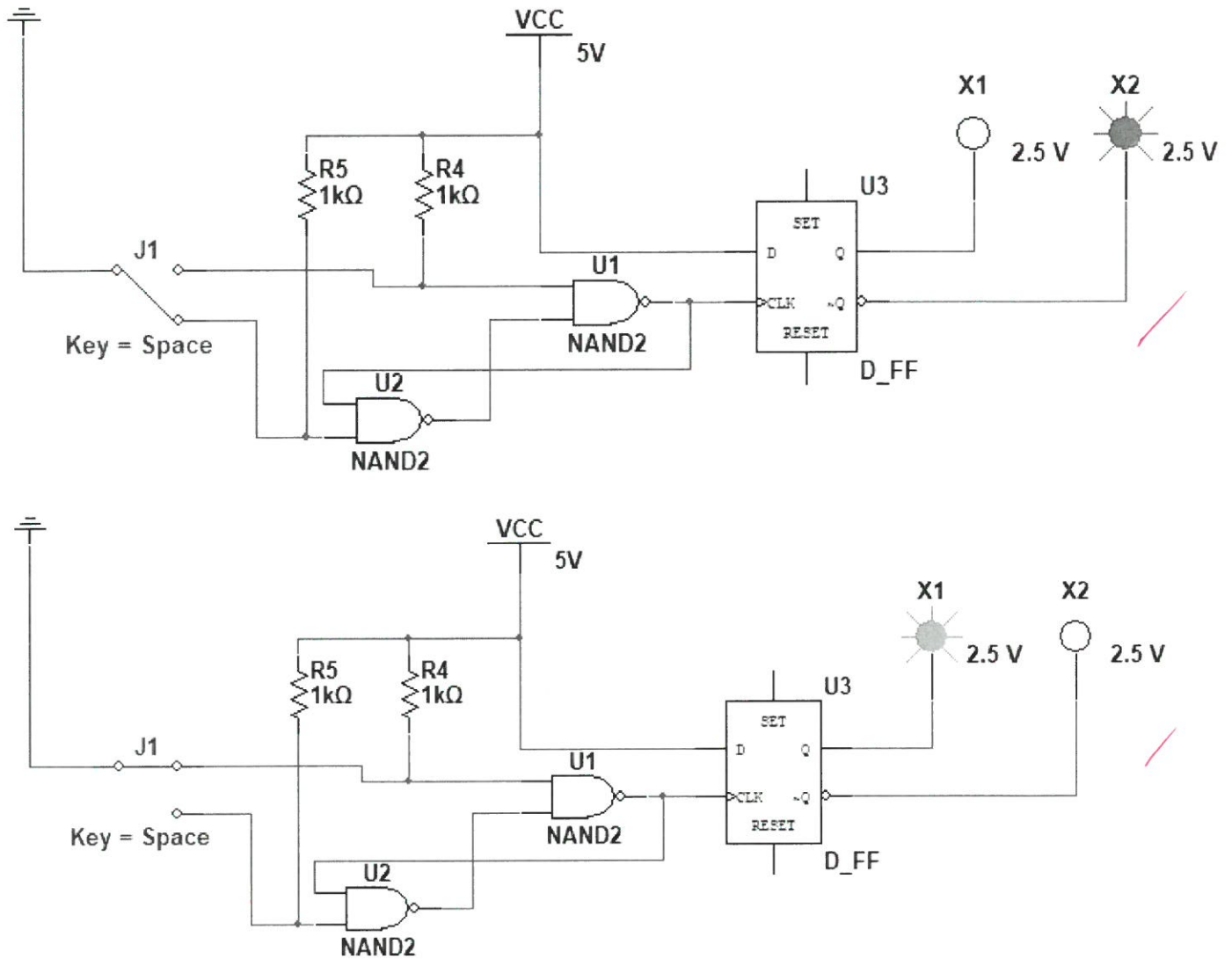


Table 1 - D-type truth table

Input	Outputs	
D	Q	$\bar{Q}$
0	0	1
1	1	0

B) Now connect the clock of J-K flip-flop to the output. Monitoring the clock, Q and QBAR outputs with LEDs and complete Table 2.

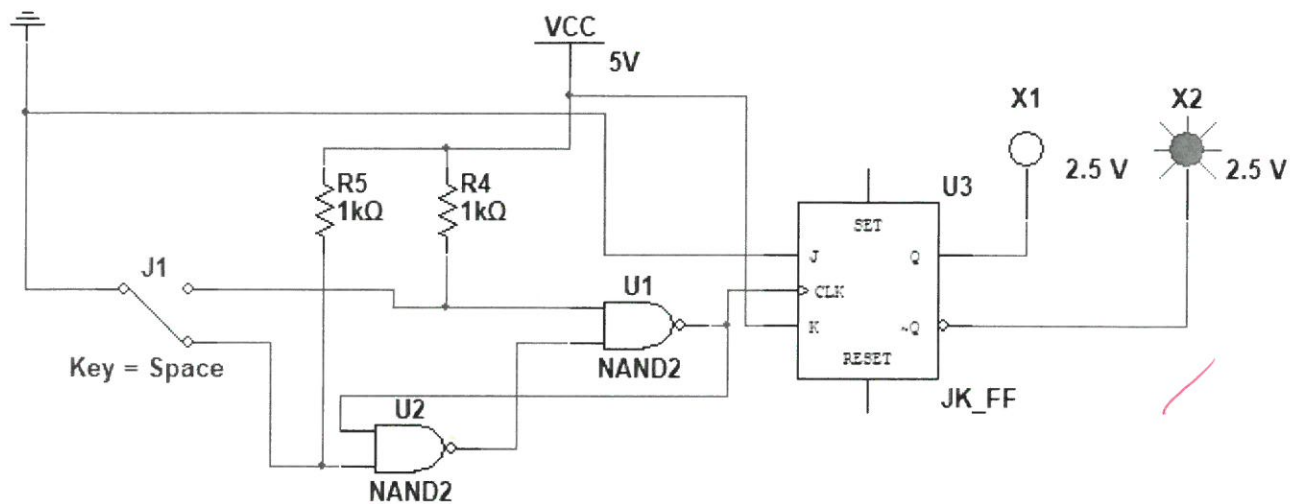


Table 2 – J-K truth table

Input		Outputs	
J	K	Q	$\bar{Q}$
0	0	NoChange	NoChange
0	1	0	1
1	0	1	0
1	1	Toggle	Toggle

C) The cross-coupled NAND gates are for switch debouncing. Why are they needed and how do they work?

Bouncing is when two contacts in electronic signals generate multiple signals when the contacts open and close. Debouncing ensures that only one single signal is accepted when an open and close contact is made. Would could imagine this to be a problem with counting circuits or typing circuits. A set-Reset latch or SR is an easy way of stopping this problem from occurring. When NAND gates are used they have one gate as the output and the other feeding back into the first gate. This circuit latches the signal until it is broken and prevents any more than one signal being received until the switch is broken.

Task 4 - Using Sequential Logic to Solve Real Problems

Design a synchronous 0-5 counter using D-type flip-flops, the design must include a state table and Karnaugh maps. Once the design has been produced use a suitable simulation package to test the function of the counter and comment upon the results.

STATE TABLE –

Current			Next			Inputs		
Qa	Qb	Qc	Qa	Qb	Qc	Da	Db	Dc
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	0
0	1	0	0	1	1	0	1	1
0	1	1	1	0	0	1	0	1
1	0	0	1	0	1	1	0	1
1	0	1	0	0	0	0	0	0

KARNAUGH MAPS –

Qa	Qb Qc			
	00	01	11	10
0	0	0	1	0
1	1	0	X	X

$$D_a = Q_b \cdot Q_c + Q_a \cdot \overline{Q_c}$$

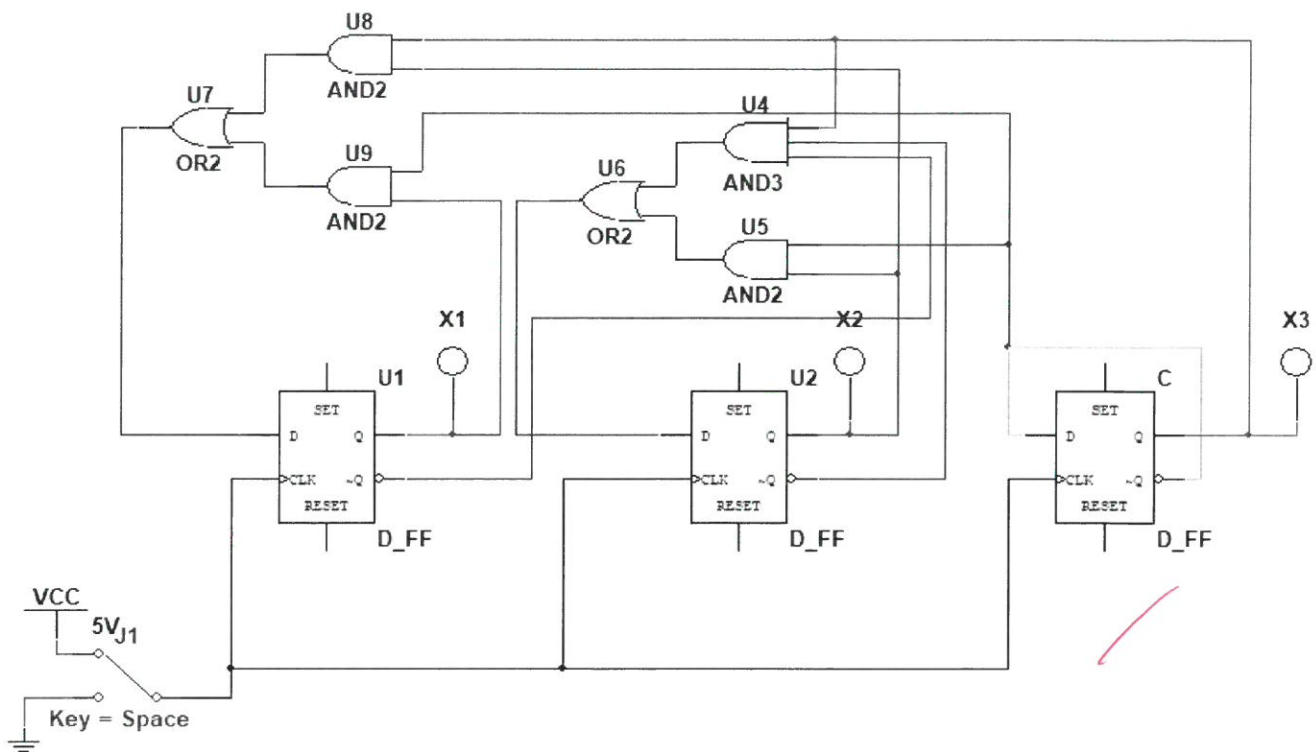
Qa	Qb Qc			
	00	01	11	10
0	0	1	0	1
1	0	0	X	X

$$D_b = \overline{Q_a} \cdot \overline{Q_b} \cdot Q_c + Q_b \cdot \overline{Q_c}$$

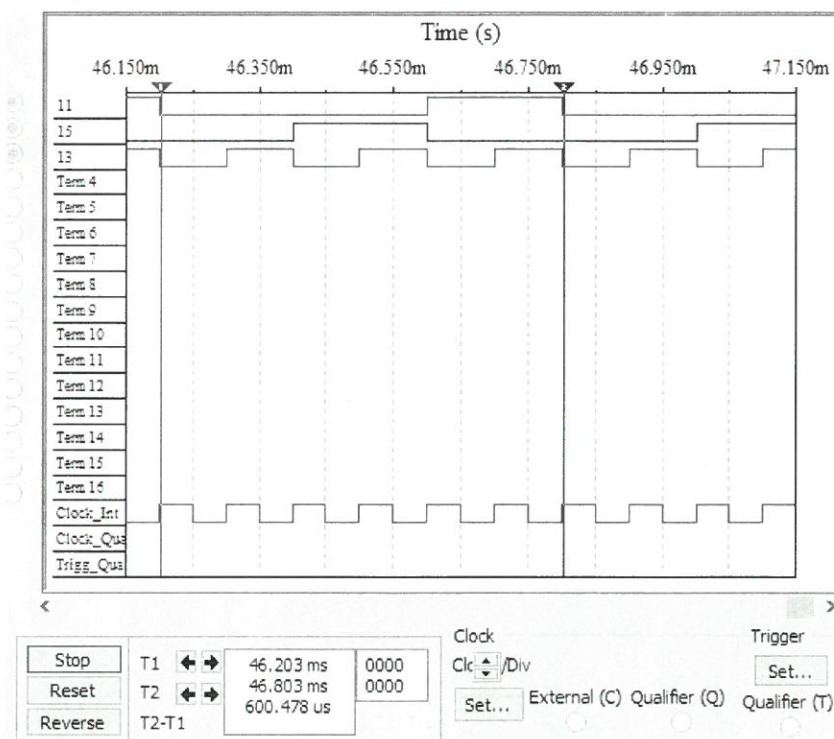
Qa	Qb Qc			
	00	01	11	10
0	1	0	0	1
1	1	0	X	X

$$D_c = \overline{Q_c}$$

Above shows the truth table and karnaugh maps. These helped in the design as it allowed me to see the simplest way to wire the circuit.



Logic Analyzer-XLA1



Above shows the circuit I created. It uses D type flip flops. The D type flip flop is a basic building block of sequential logic circuits. It is a circuit that has two stable states and can store one bit of state information. It changes with a change in input signal. The circuit worked as expected with the switching working in order. I problem I found was that there was a lot of gates and links between flip flops which could have been reduced with the use of JK flip flops as it allows a change in high and low state with the multiple input signals. This would reduce the gates used in the circuit and would make it easier to wire and visual inspect.

You have included no references.