

1451789

by Joshua Williams

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Good comprehensive table of figures

1. Executive summary

The report delves into background research into fabrication faults in integrated circuits (ICs) with heavy emphasis on the popular technique SSF fault model. This uses logic gates with inputs and outputs being logic SA0 or SA1 (SA being Stuck-at-fault). The techniques used in modern manufacturing were also explored and the benefits of these technologies being implemented into a business. The wider engineering requirements were also looked at such as machine vision systems due to the fact that most facilities will see this as the future of any manufacturing business model. The last section of research investigates ESD (Electro-Static-Discharge). This is where a momentary flow and sudden of electric current between two electrically charged objects caused by contact, dielectric breakdown or an electrical short. It is essential in knowing prevention methods in electronic production as the discharge has the capabilities of permanently damaging circuit components. The designing of the CUT (Circuit-under-test) is generated on the software Multisim. This is where the word generator and 6-bit register were designed and tested under the same 3 fault conditions. The next designing step was using the LabView program, which developed a G-code program to communicate with the DAQmx development board to produce the fault conditions. The last step was to produce a CAM (Computer-Aided-Manufacture) printed circuit board (PCB) on the industry standard software Eagle. The CAM design was manufactured and then tested on the DAQmx development board, and this also had the fault conditions applied to show the PCBs capabilities.

This summary demonstrates an extensive understanding of the requirements.

2. Research

2.1 Fabrication faults in ICs

In modern fabrication processes and the ever-increasing complexity of modern ICs (Integrated Circuit) small variations could result in poor construction within circuitry and faults built in.

The term failure mode is used as an expression of a “defect” at the electrical level. Failure modes are modelled at behavioural or faults at logic (UMBC, 2004).

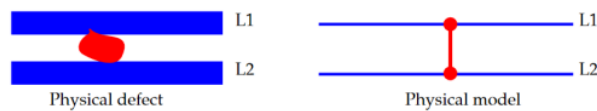


Figure 1 - Failure Modes (UMBC, 2004).

Through the logic level, failure mode can be translated in different ways (UMBC, 2004).

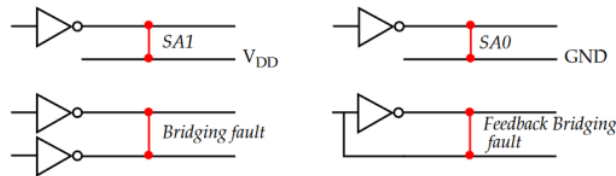


Figure 2 - Different Failure Modes (Plusquellic, 2007).

Figure 2 is showing the possibility of the logic gate being forced either to logic 1 (Stuck at 1) or logic 0 (Stuck at 0). By defect this is linking the output to the voltage ground or high, however this can not only be the one cause of SA0 or SA1 (Plusquellic, 2007).

Another known fault is when the bridging faults between two gates or between the output and the feedback. This is through shortage of two unconnected signals which then creates a new line of logic (Plusquellic, 2007).

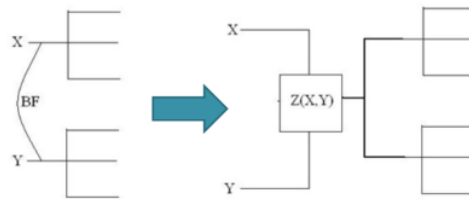


Figure 3 - Representation of a Bridging Fault (Owen, 2016).

Presume that the bridging fault lays between signals X and Y. It is designated by (X.Y) and the function generated by it being Z (X.Y). If the values for the shorted signals the same, then the response of the function would be the same. When the values for the signals are different, the two values could be driven (Owen, 2016).

The output function can be:

OR of the two signals – OR bridging fault

AND of the two signals – AND bridging fault

OR bridging fault

When the function generated is the OR, then it is represented as an OR bridging fault between the signal lines. Shown in Figure 4, OR (X.Y) will be driven to the next signal lines (Owen, 2016).

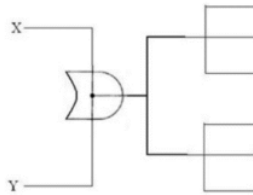


Figure 4 - OR Bridging Fault (Owen, 2016).

AND bridging fault

When the function is generated as an AND, then this represents an AND bridging fault between the signal lines. AND (X.Y) will be driven to the next signal lines (Owen, 2016).

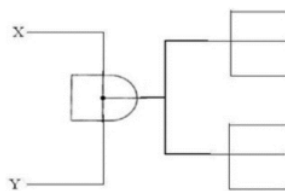


Figure 5 - AND Bridging Fault (Owen, 2016).

The last type of bridging fault is the feedback bridge fault (Figure 6). This creates a feedback loop and is referred to as FBF. The FBF converts the combinational circuit to the sequential circuit (Owen, 2016).

Excellent explanations here with good relevant examples

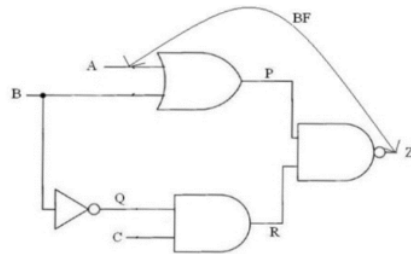


Figure 6 - Feedback Bridge Fault (Owen, 2016).

Transistor stuck at fault - Transistors have the possibility of developing faults where they are forced open or closed. Consider Figure 7, if there is a stuck at fault (closed) on transistor 1, then even when in put a has a logic value 1 this transistor is conducting. Therefore, applying the input vector $a=1, b=1, c=1$, there is a path from ground to source and the output, node z, will have a value somewhere between a logic 1 and a logic 0; this indeterminate value must then be propagated to an output. The other fault stuck open the transistor is never conducting as the operation of the cell consecutive nature. In an unfaulty circuit, a path for either ground to the output or source to the output. If the path is disabled, through a nonconducting transistor, the output will always preserve the previous value (Reeves, 2023).

	tests for					
	tso		tsc			
	abc	z/z'	abc	z/z'		
1	111	0/0	111	0/X		
	011	1/0				
2	111	0/0	111	0/X		
	101	1/0				
3	111	0/0	111	0/X		
	110	1/0				
4	000	1/1	110	1/X		
	111	0/1				
5	000	1/1	101	1/X		
	111	0/1				
6	000	1/1	011	1/X		
	111	0/1				

Figure 7 - Transistor Level of a Three Input Nand Gate (Reeves, 2023).

2.2 Methods and techniques required to manufacture a sustainable product that meets the wider engineering requirements

2.2.1 Machine vision systems

Machine vision systems surrounds itself with industrial and non-industrial applications. With the combination of software and hardware this can provide operational guidance to devices with execution of their functions with close attention to capturing and processing images. Machine vision systems require digital sensors protected inside the industrial cameras with specific optics to acquire images. The computer software and hardware will process, analyse, and measure numerous characteristics for decision making (Cognex, 2023).

The vision system method can be used when an object needs to be measured. An example of this is when determining a spark plug gap or location requirements for a robot to align parts in a manufacturing process. Figure 8 is showing how a system can be implemented to pass or fail oil filters (right) and measure the centre of the bracket (left) (Cognex, 2023).

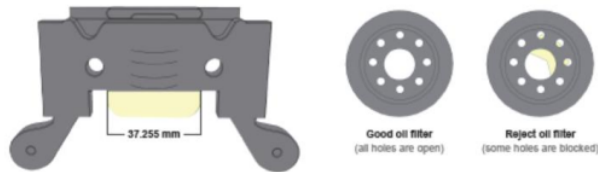


Figure 8 - Pass or Fail Example (Cognex, 2023).

An example product of this type of application is shown through the NI smart cameras from LabView.



*Good application examples
used here to support research*

Figure 9 - NI Smart Camaras (NI, 2023).

The Smart camaras (Figure 9) are industrial, high-quality image sensors with a combination of powerful processors to create an all-in-one solution for machine vision applications. Several different NI software's can be used to configure the camara. The one focused in this research is Vision assistant as this would be best suited. The Vision assistant is an algorithm engineering tool that will simplify vision system implementation by assisting user in developing algorithms for deployment on either the CPU or FPGA (NI, 2023). *This is a good significant finding in the research*

When the algorithm has been completed, the Vision Assistant can generate code in LabView or C. This code will be implemented into the controller. Then using the software (Figure 10) it can easily be modified tom incorporate the code into other parts of the system (NI, 2023). *These sentences should be cobined into a single sentence*

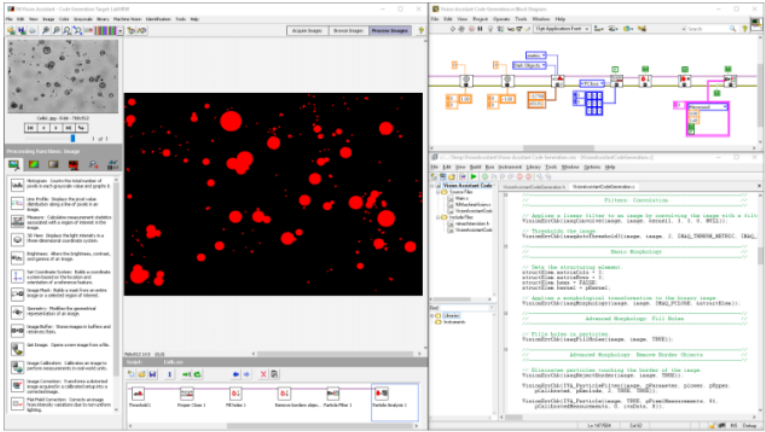


Figure 10 - Vision Assistant to generate LabView or C (NI, 2023).

2.2.2 In Circuit Test and Component Testing

In-circuit test (ICT) is applied after the assembly stage. This will verify if the circuit has the correct functioning capabilities and position of the electronic component on the PCB is correct. The test encompasses the verification of short circuits, open circuits, resistance, capacitance, and other parameters. For this purpose, a flying probe is required, built on an array of drivers and sensors that will perform measurements required by the test by moving freely on the board. An alternative test fixture could be used, consisting of a bed of nails (Figure 45, Appendix 1A,) and designed specifically for DUT (Device Under Test). Each "nail" acts like a real sensor, able to locate a point of a DUT to test the system. The method Bed-of-nails is an expensive and not pliable technique. It is not suitable when the board has high component density (Proto-electronics, 2023).

Very good explanantion and relevant supporting image example

2.2.3 Frequency signature recognition

The method of vibration monitoring is becoming a staple in maintenance regimes and relies on characteristics of different vibrations which rolling bearings exhibit as the rolling surfaces degrade. A method from SKF uses a technique of vibration FFT (Fast Fourier Transform) spectrum this tool is very useful in vibration analysis. If a machinery problem persists, FFT spectra can provide the information to diagnose the fault and causes of the issues. The other useful element is seeing the trend and how long until the problem is critical (Mais, 2002).

Minor grammar error

An example of this practice shown in Appendix 1A, Figure 46. A running speed at $F = 45\text{Hz}$, harmonics of running speed at $F = 75\text{Hz}$ and bearing defect frequencies at 516Hz and 650Hz . This is now shown in overlay markers (Mais, 2002).

Good research findings here that underpins a good relevant understanding of the concept, and its use in industry

2.2.4 Contactless sensing in manufacturing

Proximity sensors are the long-standing innovators of contactless sensing in automated systems. The ability for proximity sensors to collect and convert information into electrical signals without contact shows they are highly regarded in systems (Fk-instrument, 2022).

These automation devices revolutionised many industries with some of the following features:

Contactless sensing – the sensory element in proximity sensors allows for relevant data collection via the contactless sensing, a common feature required for most manufacturing facilities (Fk-instrument, 2022).

Diverse Applications – with comparison to optical sensors, proximity sensors are better in accommodating changes in temperature and moisture environments (Fk-instrument, 2022).

It is worth explaining that the vision and frequency detection systems are inclusive of the contactless sensing topic area.

2.3 Electro-Static Discharge (ESD) and methods used

2.3.1 Electro-Static Discharge (ESD) Effects

ESD is when a momentary flow and sudden of electric current between two electrically charged objects caused by contact, dielectric breakdown or an electrical short. Firstly, ESD required a build-up of electrostatic charge. This is when two objects rub together, one of the components become positively charged and the other is negatively charged (through the flow of electrons) (Parker, 2023).

From this the results are a positively charged component now having electrostatic charge. This component will come into contact with the right component, it will then transfer. Thus, causing an electrostatic discharge (Parker, 2023).

This behaviour results in the positively charged material now having an electrostatic charge. When that charge encounters the right material, it transfers and creates an electrostatic discharge (Parker, 2023).

ESD damage to electronic are summarised in three categories:

Soft Failures – ESD can alter the internal logic, this causing the system to lock up or behave unexpectedly. ESD can disrupt data flow in electronic systems. Although the effect is temporary, ESD events can slow down communication or require a reboot of systems in an event of a lockout (Omazaki, 2023).

Latent Defects – means the degrading of components. Latent failure is not so noticeable in circuits. It is where the device has been damaged and does not fail instantly. As the damage is not apparent, successive damage can continue to occur before failures. As the component is partially damaged the failure can occur years later. The discharge of electricity near active electronic components can cause memory corruption or temporary failure (Omazaki, 2023).

Catastrophic Failures – this failure causes permanent damage to an ESD sensitive component. This could have been caused by a metal melt, junction breakdown or oxide failure. Under normal inspection this would be detected. This type of failure in an electronic component can usually be the least costly as the ESD damage may be detected and resolved early in the manufacturing stage (Omazaki, 2023).

ESD sources shown in Figure 11 shows the sources of ESD and the charge that is typical to each application. The table also shows the impact of the humidity level in each of the levels and how this effects the ESD in each application. It shows when the humidity levels are low

the static charge is higher. When the humidity is higher the voltage is lower but at this level, for example 1500 Volt it can still be hazardous to components (Omazaki, 2023).

Source	10 – 20 % humidity	65 - 90 % humidity
Walking on carpet	35,000 Volt	1,500 Volt
Walking on plastic base	12,000 Volt	250 Volt
Working at work table	6,000 Volt	100 Volt
Vinyl covers	7,000 Volt	600 Volt
Plastic bag (picked up from work table)	20,000 Volt	1,200 Volt
Work chair with foam cushion	18,000 Volt	1,500 Volt

Figure 11 - ESD Sources (Omazaki, 2023).

2.3.2 Prevention methods of ESD in electronic design and manufacturing

Method being adopted is ruggedise the electronic components. Many manufacturers in the electronic industry have invested greatly in this method as this way the components are more resistant to potential damage from wayward electrostatic shocks. This method does have a downside as most electronic components are made from a variety of manufacturers, the ability of the resistance to ESD would be only strong as the weakest component in the circuit (Formaspace, 2021).

The other method of prevention can be to establish an ESD-safe working zone. The formal name in industry is the Electrostatic Protection Area (EPA). The first procedure of this is to make sure every workstation item is grounded (Figure 12) (Formaspace, 2021).

ESD WORK SURFACE	ESD SHELVING	ESD CASTERS	ESD CHAIRS	ESD MATS
→ High Pressure Laminate (HPL), Dual Layer HPL or ESD Powder Coated Steel for continuous monitoring → Impact and wear resistant → Resistant to light spills → Eliminates need for ESD surface mats → Meets ANSI/ESDA standards → Built to your required level of ESD compliance	→ HPL, Dual Layer HPL or ESD Powder Coated Steel → Heat and chemical resistant → Impact and wear resistant → Eliminates the need for ESD surface mats → Used on upper and lower shelves → Wire shelving and storage components available	→ Used for dissipation on mobile units → Floor protective anti-static wheels → Allows electricity to flow through bench → Use on carts, mobile benches, and ESD chairs → Rejects floor debris → Resistant to chemicals, water, and steam	→ Reduces static charge from sitting → Discharges through floor grounds → Ergonomic features increase productivity and reduce fatigue → Meets ANSI/ESDA standards → Composed of ESD polyurethane, ESD fabric or ESD vinyl	→ Best for occasional ESD applications → Conductive and static dissipative matting used for surface and floor dissipation → Floor mats reduce workers fatigue and provide comfort → Protects valuable components → Moderate chemical and moisture resistance

Figure 12 - ESD Solutions

ESD wrist straps are used for the first line of ESD defence to be used and is the most common grounding device used. Wrist straps help distribute static electricity generated from a person to a safe ground. For the wrist strap to work, it either must be connected to earth bonding points on a workstation, or it comes with a removable coiled cord and crocodile clip for mobile working (Bondline, 2021).



Figure 13 - Anti-Static Wrist Strap (Bondline, 2021).

Research on ESD and preventive measures has highlighted significant points supported with evidential facts, and good examples

3. Design of Assignment Requirements

Figure 14 is the circuit design that was built using the ECAD design and it will be applied for testing and analysis.

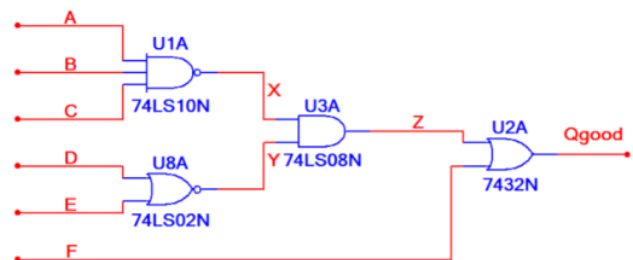


Figure 14 - Circuit Under Test (CUT)

3.1 Stuck at Fault Modelling

From the research the technique of SA fault modelling was used in this section. This was to test the SA faults at zero (SA0) and SA faults at one (SA1). By using the formula, no of tests = $m + 1$ and m is the number of inputs. This is deduced from the number of test vectors.

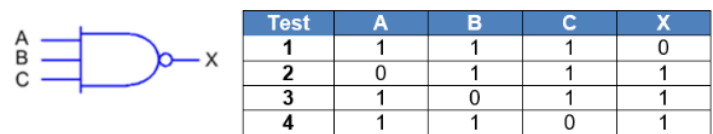


Figure 15 - 3 Input NAND gate - Reduced Test

Figure 15 is showing the 3 input NAND gate at the SA fault model. Showing the 3-inputs, by using the formula the required about of tests will be 4.

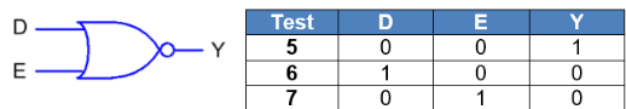


Figure 16 - 2 Input NOR gate - Reduced Test

Figure 16 is showing the reduced table of tests for the 2 input NOR gate.

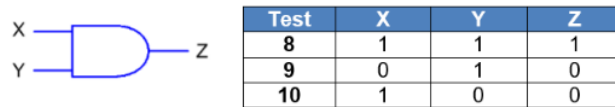
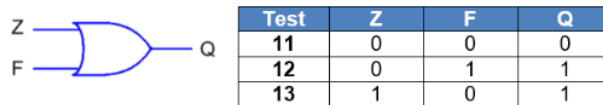


Figure 17 - 2 Input AND gate - Reduced Test

Figure 17 is showing the reduced table of tests for the 2 input AND gate.



Good coverage of reduction methods

Figure 18 - 2 Input OR gate - Reduced Test

Figure 18 is showing the reduced table of tests for the 2 input OR gate.

3.2 Test Vector Test Pattern Tables

Test	A	B	C	D	E	F	Q Good	HEX	X	Y	Z	Fault
①	1	1	1	0	0	0	0	70	0	1	0	A+B+C SA0
2	0	1	1	0	0	0	1	31	1	1	1	A SA1
3	1	0	1	0	0	0	1	51	1	1	1	B SA1
4	1	1	0	0	0	0	1	61	1	1	1	C SA1
⑤	0*	0*	0*	0	0	0	1	01	1	1	1	D+E SA1
6	0*	0*	0*	1	0	0	0	08	1	0	0	D SA0
7	0*	0*	0*	0	1	0	0	04	1	0	0	E SA0
⑧	0*	0*	0*	0	0	0	1	01	1	1	1	X+Y SA0
⑨	1	1	1	0	0	0	0	70	0	1	0	X SA1
10	0*	0*	0*	1**	1**	0	0	0C	1	0	0	Y SA1
11	1	1	1	1**	1**	0	0	7C	0*	0*	0	F+Z SA1
12	1	1	1	1**	1**	1	1	7F	0*	0*	0	F SA0
⑬	0*	0*	0*	0	0	0	1	01	1	1	1	Z SA0

Table 1 - Derived Table for Possible Faults

Table 1 is all the possible stuck faults test and what result is expected at the end of each test stage.

The (*) is highlighted to show that the condition must be at logic 0.

The (**) is highlighted to show that the condition must be at logic 1.

*This is not accurately explained. The * indicates that only one of the values in the row marked with a single * needs to be at logic 0. The double ** indicates only one value needs to be at logic 1.*

The each of the tests with highlights indicate that duplication with tests and this causes redundancies. From this only one are needed from tests 1, 5, 8, 9 and 13. The table will now be reduced.

Test	A	B	C	D	E	F	Q Good	HEX	X	Y	Z	Fault
1	1	1	1	0	0	0	0	70	0	1	0	A+B+C SA0, X SA1
2	0	1	1	0	0	0	1	31	1	1	1	A SA1
3	1	0	1	0	0	0	1	51	1	1	1	B SA1
4	1	1	0	0	0	0	1	61	1	1	1	C SA1
5	0*	0*	0*	0	0	0	1	01	1	1	1	D+E SA1, X+Y SA0, Z SA0
6	0*	0*	0*	1	0	0	0	08	1	0	0	D SA0
7	0*	0*	0*	0	1	0	0	04	1	0	0	E SA0
10	0*	0*	0*	1**	1**	0	0	0C	1	0	0	Y SA1
11	1	1	1	1**	1**	0	0	7C	0*	0*	0	F+Z SA1
12	1	1	1	1**	1**	1	1	7F	0*	0*	0	F SA0

Table 2 - Reduced Table

Table 2 is showing the result from the redundant tests have been removed. Test 8, 9 and 13 have now been removed. By using the (*) wildcards test 5 can be changed to become the same as test 4. This now creates a redundant test vector and was withdrawn through the equivalence rule.

Test	A	B	C	D	E	F	Q Good	HEX	X	Y	Z	Fault
1	1	1	1	0	0	0	0	70	0	1	0	A+B+C SA0, X SA1
2	0	1	1	0	0	0	1	31	1	1	1	A SA1
3	1	0	1	0	0	0	1	51	1	1	1	B SA1
4	1	1	0	0	0	0	1	61	1	1	1	C SA1, D+E SA1, X+Y SA0, Z SA0
6	0*	0*	0*	1	0	0	0	08	1	0	0	D SA0, Y SA1
7	0*	0*	0*	0	1	0	0	04	1	0	0	E SA0
11	1	1	1	1**	1**	0	0	7C	0*	0*	0	F+Z SA1
12	1	1	1	1**	1**	1	1	7F	0*	0*	0	F SA0

Table 3 - Reduced table from the Wildcard Rule

This rule was again applied to test 6 and 10 making the tests redundant. Table 3 results are now showing that the table now consists of 8 vectors instead of the 13 original vectors. It is a common theme that the fault condition of the redundant test vector conditions and this is then added to existing test vectors.

Elimination of redundant tests has been explained, however, some explanations should be more accurate.

3.3 Multisim Design Test using the Word Generator

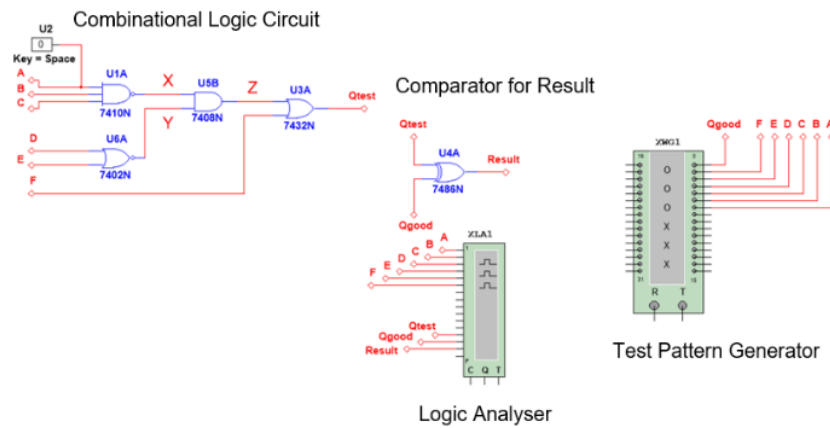


Figure 19 - Word Generator using Multisim

Figure 19 shows the CUT ATE using the method of the word generator to test the sequence through the required inputs. The test condition displayed (Figure 19) shows the no fault element for the CUT.

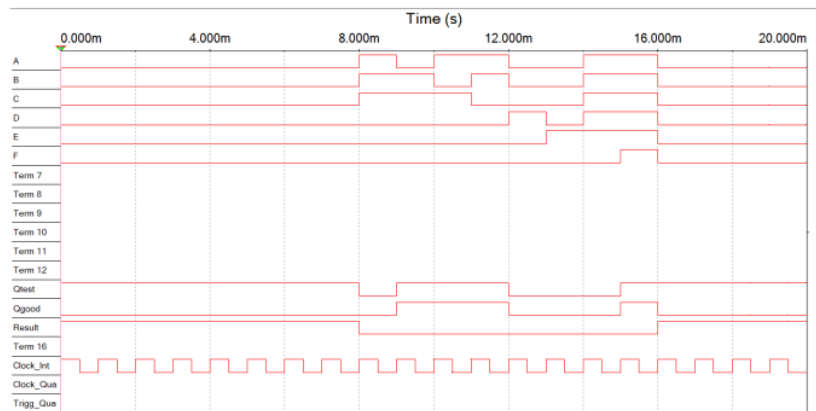


Figure 20 - Word Generator Result - No fault

Figure 20 shows the no fault condition from the word generator test. Shown between 8m and 16m is the result of the waveform. This CUT is a no fault as there are no positive pulses on the output. If a fault is detected a positive pulse will occur.

Good understanding demonstrated

3.4 Multisim Design Test of the 6-Bit Register

The 6-bit register was part of the ATE design as alternative. This was designed and implemented for the same fault scenarios as the logic analyser. These will also be tested and analysed to draw conclusions about this method.

PRESENT STATE						NEXT STATE					
A	B	C	D	E	F	A+	B+	C+	D+	E+	F+
1	1	1	0	0	0	0	1	1	0	0	0
0	1	1	0	0	0	1	0	1	0	0	0
1	0	1	0	0	0	1	1	0	0	0	0
1	1	0	0	0	0	0	0	0	1	0	0
0	0	0	1	0	0	0	0	0	0	1	0
0	0	0	0	1	0	1	1	1	1	1	0
1	1	1	1	1	0	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	0	0	0

Table 4 - State Table

Table 4 is the table that is required for the next step in the designing of the finite state machine. This is the next state table and by completing this the test vectors for inputs A to F can be produced.

From this the Karnaugh maps can be produced, and this will produce the logic states that is a condition needed for the feedback combinational logic and this creates the input sequence.

A B C	000	001	011	010	100	101	111	110
D E F								
000	0	0	(1)	0	0	(1)	0	0
001	0	0	0	0	0	0	0	0
011	0	0	0	0	0	0	0	0
010	(1)	0	0	0	0	0	0	0
100	0	0	0	0	0	0	0	0
101	0	0	0	0	0	0	0	0
111	0	0	0	0	0	0	(1)	0
110	0	0	0	0	0	0	(1)	0

Table 5 - Karnaugh Map for Output QA

Table 5 is showing the Karnaugh map produced for the register QA output.

The expression in Boolean form for this Karnaugh map:

$$A.B.C.D.E + A.NB.C.ND.NE.NF + NA.B.C.ND.NE.NF + NA.NB.NC.ND.E.NF$$

A B C D E F	000	001	011	010	100	101	111	110
000	0	0	0	0	0	1	1	0
001	0	0	0	0	0	0	0	0
011	0	0	0	0	0	0	0	0
010	1	0	0	0	0	0	0	0
100	0	0	0	0	0	0	0	0
101	0	0	0	0	0	0	0	0
111	0	0	0	0	0	0	1	0
110	0	0	0	0	0	0	1	0

Table 6 - Karnaugh Map for Output QB

Table 6 is showing the Karnaugh map produced for the register QB output.

The expression in Boolean form for this Karnaugh map:

$$A.C.ND.NE.NF + A.B.C.D.E + NA.NB.NC.ND.E.NF$$

A B C D E F	000	001	011	010	100	101	111	110
000	0	0	1	0	0	0	1	0
001	0	0	0	0	0	0	0	0
011	0	0	0	0	0	0	0	0
010	1	0	0	0	0	0	0	0
100	0	0	0	0	0	0	0	0
101	0	0	0	0	0	0	0	0
111	0	0	0	0	0	0	1	0
110	0	0	0	0	0	0	1	0

Table 7 - Karnaugh Map for Output QC

Table 7 is showing the Karnaugh map produced for the register QC output.

The expression in Boolean form for this Karnaugh map:

$$NA.NB.NC.ND.E.NF + NA.B.C.ND.NE.NF + A.B.C.ND.NE.NF + A.B.C.D.E$$

A B C D E F	000	001	011	010	100	101	111	110
000	0	0	0	0	0	0	0	1
001	0	0	0	0	0	0	0	0
011	0	0	0	0	0	0	0	0
010	1	0	0	0	0	0	0	0
100	0	0	0	0	0	0	0	0
101	0	0	0	0	0	0	0	0
111	0	0	0	0	0	0	0	0
110	0	0	0	0	0	0	1	0

Table 8 - Karnaugh Map for Output QD

Table 8 is showing the Karnaugh map produced for the register QD output.

The expression in Boolean form for this Karnaugh map:

$$NA.NB.NC.ND.E.NF + A.B.NC.ND.NE.NF + A.B.C.D.E.NF$$

A B C D E F	000	001	011	010	100	101	111	110
000	0	0	0	0	0	0	0	0
001	0	0	0	0	0	0	0	0
011	0	0	0	0	0	0	0	0
010	①	0	0	0	0	0	0	0
100	①	0	0	0	0	0	0	0
101	0	0	0	0	0	0	0	0
111	0	0	0	0	0	0	0	0
110	0	0	0	0	0	0	①	0

Table 9 - Karnaugh Map for Output QE

Table 9 is showing the Karnaugh map produced for the register QE output.

The expression in Boolean form for this Karnaugh map:

$$NA.NB.NC.ND.E.NF + NA.NB.NC.D.NE.NF + A.B.C.D.E.NF$$

A B C D E F	000	001	011	010	100	101	111	110
000	0	0	0	0	0	0	0	0
001	0	0	0	0	0	0	0	0
011	0	0	0	0	0	0	0	0
010	0	0	0	0	0	0	0	0
100	0	0	0	0	0	0	0	0
101	0	0	0	0	0	0	0	0
111	0	0	0	0	0	0	0	0
110	0	0	0	0	0	0	①	0

Table 10 - Karnaugh Map for Output QF

Table 10 is showing the Karnaugh map produced for the register QE output.

The expression in Boolean form for this Karnaugh map:

$$A.B.C.D.E.NF$$

From the next state logic (Table 4) the results from this process created the design shown in Figure 21. The Boolean expressions results are shown in the form of the feedback circuits, and this is to minimise the combinational circuit. This can now be tested with a no-fault condition. Shown in the CUT, a comparison of output is used to prove that an identical circuit output is working. By using an X OR Gate this can differentiate a variety of outputs of the CUT to the proven circuit that is correct.

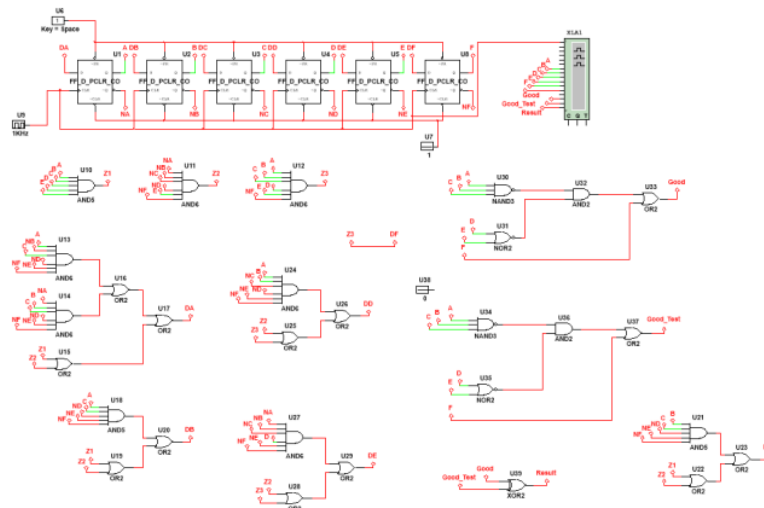


Figure 21 - 6-Bit Register Design

This PRPG (6-bit register) was tested under the no fault condition (Figure 22). As both outputs have the same result from the CUT this is proven to be an acceptable circuit. The flat line on the Result pulse shows the X OR gate and no pulses are generated shows no difference on the output.

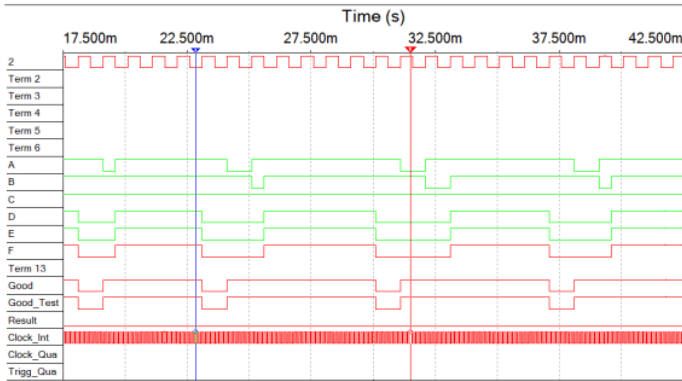


Figure 22 - 6-Bit Register Result – No fault

Explanation indicates a very good understanding of requirements

4. Analysis of NI MultiSim results

4.1 Multisim Results of the Word Generator

The design circuit was modified to produce different fault conditions, these were all from the test vectors produced from the tables. The fault conditions are confirmed by simulations as they generate the CUT inputs data sequence.

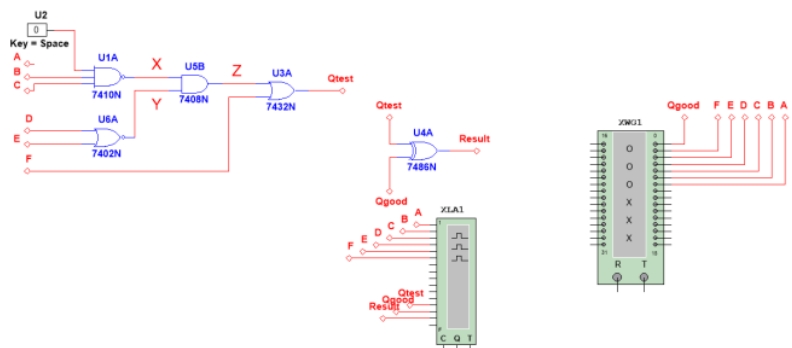


Figure 23 - A SA at 0 (Logic Analyser)

Figure 23 is showing the result from A SA at 0, this was derived from the table of test vectors.

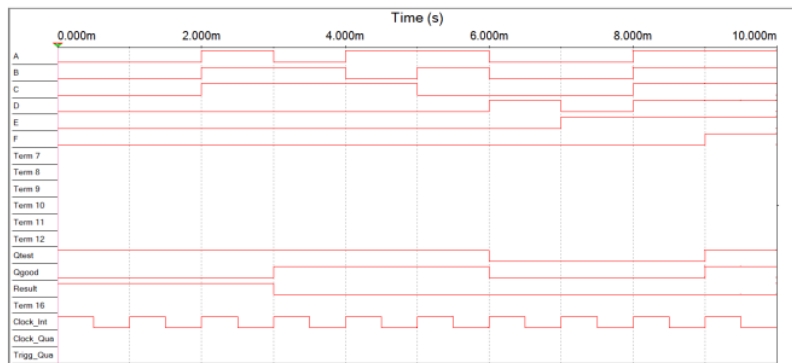


Figure 24 - Test Result for A SA at 0 (Logic Analyser)

Figure 24 is showing the result of logic analyser from A SA at 0 test. When comparing with no fault, this result has a rising positive pulse on the output this indicates a fault condition.

The test results (Figure 25 and Figure 26) shows the CUT and the resultant output from the logic analyser are at logic 1 when the B input is held at logic 0. The result is shown between the 8m and 16m.

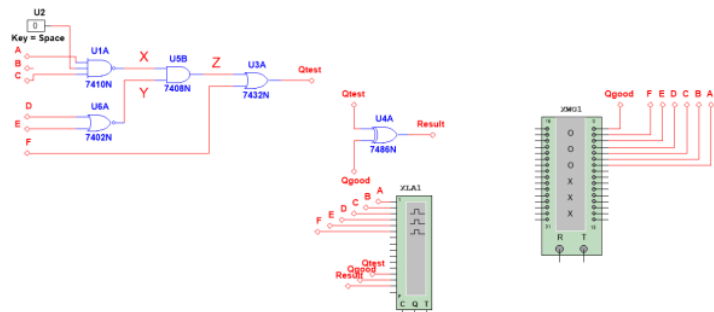


Figure 25 - B SA at Zero (Logic Analyser)

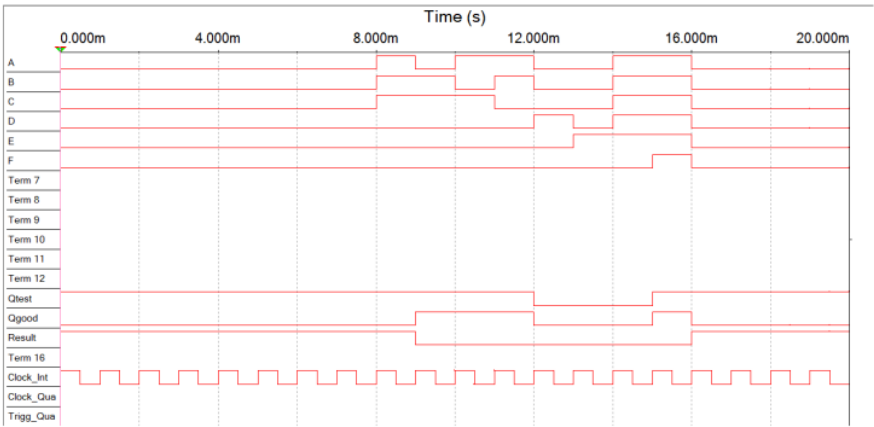


Figure 26 - Test Result for B SA at 0 (Logic Analyser)

Figure 27 and Figure 28 are showing the change in CUT to accommodate for the E SA at 0 fault condition. As the resultant output from the logic analyser is stuck at 1 and the logic input of E held at zero this becomes a fault. The evidence is shown with a positive pulse between 8m and 16m (Figure 28).

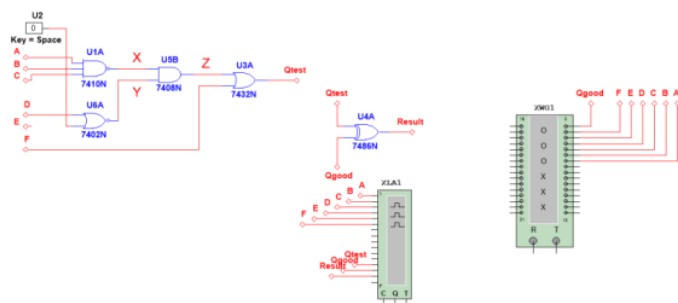


Figure 27 - E SA at Zero (Logic Analyser)

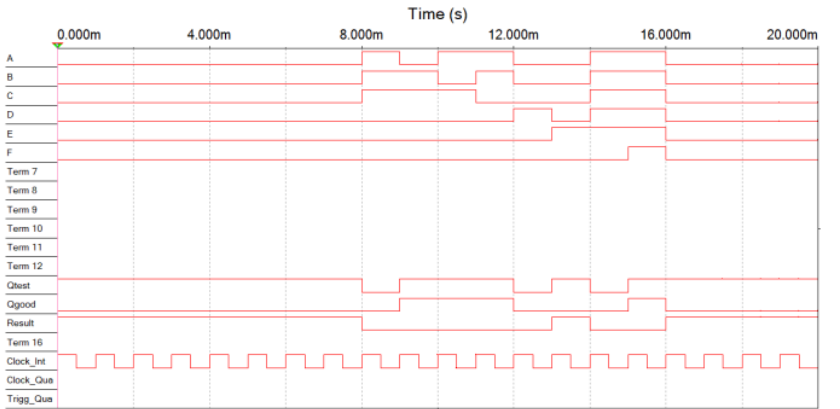


Figure 28 - Test Result for E SA at 0 (Logic Analyser)

Good application examples given with correct results. The presentation could have been improved with annotated fault conditions.

4.2 Multisim Results of the 6-Bit Register

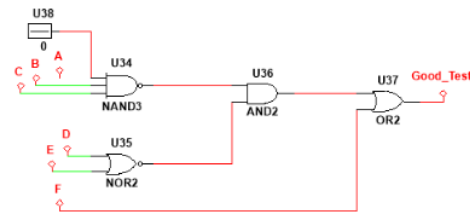
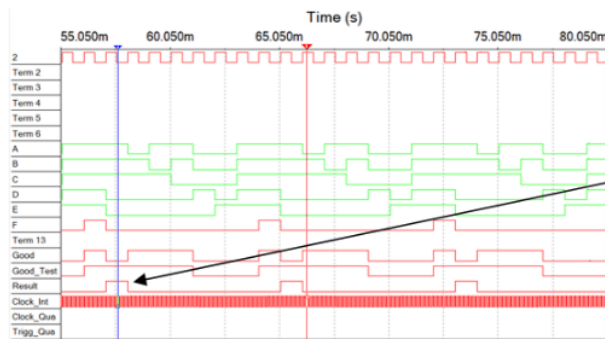


Figure 29 - 6-Bit CUT - A SA0

Figure 29 is showing the circuit that is adapted to have the logic 0 stuck on throughout the testing of the 6-bit register.



Good explanation with correct result

Figure 30 - 6-Bit Result - A SA0

Figure 30 showing the results from the fault condition A SA0. As the blue cursor shows a pulse in the result this shows that a fault condition is present.

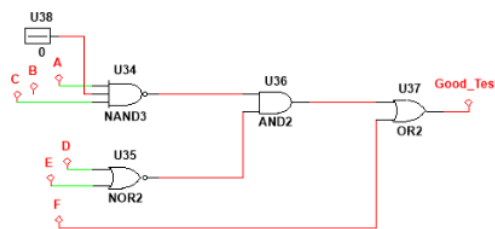


Figure 31 - 6-Bit CUT - B SA0

Figure 31 is showing the same test but completed with input B at the fault condition SA0.

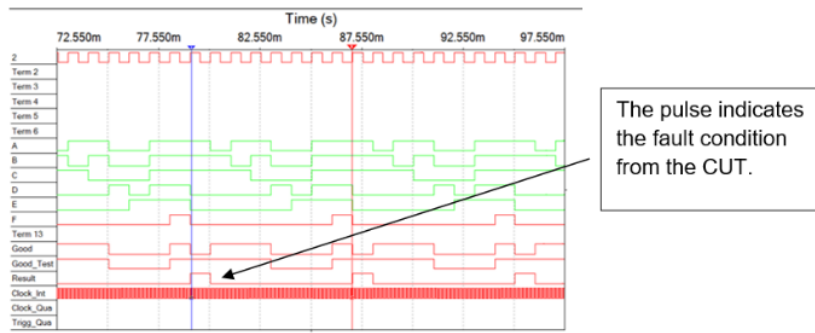


Figure 32 - 6-Bit Result - B SA0

Figure 32 is the B SA0 fault condition and this shows a pulse in the result meaning a fault is present.

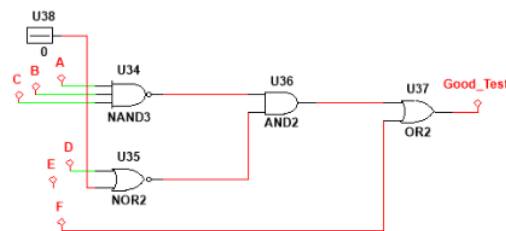


Figure 33 - 6-Bit CUT - E SA0

Figure 33 is the last CUT this was the fault condition E SA0.

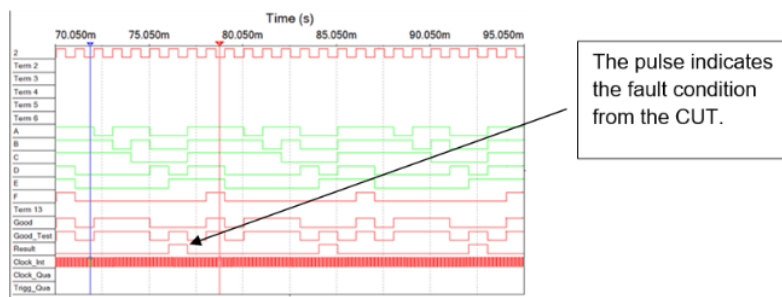


Figure 34 - 6-Bit Result - E SA0

Figure 34 is the result from the last test which was the fault condition E SA0. The pulse in the result shows that a fault is present.

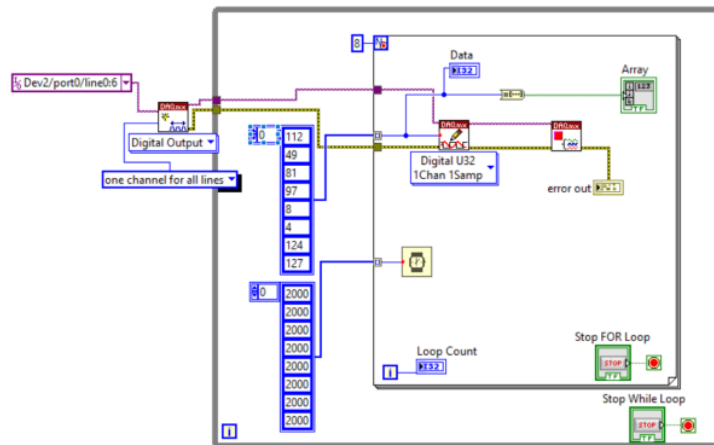
These tests from the 6-Bit register shows that when a fault is applied to the CUT a pulse will occur on the result line.

Good explanations of reslts obtained with application examples

5. Practical build and test using LabView

5.1 LabView Program build

This section of the report will show the development of a LabView program that will provide the interface for the DAQmx development board. The LabView program provides the link to a physical circuit using the G code program and will provide the data stream to drive the inputs. The instrumentation of LabView can allow the physical circuit to be run from it virtually.



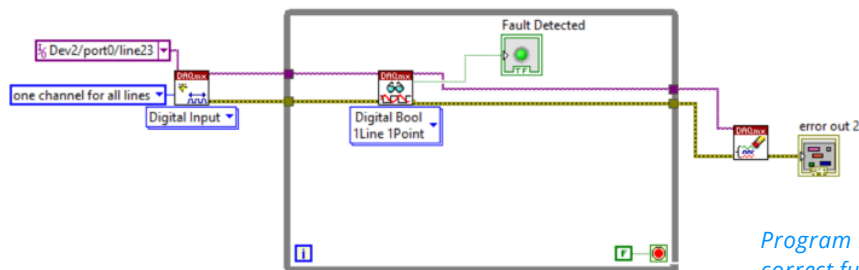
Good explanation of concept

Good layout pf program

Figure 35 - Block Diagram of the LabView Program

Figure 35 was developed for driving inputs that were applied to the DAQmx board, this is through the DAQmx instrument channel I/O controller. The 'while' loop was produced in the program to run for infinite amount of time, and this can also be stopped manually. The 'for' loop was implemented as it runs for eight iterations for each of the eight test vectors. The sample rate is produced by the time delay.

Good explanation

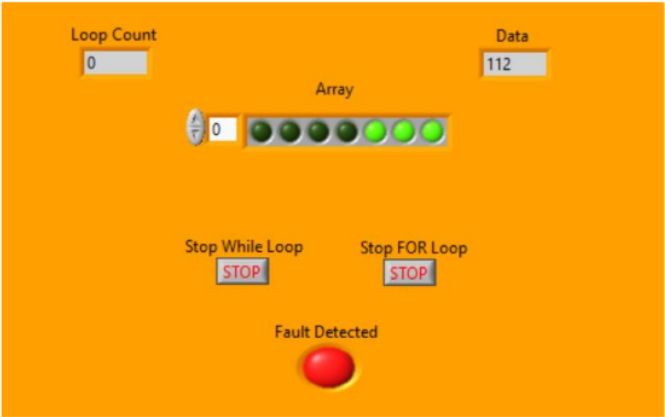


Program layout is good with correct functions included

Figure 36 - Second Block of the LabView Program

Figure 36 was the second block to allow the output which is line 23 in block diagram from the X-OR gate located on the DAQmx and provides the display of a logical condition.

This is a critical part of the system that is explained and understood



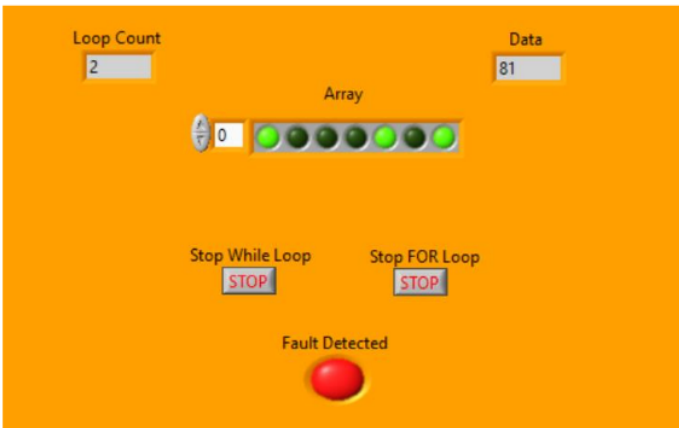
Good layout of front panel

Figure 37 – LabView Program - Front Panel

Figure 37 is the front panel that was developed to produce the fault detections from the circuit under test (CUT). The fault detection comes from the output of the X-OR gate. The inputs on the array run from left to right, the left is MSB, and the right is LSB. From the fault model reduction tables, the results are shown through binary data. The 'for loop' iteration on the front panel is shown on the data display.

Program functions are explained and understood

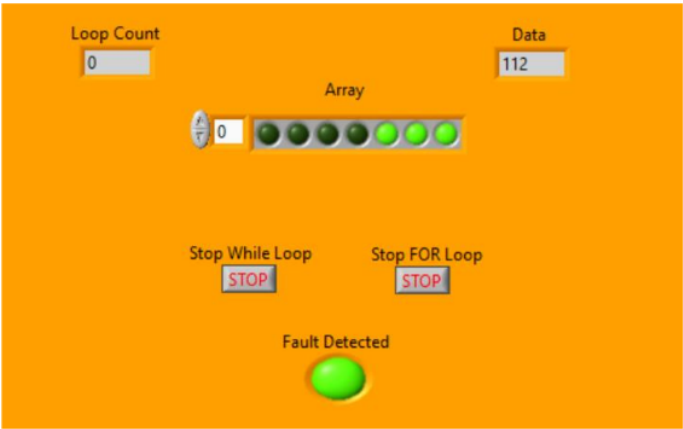
5.2 LabView Program Test with DAQmx



NFF condition is indicated

Figure 38 - LabView Program - No Fault

Figure 38 is showing the no fault condition on the front panel as the LED is not showing green. The DAQmx board with this condition is shown in (Figure 47, Appendix 2A) as no LED is illuminated no fault is detected.



Fault indication is demonstrated with reference to DAQ board with CUT in appendix

Figure 39 - LabView Program - A SA0

Figure 39 is the result from the A SA0, the fault has been detected as the LED has turned green. The result from the development board is shown in Figure 48, Appendix 2A.

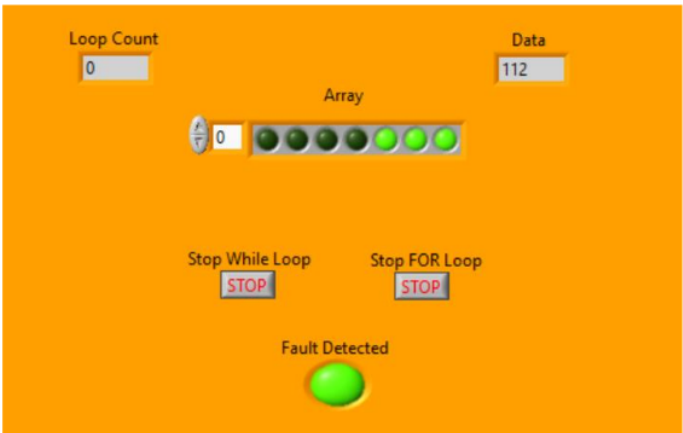
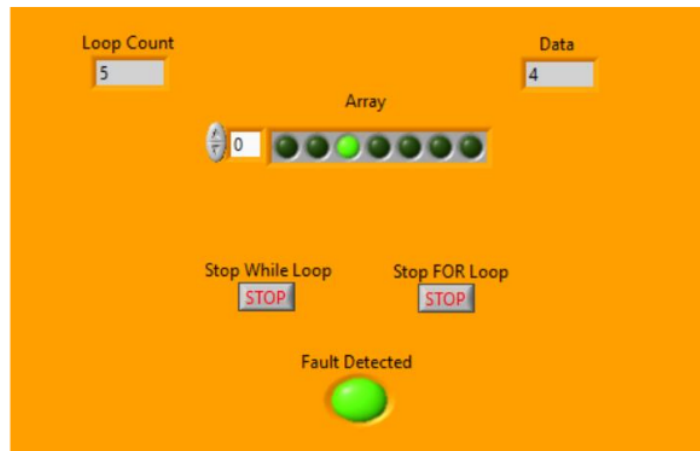


Figure 40 - LabView Program - B SA0

Figure 40 is showing the result of the B SA0 fault condition. The green LED had come one showing the fault. The DAQmx result is shown in Figure 49, Appendix 2A.



3 fault conditions have been tested and explained with ref to DAQ board setup in appendix

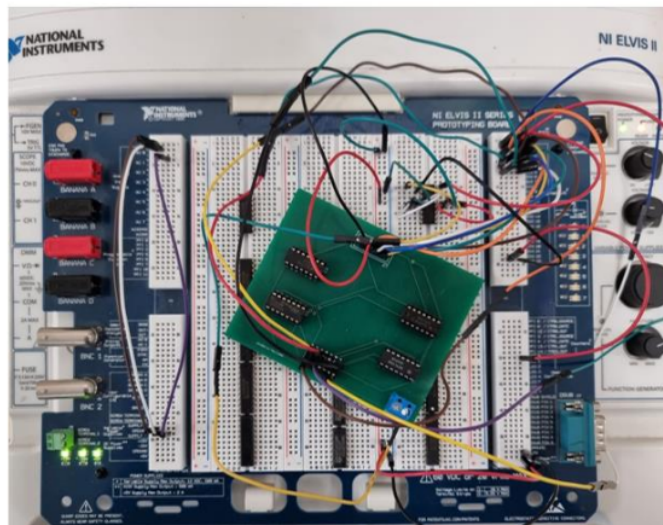
Figure 41 - LabView - E SA0

Figure 41 is showing the fault E SA0 and the green LED is illuminated a known fault is present. The DAQmx result is shown in Figure 50, Appendix 2A.

5.3 LabView Program with the Implementation of the CAM Circuit

Shown in Figure 42 is where the PCB has been implemented onto the DAQmx board. This is where no fault condition is present, this shows that the board is functioning correctly and now each of the fault conditions were tested shown in Appendix 2B and all had the same outcome as expected.

Grammar needs to be checked here!



Good explanation and image of test setup with NFF condition

Figure 42 - CAM Circuit - No Fault Condition

6.2 Geber files for the Printed Circuit Board

Figure 58, Appendix 2C is showing the top solder mask. The file is responsible for showing the system of the location of the solder resin layers onto the copper traces on the printed board. By applying this unintended solder bridges are prevented.

Figure 59, Appendix 2C is showing the bottom of the solder mask. The file oversees over seeing where the silicone needs to be placed onto the solder connections for each of the components. This is to stop unintended solder bridges from happening.

Figure 60 and Figure 61 in Appendix 2C are showing the top and bottom of the copper file. These two files show the path for where the copper runs.

Figure 62, Appendix 2C is the silkscreen, and this file identifies where each of the component should be positioned on the board.

Figure 63, Appendix 2C is the final manufacturing design. This design was sent out to be manufactured by an external company.

[Good explanation of Gerber file functions](#)

7. Conclusions and Recommendations

To conclude the report, the research was proven to provide a background knowledge into the stuck at fault modelling technique which in turn was implemented into the further design processes in the report. The learning from this was that which result was expected from each possible fault. The different manufacturing techniques and the wider engineering needs were explored. From this modern industry 4.0 techniques will be incorporated in more manufacturing processes in the future especially with vision systems in mind. When designing CUT, it was apparent that the 6-input combinational circuit met the requirements regarding the design. By successfully implementing the stuck at fault model and this in turn was used as a reduction method for the test vectors. During the following stage, the circuits had three different faults applied through the resultant test vector tables, which would show a better comparison between each of the circuits. It was found that applying the fault conditions, an output result was found through the X-OR gate and used for comparison. The word generator was the first to be developed, and this was successfully tested as the no fault condition showed a zero pulse. The three faults were applied and when the positive pulse occurs the fault is present on the CUT. The 6-bit register was the next the circuit design to be tested using the ATE design implementation. The same conditions were applied to this and making comparisons with the word generator the same outcome occurred. The penultimate test was to design the LabView program and implement onto the DAQmx development board. This was to drive 6 inputs of the CUT and carry out the same test procedure. The same conditions were applied, the no fault condition first to see if the CUT was successfully working. The identical three faults were again applied to CUT, all three gave the correct fault indications on the panel view. When comparing with theory this result shows the expected outcome occurred. The benefit of using LabView is that the G code is easily implemented, and the software provides a graphical user interface (GUI) for the real time process. The last section of the report was to produce a manufactured CAM design using the Eagle software, the Gerber files were sent to a manufacturer to be produced. The PCB was implemented onto the DAQmx board and was successfully tested using the same fault conditions. The overall performance of the test methods is quite good however, considerations should be taken, for example, the bed nails technique. The initial outlay is quite costly however, from a cost driver perspective it would be suited in the long run as it would pick up on a considerable amount of faults.

The conclusion demonstrates a good understanding of the procedures carried out to satisfy requirements.

8. Citation List

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[Accessed 30 January 2022].

A very good range of sources investigated for research requirements

9. Appendix

9.1 Appendix 1A

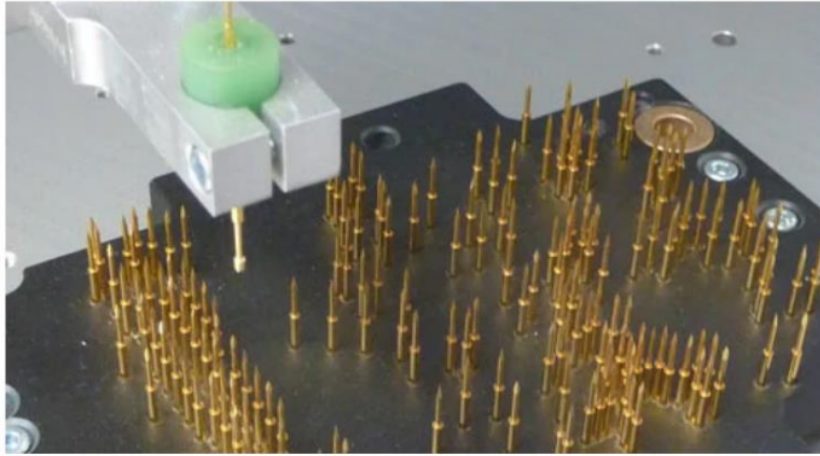


Figure 45 - Test fixture for Bed-of-Nails test (Proto-electronics, 2023).

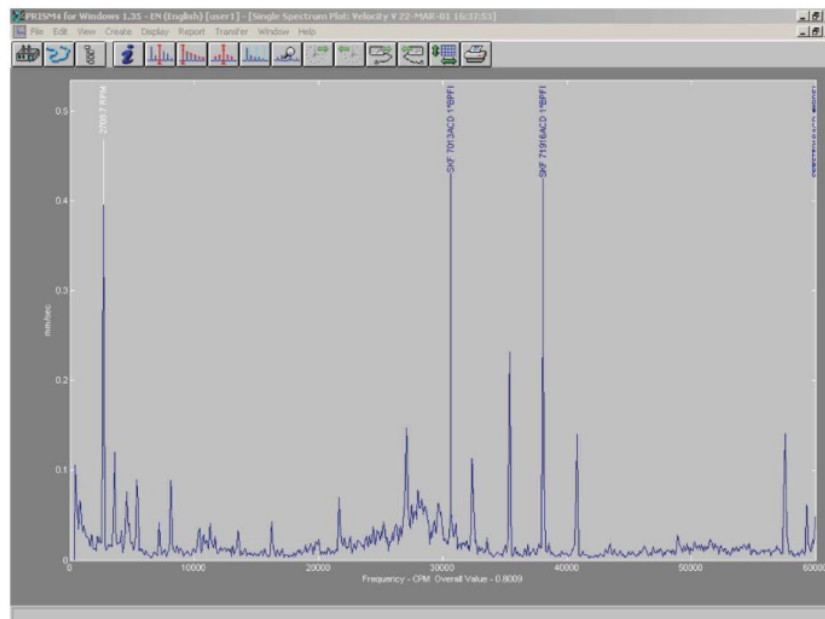


Figure 46 - Velocity Spectrum (Mais, 2002).

9.2 Appendix 2A

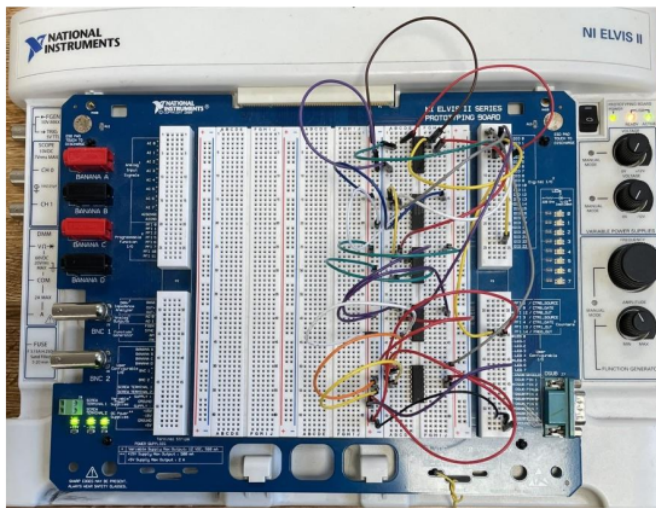


Figure 47 - DAQmx at No Fault Condition

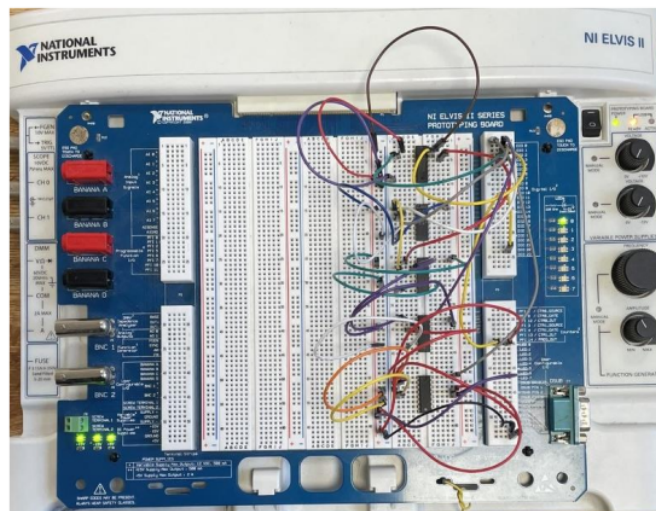


Figure 48 - DAQmx - A SA0

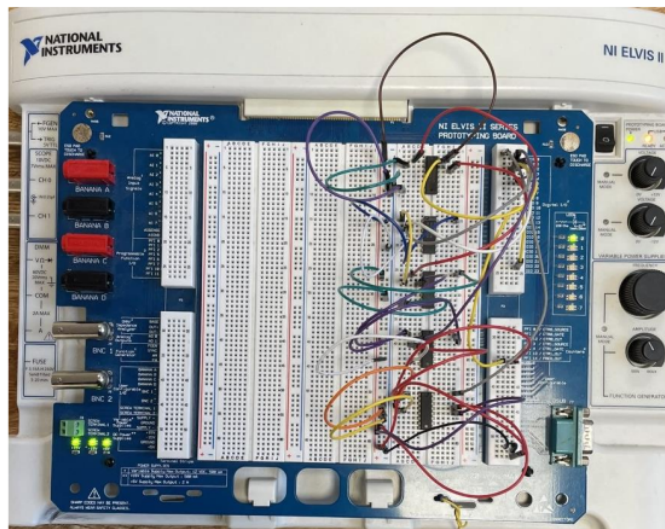


Figure 49 - DAQmx - B SA0

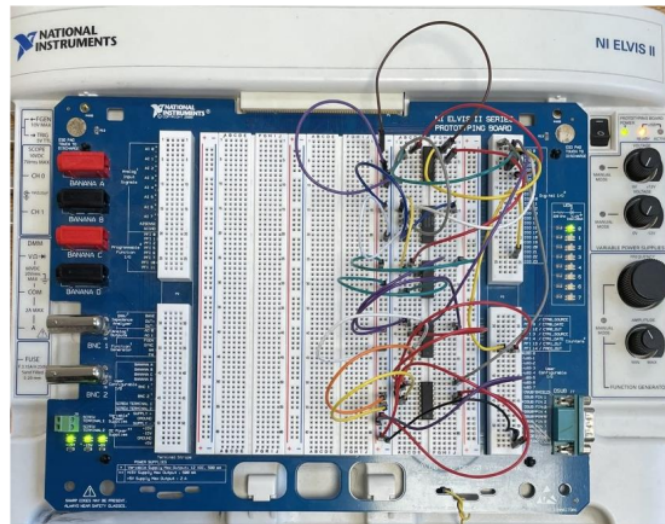


Figure 50 - DAQmx - E SA0

9.3 Appendix 2B

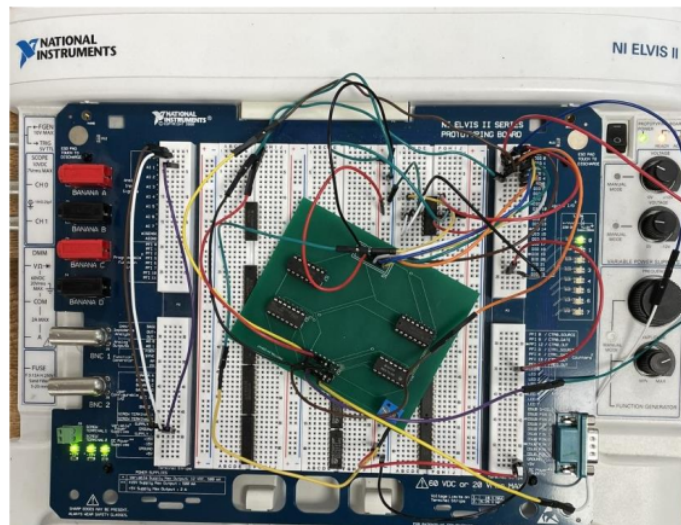


Figure 51 - CAM Circuit - A SA0

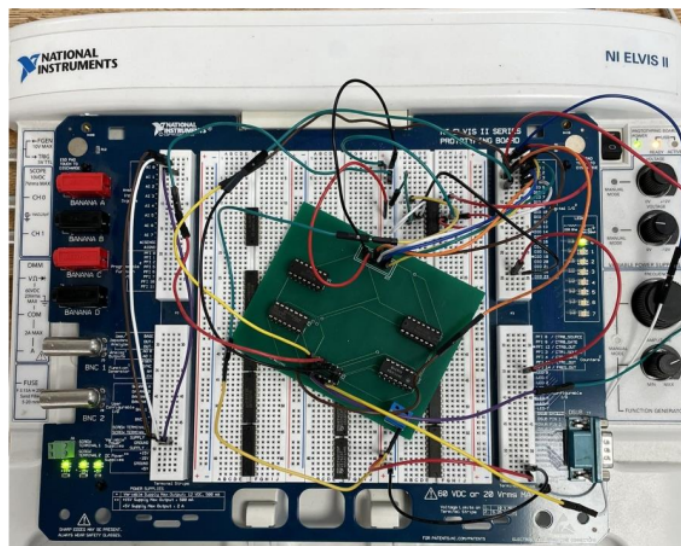


Figure 52 - CAM Circuit - B SA0

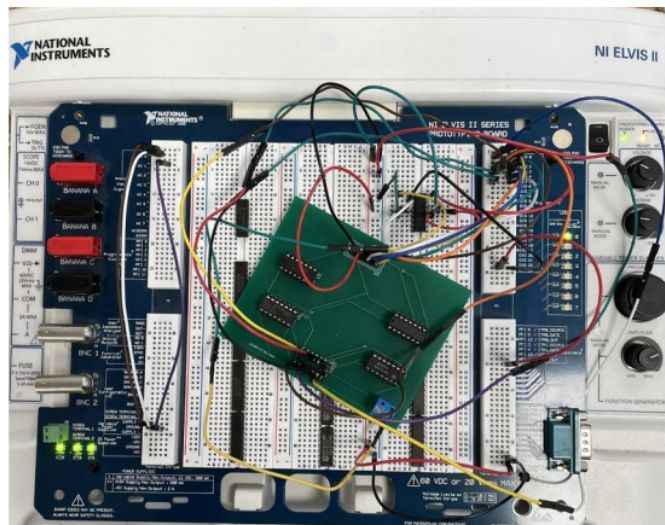


Figure 53 - CAM Circuit - E SA0



Figure 54 - LabView CAM Circuit - A SA0

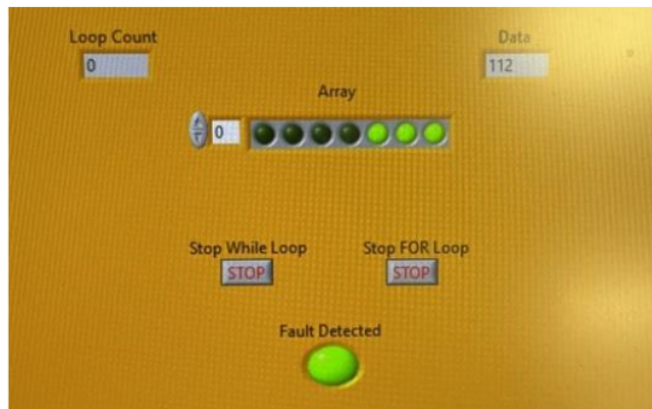


Figure 55 - LabView CAM Circuit - B SA0



Figure 56 - LabView CAM Circuit - E SA0

9.4 Appendix 2C

CAMOutputs > GerberFiles		Search GerberFiles	
Name	Type	Compressed size	Pass
copper_bottom.gbr	GBR File	2 KB	No
copper_top.gbr	GBR File	2 KB	No
gerber_job.gbrjob	GBRJOB File	1 KB	No
profile.gbr	GBR File	1 KB	No
silkscreen_bottom.gbr	GBR File	1 KB	No
silkscreen_top.gbr	GBR File	10 KB	No
soldermask_bottom.gbr	GBR File	1 KB	No
soldermask_top.gbr	GBR File	1 KB	No
solderpaste_bottom.gbr	GBR File	1 KB	No
solderpaste_top.gbr	GBR File	1 KB	No

Figure 57 - Content of the Gerber Files

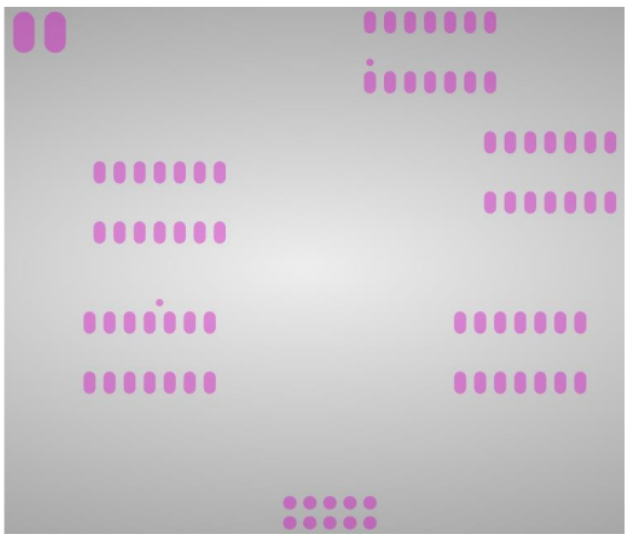


Figure 58 - Solder Mask (Top)

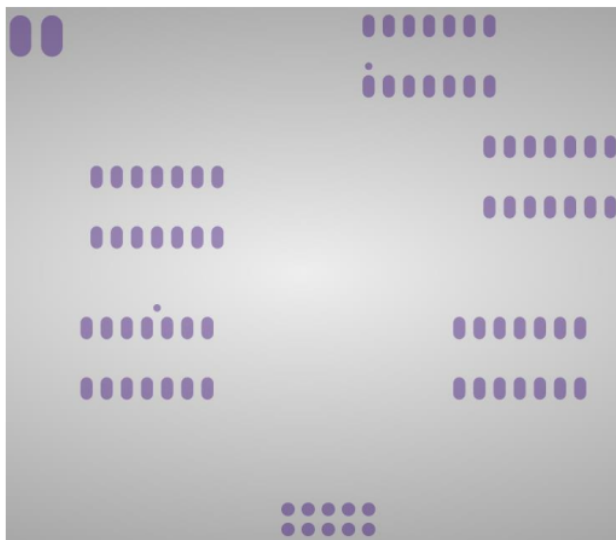


Figure 59 - Solder Mask (Bottom)

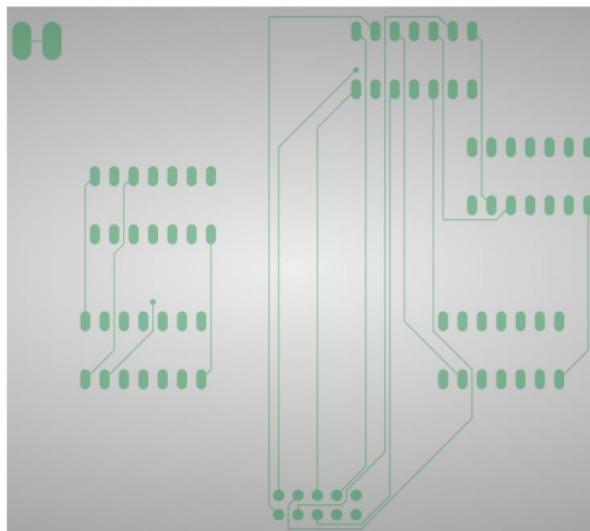


Figure 60 - Copper (Top)

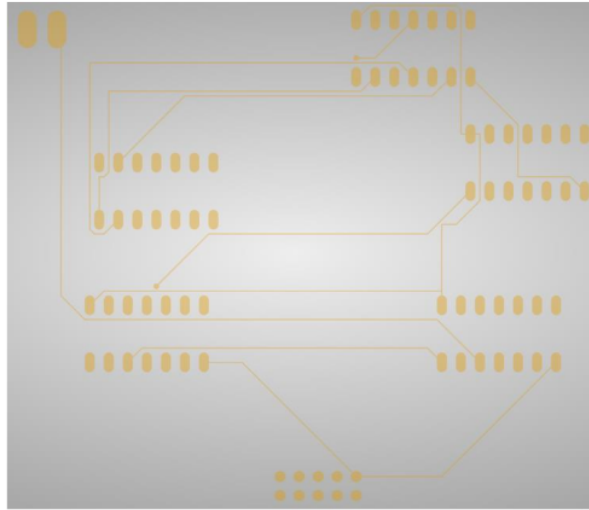


Figure 61 - Copper (Bottom)

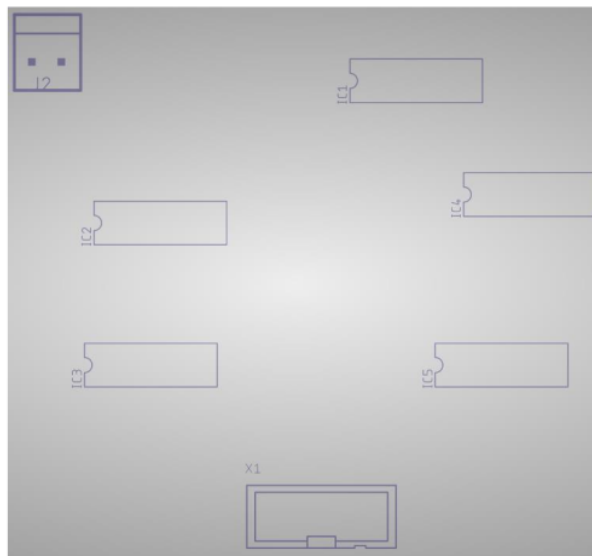


Figure 62 - Silkscreen

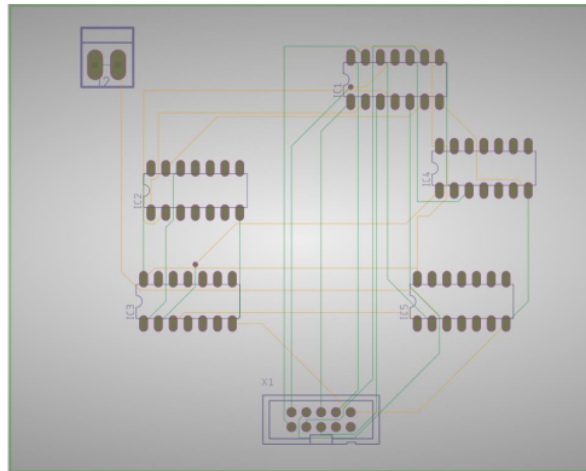


Figure 63 - Manufacturing Design with all files

Very good use of appendices for relevant supporting images

1451789

GRADEMARK REPORT

FINAL GRADE

GENERAL COMMENTS

Instructor

78/100

PAGE 1

PAGE 2

PAGE 3

Text Comment. Very good detailed table of contents

PAGE 4

PAGE 5

Text Comment. Good comprehensive tabe of figures

PAGE 6

Text Comment. This summary demonstartes an extensive understanding of the requirements.

PAGE 7

PAGE 8

Text Comment. Excellent explanations here with good relevant examples

PAGE 9

PAGE 10

Text Comment. Good application examples used here to support research

Text Comment. This is a good significant finding in the research

Text Comment. These sentences should be cobined into a single sentence

Text Comment. Very good explanantion and relevant supporting image example

Text Comment. Minor grammar error

Text Comment. Good research findings here that underpins a good relevant understanding of the concept, and its use in industry

Text Comment. It is worth explaining that the vision and frequency detwction systems are inclusive of the contactless sensing topic area.

Text Comment. Good explanations with good relevant sources and examples

Text Comment. Research on ESD and preventive measures has highlighted significant points supported with evidential facts, and good examples

Text Comment. Good coverage of reduction methods

Text Comment. This is not accurately explained. The * indicates that only one of the values in the row marked with a single * needs to be at logic 0. The double ** indicates only one value needs to be at logic 1.

Text Comment. Elimination of redundant tests has been explained, however, some explanations should be more accurate.

Text Comment. Good understanding demonstrated

PAGE 20

PAGE 21

PAGE 22

PAGE 23

Text Comment. Explanation indicates a very good understanding of requirements

PAGE 24

Text Comment. Fault condition should be labelled

PAGE 25

PAGE 26

Text Comment. Good application examples given with correct results. The presentation could have been improved with annotated fault conditions.

PAGE 27

Text Comment. Good explanation with correct result

PAGE 28

Text Comment. Good explanations of results obtained with application examples

PAGE 29

Text Comment. Good explanation of concept

Text Comment. Good layout of program

Text Comment. Good explanation

Text Comment. Program layout is good with correct functions included

PAGE 30

Text Comment. This is a critical part of the system that is explained and understood

Text Comment. Good layout of front panel

Text Comment. Program functions are explained and understood

Text Comment. NFF condition is indicated

PAGE 31

Text Comment. Fault indication is demonstrated with reference to DAQ board with CUT in appendix

PAGE 32

Text Comment. 3 fault conditions have been tested and explained with ref to DAQ board setup in appendix

Text Comment. Grammar needs to be checked here!

Text Comment. Good explanation and image of test setup with NFF condition

PAGE 33

Text Comment. CAM design of prototype is good

PAGE 34

Text Comment. Good explanation of Gerber file functions

PAGE 35

Text Comment. The conclusion demonstrates a good understanding of the procedures carried out to satisfy requirements.

PAGE 36

PAGE 37

Text Comment. A very good range of sources investigated for research requirements

PAGE 38

PAGE 39

PAGE 40

Text Comment. Very good use of appendices for relevant supporting images

GRADING FORM: CSG-RUBIC

JOSHUA WILLIAMS

0

RESEARCH-INFORMED LITERATURE



Very good research carried out that covers significant relevant points for the topic area. The sources investigated demonstrates extensive research.

18/20

KNOWLEDGE AND UNDERSTANDING



A very good understanding has been demonstrated in all areas of the requirements and the test vectors have been obtained with explanations. 3.5/5 The LabVIEW design of test vectors indicates a good understanding and high

16/20

level of study in the development stages. 4.5/5 The Msim alternative ATE systems have been designed and developed to a good standard with good use of alternative functions. 4/5 CAM design shows a good understanding of the process requirements from design to manufacture. 4/5

ANALYSIS

 Extensive ECAD testing with good explanations provided. Test results supported with good images. 7/10 Tests carried out are referenced to the test table that follows the theory of SSF modelling. 4/5 Good conclusion and relevant recommendations. 4/5

15/20

PRACTICAL APPLICATION AND DEP.

 Development and test of prototype has been carried out with good detail and explanations. 7/10 Tests carried out with LabVIEW have been explained with good illustrative examples ,and extensive level of detail. 7/10

14/20

SKILLS FOR PROFESSIONAL PRAC.

 Extensive use of relevant software has been demonstrated. 8/10 A very good report layout with all the required content in the correct order. 4/5 Good report, however word count has exceeded. Very good use of appendices. 3/5

15/20