



12 Pages

1. Please give the information requested in the boxes below.
2. Enter your name in the space provided to the right, fold over and seal down (using the label provided) to hide your name.
3. The answers must be legibly written. The Examiners can either ignore illegible script or have it typed and the expense of typing charged to the candidate.
4. Write your answers in ink.
5. Begin each answer on a fresh page. Do all rough work in the answer book and cross it through.
6. No part of this book is to be torn out; it must be handed in complete.
7. If more books than one are used, fasten them together using the tags available from the invigilator(s).
8. **Every book must be handed in. In no circumstances may answer books, used or unused, be taken out of the examination venue.**

1	Student Number	SZW23868203
2	Title of Examination Paper	HNC ELECTRICAL AND ELECTRONIC ENGINEERING*
3	Module Code	GOEE4000
4	Date and Time of Examination	17/5/24 14:00 (PM)
5	Examination Venue	GOWER COLLEGE TYCOCH CAMPUS MAIN HALL CENTRE NO: 68860
6	Seat Number	H4
7	Number of Answer Books handed in	1

* MICROPERIPHERALS AND INTERFACES

SURNAME: SZWEDIUK

FORENAME(S): SAMUEL THOMAS

[illegible]

RK
33/50

$$66 \frac{0}{0}$$

- 1) REGISTER +
- 1.1.1, CONTROL UNIT - CONTAINS ALU + CPU, MAIN COMPONENT
- 1.1.2, INTERRUPTS - STOP/ INTERRUPT AN ~~INSTR~~ INSTRUCTION OR TASK
- 1.1.3, MEMORY HIERARCHY - ALLOWS PRIORITY OF DIFFERENT TYPES OF MEMORY (RAM AND ROM)
- 1.1.4, DMA - DIRECT MEMORY ACCESS ALLOWS THE MEMORY TO CONTROL A TASK WITHOUT THE CPU (CYCLE STEALING)
- 1.1.5, PWM - PULSE WIDTH MODULATION IS A PULSE OF DIGITAL SIGNALS TO GIVE AN AVERAGE OUTPUT.
need further explain.

Q1
11.5/15

- 1.2, HIGH LEVEL PROGRAMMING - PROGRAMMING SOFTWARE SUCH AS C++
ASSEMBLY LANGUAGE - BASIC LANGUAGE JUST ABOVE BINARY
MACHINE LANGUAGE - BINARY LANGUAGE PROGRAMMING
- 1.3, CISC - COMPLEX INSTRUCTION SET COMPUTING, USED IN EMBEDDED SYSTEMS, VARIED INSTRUCTIONS OF DIFFERENT SIZES
RISC - REDUCED INSTRUCTION SET COMPUTING, USED IN PERSONAL COMPUTERS, SIMPLER INSTRUCTIONS OF THE SAME SIZE
- 1.4, STACK - OPERATES ON FIRST IN LAST OUT PRINCIPAL, FIRST INSTRUCTION IN IS THE LAST TO EXECUTE
QUEUE - OPERATES ON FIRST IN FIRST OUT PRINCIPAL, FIRST INSTRUCTION IN IS THE FIRST TO EXECUTE

ACTIVE 'HIGH'			ACTIVE 'LOW' INVERTING		
CONTROL	IN	OUT	CONTROL	IN	OUT
0	1	HI-Z	0	1	0
0	0	HI-Z	0	0	1
1	1	1	1	1	HI-Z
1	0	0	1	0	HI-Z

②

②

- 2)
- 1, ~~ROM~~ SYSTEM MEMORY THAT CANNOT CHANGE ✓ ①
 - 2, EEPROM - READ ONLY MEMORY THAT CAN BE ELECTRONICALLY ERASED AND RE WRITTEN X
 - 3, I/O PORTS - INPUT OR OUTPUT PORTS TO ATTACH EXTERNAL DEVICES ✓ ①
 - 4, VREF - VOLTAGE REFERENCE USED TO COMPARE TO ~~IN~~ INCOMING VOLTAGES, CAN BE SET TO INTERRUPT ✓ ①
 - 5, ~~D~~A/D - ANALOG DIGITAL CONVERTER CONVERTS INCOMING ANALOG SIGNALS INTO DIGITAL ✓ ①
 - 6, OSCILLATOR - PROVIDES A SYSTEM CLOCK ✓ ①
 - 7, SPI - SERIAL PORT INTERFACE, I²C - INTER INTEGRATED SYSTEM. DIFFERENT TYPES OF COMMUNICATION SYSTEMS ①
 - 8, USART - UNIVERSAL SYNCHRONOUS ASYNCHRONOUS REGISTER TIMER ✓ also need further discussion. ①.5
 - 9, CPU - MAIN BRAIN OF SYSTEM WHICH CONTROLS ALL OTHER COMPONENTS ✓ ①
 - 10, WDT - WATCHDOG TIMER MONITORS PROCESSES AND CAN RESET THE SYSTEM IN A FAULT. ✓ ①

Q2

8.5/10

3)

- 3.1, SERIAL I/O $\times$
 PARALLEL I/O $\times$
 MEMORY I/O $\checkmark$
 HARDWARE I/O $\times$
 INTERRUPT $\times$
~~EEPROM~~ I/O $\checkmark$

(1)

Q3

3/10

3.2,

~~SPI~~ ^{I²C} USES A ~~SEPA~~ A SEPERATE DATA LINE FOR SEND AND RECIEVE OF DATA, WORKS IN FULL MEANING THAT IT CAN SEND AND RECIEVE AT THE SAME TIME DUE TO MULTIPLE SLAVES AND MASTERS. $\times$

SPI USES A SHARED DATA LINE FOR SENDING AND ~~RE~~ RECIEVING MEANING IT CAN ONLY DO ONE AT A TIME, THE SYSTEM WORKS IN HALF WITH A MULTI MASTER SYSTEM. $\times$

3.3,

- A, DEPENDANT ON THE MEMORY HIERARCHY OR WHERE THE SECOND REQUEST HAS COME FROM WILL DICTATE WHICH IS ACTIONED FIRST $\checkmark$ $\times$ also need d/s as
~~ISR~~ (1) ^{ISR.}
 Response.
 B, NOT A PROBLEM $\checkmark$ (1)
 C, BOTH ACTIONS WILL ULTIMATELY BE COMPLETED BUT IN AN ORDER DICTATED BY THE SYSTEM. $\times$

Q4
2/5

4.1, AMDAHL'S LAW ALLOWS THE COST TO PERFORMANCE AND THE EFFICIENCY INCREASE OF A NEW COMPONENT TO BE CALCULATED.

4.2, $\frac{1}{(1-F) + \frac{F}{K}}$ F = PERCENTAGE OF WORK COMPLETED
BY THE COMPONENT
K = PERFORMANCE INCREASE

4.3, 1, $\frac{1}{(1-0.7) + \frac{0.7}{1.5}}$ 1.5
= 3.28 % INCREASE

2, $\frac{1}{(1-0.3) + \frac{0.3}{2.5}}$ 2.5
= 1.43 % INCREASE

$$\frac{10000}{3.28}$$

$$\frac{7000}{1.43}$$

= 3048.78 PER 1%
↑

= 4895.1 PER 1%

BETTER OPTION.

4

5

5,

5.1, USB - UNIVERSAL SERIAL BUS ✓ ①

Q5

8/10

5.2, MEMORY:

- DATA
- CONTROL X
- INPUT

5.3, USB 1 - 12 MBIT_s

USB 2 - 480 MBIT_s

USB 3 - 5 GBIT_s ✓

USB 3.1 - 10 GBIT_s

②

5.4, 1 - ELECTRICAL STATE CHANGE

2 - REQUEST DEVICE DETAILS

3 - FIND AND LOAD DRIVER ✓

4 - REQUEST DEVICE PROPERTIES

5 - ISSUE DEVICE WITH AN ADDRESS. ⑤