

EXAMINATION INTERNAL VERIFICATION FORM (2017-2018)

MODULE :	PSDE 6015 – Electronic design			LEVEL:	6
PROGRAMME :	BSc Electrical and Electronic Engineering			TERM OF EXAM: (SPRING OR SUMMER)	Summer
LEARNING OUTCOME(S) BEING ASSESSED:	All	EXAM PAPER:	Main	EXAMINATION AUTHOR :	M Hall

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1.	1/2/2018	This exam conforms to the module criteria and is fit for purpose.	16/03/2018
2.			

INTERNAL VERIFIER PLEASE TICK TO INDICATE THAT THE EXAMINATION:	
✓	Conforms to the assessment pattern described in the module syllabus
✓	Tests the module learning outcome(s) appropriately

SIGNATURES OF FINAL APPROVAL:	SIGNATURE	DATE
INTERNAL VERIFIER: I confirm that this version of the exam paper is ready to be sent to the external examiner		16/03/2018
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LOCATION: COLEG SIR GAR

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LEVEL 6

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**EXAMINATION PERIOD
MAY 2018**

**CYFNOD ARHOLIADAU
MAI 2018**

MODULE CODE: PSDE 6015

Electronic Design

TIME: 2 HOURS

THIS PAPER IS IN 2 PARTS:

ANSWER ALL QUESTIONS IN PART A

ANSWER TWO QUESTIONS OUT OF THREE IN PART B

Equipment or materials required – Calculator

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MAIN

Formulae

$$\text{Voltage Regulation} = \frac{V_{no-load} - V_{full-load}}{V_{full-load}}$$

$$I_{L(max)} = \frac{V_Z}{R_{L(min)}}$$

$$R_{S(max)} = \frac{V_{in} - V_Z}{I_{L(max)} + I_{Z(min)}}$$

$$R_S = \frac{V_{in} - V_Z}{I_B + I_Z}$$

$$T_A = T_J - P_D \theta_{JA}$$

$$\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA}$$

$$T_S = T_J - (\theta_{JC} \times P_d)$$

$$h_c = 2.21 \times 10^{-3} \left(\frac{T_s - T_A}{H} \right)^{\frac{1}{4}}$$

$$h_r = 1.47 \times 10^{-10} \times \varepsilon \left(\frac{T_s + T_A}{2} + 273 \right)^3$$

$$\theta_{SA} = \frac{1}{2 \times H^2 \times \eta \times h}$$

$$I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_{GS(off)}} \right]^2$$

$$V_{DS} = V_{DD} - I_{DSS} R_D$$

$$MTBF = \frac{e^{\frac{tr}{\tau}}}{T_0 \times f \times a}$$

PART A – Answer ALL 8 questions.

A1. Power supply A delivers $18V_{DC}$ with a ripple of $0.7V_{rms}$ while power supply B delivers $35V_{DC}$ with a ripple of $1V_{rms}$. Which is the better power supply?

(4 marks)

A2. Explain the operation of the circuit shown below in Figure A2:

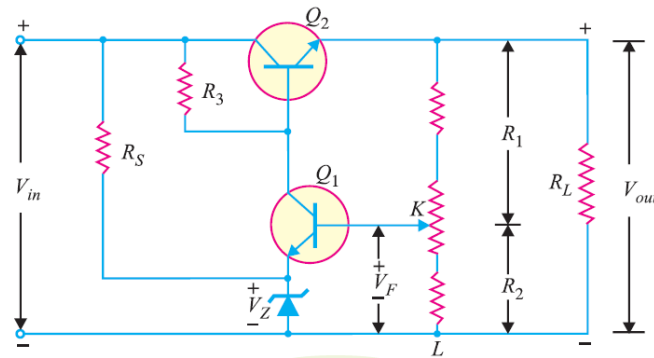


Figure A2

(5 marks)

A3. Determine the maximum allowable value of R_S for the zener voltage regulator circuit shown below given that $V_{in} = 24V$, $V_z = 4.7V$, $I_{Z(min)} = 1.7mA$ and R_L is variable between $1.1k\Omega$ and $1.5k\Omega$

(5 marks)

A4. A MC7809CT voltage regulator in a TO-220 case is required to dissipate $400mW$ at a desired junction temperature of $80^\circ C$. From the datasheet, θ_{JA} is $190^\circ C/W$ and θ_{JC} is $3^\circ C/W$

- i. Determine whether a heat-sink is required for the regulator to operate at normal room temperature ($22^\circ C$).
- ii. If the power output was increased to $3W$ and all other factors remain the same, calculate the required heat-sink. The IC is to be mounted without an insulator using heatsink compound with a θ_{CS} of $1.6^\circ C/W$.

(6 marks)

A5. Explain 3 considerations that must be taken into account when selecting which type of ASIC to choose for a specific design?

(6 marks)

A6. A JFET has a drain current of $12mA$. If $I_{DSS} = 17mA$ and $V_{GS(off)} = -4.5V$, find the value of V_{GS} .

(4 marks)

A7. Figure A7 below shows the circuit of a zener voltage regulator, explain how this circuit counters the negative effects of 'zener impedance' and produces a reference voltage with a stable temperature characteristic.

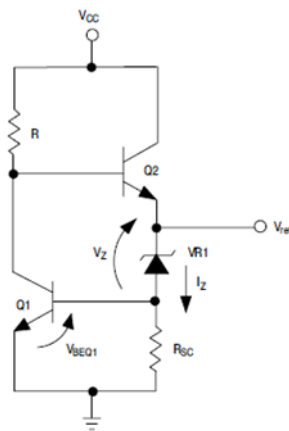


Figure A7

(5 marks)

A8. Explain the term metastability in FPGA design and how it can occur.

(5 marks)

Total Marks for Part A = 40

PART B – Only answer 2 of the following 3 questions (B1, B2, B3)

Question B1 – Power Supply Design and Thermal Management

- a. Figure B1.1 shows a voltage regulator, where the load current varies from 0 to 2.5A and the unregulated DC input varies between 10 and 20V. The zener diode requires at least 1.1mA of current to stay in its regulating region (i.e. $I_{Z(\min)} = 1.1\text{mA}$). β of the transistor = 70. Determine:

- The value of R_S to ensure proper circuit operation
- The maximum power dissipation in R_S .
- The maximum power dissipation in the zener diode.

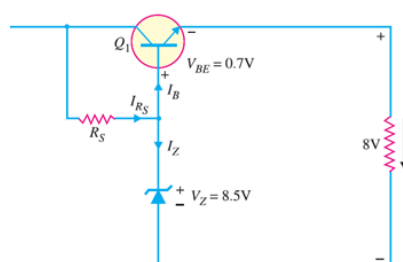


Figure B1.1

(8 marks)

- b. Explain the operation of the circuit shown in Figure B1.2.

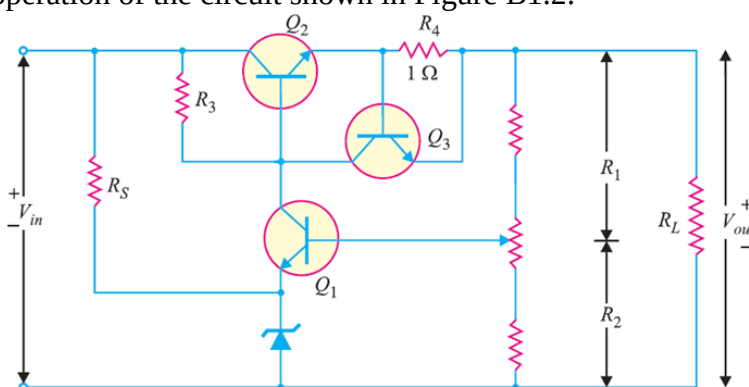


Figure B1.2

(6 marks)

- c. A vertical heat sink solution is required for an IC delivering 7.5W in an environment with an ambient temperature of 80°C. A 3" square and a 2" square fin of 1/16th" oxidised copper is available. For each heat sink, determine the value of θ_{SA} and state which is most appropriate for the application given that $T_J = 175^\circ\text{C}$, $\theta_{JC} = 4^\circ\text{C/W}$ and $\theta_{CS} = 1.6^\circ\text{C/W}$. A nomograph is included at the end of this paper. (**Remove it and insert it into your answer book**)

(16 marks)

Total Marks for Question B1 = 30

Question B2 – Programmable Logic Devices

- Explain with the aid of a diagram the operation of a N-channel depletion mode MOSFET. (6 marks)
- Show how an OR gate may be implemented on a PLD by showing the arrangement of the fusible links. (3 marks)
- Explain how a MOSFET is biased using the “zero bias” technique. (6 marks)
- The circuit shown below in Figure B2.1 has two identical flip-flops which are clocked at 30MHz. The synchronising flip-flop is sampling an asynchronous 8MHz input.

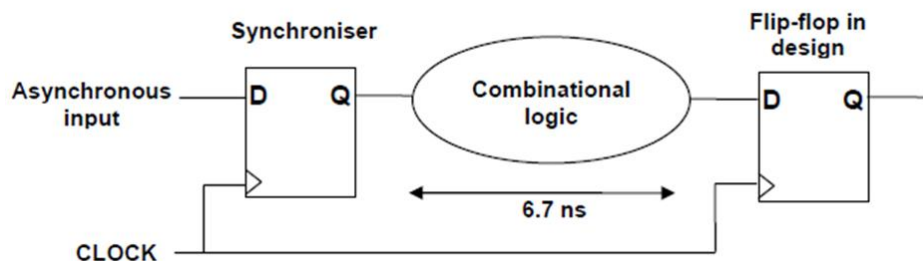


Figure B2.1

Given that:

$$\tau = 0.25\text{ns},$$

$$T_0 = 9 \times 10^{-18}\text{s}$$

$$t_{\text{setup}} = 1\text{ns}$$

- Calculate the resolution time and MTBF of the circuit.
- If the clock frequency in the circuit above is quadrupled, calculate the effect on MTBF.
- Show how the circuit can be modified to improve the MTBF by adding an additional flip-flop. Give an expression to estimate the new MTBF and calculate the new value. Use the quadrupled clock frequency. (15 marks)

Total Marks for Question B2 = 30

Question B3 – VHDL and ASIC Technology

- a. There are four main types of Application Specific Integrated Circuits (ASIC's), give a brief description of each type. (8 marks)
- b. Compare block diagrams representing the design flow for an ASIC and the design flow for a Field Programmable Gate Array (FPGA). (6 marks)
- c. The VHDL file shown below is taken from National Instruments MultiSim PLD Design and emulates the operation of a standard logic block.
- What are the inputs to the device and what are outputs from the device?
 - Draw a block diagram of the device 'Entity'.
 - Explain the operation of the device with the aid of a truth table.

```
library IEEE;  
use IEEE.STD_LOGIC_1164.ALL;
```

```
entity Gate1 is  
port (  
    A, B, C, D : in STD_LOGIC;  
    LT, RBI, BI : in STD_LOGIC;  
    Y:out STD_LOGIC_VECTOR (7 downto 0)  
);  
end Gate1;
```

```
architecture BEHAVIORAL of Gate1 is  
    signal O : STD_LOGIC_VECTOR(0 TO 6);
```

```
begin  
    process (BI,LT,RBI,A,B,C,D)  
    begin  
        if BI='0' then O<="1111111";  
        elsif LT='0' then O<="0000000";  
        elsif (A='0' and B='0' and C='0' and D='0' and RBI='1') then O<="0000001";  
        elsif (A='1' and B='0' and C='0' and D='0') then O<="1001111";  
        elsif (A='0' and B='1' and C='0' and D='0') then O<="0010010";  
        elsif (A='1' and B='1' and C='0' and D='0') then O<="0000110";  
        elsif (A='0' and B='0' and C='1' and D='0') then O<="1001100";  
        elsif (A='1' and B='0' and C='1' and D='0') then O<="0100100";  
        elsif (A='0' and B='1' and C='1' and D='0') then O<="1100000";  
        elsif (A='1' and B='1' and C='1' and D='0') then O<="0001111";  
        elsif (A='0' and B='0' and C='0' and D='1') then O<="0000000";  
        elsif (A='1' and B='0' and C='0' and D='1') then O<="0001100";  
        elsif (A='0' and B='1' and C='0' and D='1') then O<="1110010";  
        elsif (A='1' and B='1' and C='0' and D='1') then O<="1100110";
```

```

    elsif (A='0' and B='0' and C='1' and D='1') then O<="1011100";
    elsif (A='1' and B='0' and C='1' and D='1') then O<="0110100";
    elsif (A='0' and B='1' and C='1' and D='1') then O<="1110000";
    elsif (A='1' and B='1' and C='1' and D='1') then O<="1111111";
end if;
end process;
Y6<=O(6);
Y5<=O(5);
Y4<=O(4);
Y3<=O(3);
Y2<=O(2);
Y1<=O(1);
Y0<=O(0);
end BEHAVIORAL;

```

(10 marks)

d. Give a brief explanation of the following coding methods:

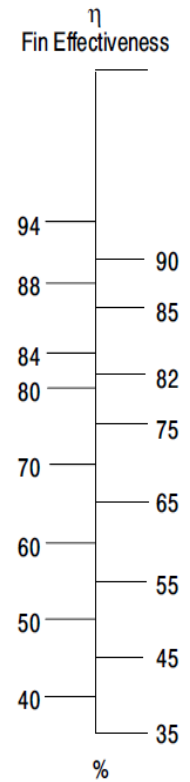
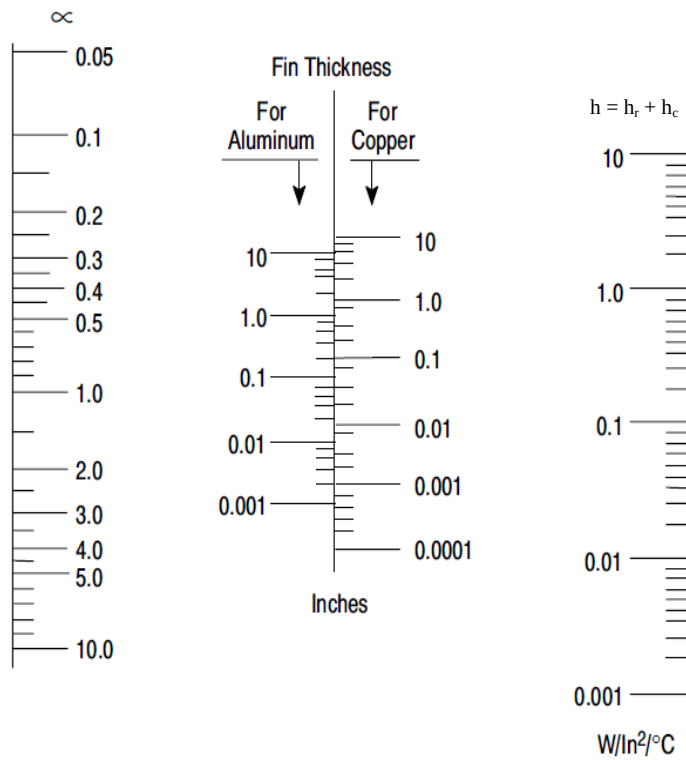
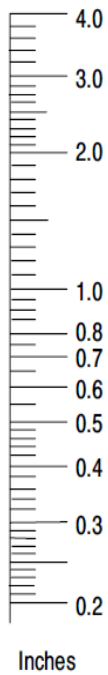
- i. Gray State Encoding
- ii. One-hot State Encoding

(6 marks)

Total Marks for Question B3 = 30

Diwedd/End

$$B=H/2$$



SURFACE	EMISSION, E
Polished Aluminum	0.05
Polished Copper	0.07
Rolled Sheet Steel	0.66
Oxidized Copper	0.70
Black Anodized Aluminum	0.7 - 0.9
Black Air Drying Enamel	0.85 - 0.91
Dark Varnish	0.89 - 0.93
Black Oil Paint	0.92 - 0.96



EXAMINATION SOLUTIONS
(to accompany the examination paper sent to the external examiner
but NOT to be seen by students)

Programme:	BSc in Electrical & Electronic Engineering	Level:	6
Module:	PSDE 6015 Electronic Design		
Author:	M Hall	Page:	Page 1 of 12

Part A	Question	Marks
A1	<i>For A, Ripple Factor</i> $= \frac{V_{rms}}{V_{DC}} = \frac{0.7}{18} = 0.039$ <i>For B, Ripple Factor</i> $= \frac{V_{rms}}{V_{DC}} = \frac{1}{35} = 0.029$ Power Supply B is therefore better	2 1 1
A2	The unregulated DC supply is fed to the voltage regulator. The circuit maintains a constant output voltage irrespective of the variations in load or input voltage. It does this in the following way: Suppose the output voltage increases due to any reason. This causes an increase in voltage across R2 as it is a part of the output circuit. This in turn means that more VF is fed back to the base of transistor Q1; producing a large collector current in Q1. Most of this collector current flows through R3 and causes the base voltage of Q2 to decrease. This results in less output voltage i.e. increase in voltage is offset. Thus output voltage remains constant. Similarly, if the output voltage tries to decrease, the feedback voltage VF also decreases. This reduces the current through Q1 and R3. This means more base voltage at Q2 and more output voltage. Consequently, the output voltage remains at the original level.	5

A3	$I_{L(max)} = \frac{V_Z}{R_{L(min)}} = \frac{4.7}{1100} = 4.3mA$ $R_{S(max)} = \frac{V_{in} - V_Z}{I_{L(max)} + I_{Z(min)}} = \frac{24 - 4.7}{4.3m + 1.7m} = 3.22k\Omega$	2 3
A4i.	$T_A = T_J - P_D \phi_{JA}$ $T_A = 80 - (400m \times 190) = 4^\circ C$ Since the actual $T_A = 22^\circ C$ a heatsink is required.	2 1
ii.	$\phi_{SA} = \frac{T_J - T_A}{P_D} - \phi_{JC} - \phi_{CS}$ $\phi_{SA} = \frac{80 - 22}{3} - 3 - 1.6 = 14.7^\circ C/W$ Therefore a $14.7^\circ C/W$ heatsink is required.	3
A5	3 from the following: <u>Time to Market</u> Time to market is a primary driver Dramatic increase in profit with earlier time-to-market landing Cutting one month off schedule increases profit roughly 10% <u>Cost</u> Standard cell synthesis can cost £125k per license Typical standard cell NRE £50K to £200K If you can't spend at least a million, you are not in the game One bug in a standard cell design can be a disaster A standard cell "re-spin" takes possibly 8 weeks and a lot of money Really cheap tools are available for FPGA implementation – free! FPGAs cost £10-100 each in single quantity FPGA bugs are fixed at zero cost in minutes <u>Technical Feasibility</u> Can it run fast enough? Is it low enough power? Can it operate at 1.2V? Is the required IP (Intellectual Property) available? <u>Financial Analysis</u> What is the cost to get first prototypes (NRE) What is the volume piece part price? How many will we ship? How much market share would we lose?	6

A6	$I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_{GS(off)}} \right]^2$ $V_{GS} = V_{GS(off)} \left[1 - \sqrt{\frac{I_D}{I_{DSS}}} \right] = -4.5 \left[1 - \sqrt{\frac{12m}{17m}} \right] = -0.72V$	4
A7	The effect of zener impedance can be minimized by driving the zener diode with a constant current. The value of the zener current is largely independent of VCC and is given by: $I_Z = \frac{V_{BEQ1}}{R_{SC}}$ This gives a reference voltage of: $V_{ref} = V_Z + V_{BEQ1} = V_{BZ} + I_Z Z_Z + V_{BEQ1}$ The reference voltage is therefore largely independent of supply voltage variations. This configuration has the additional benefit of better temperature stability than that of a simple Resistor - zener reference. From the diagram, it can be seen that the reference voltage temperature stability is equal to that of the zener diode, VR1. The stability of zener diodes used in most integrated circuitry is about +/- 2.2 mV/°C or 0.04%/°C . If the junction temperature varies 100°C, the zener reference voltage would vary 4%. A variation this large is usually unacceptable. However, the circuit does not have this drawback. Here the positive 2.2 mV/°C temperature coefficient of the zener diode is offset by the negative 2.2 mV/°C TC of the V_{BE} of Q₁. This results in a reference voltage with very stable temperature characteristics.	5
A8	Metastability within an FPGA design will typically occur in one of two ways: When an incoming signal is asynchronous with regard to the clock domain. This may be an external input signal or a signal crossing between clock domains. In this case, the design engineer is expected to resynchronise the signal to address metastability, which is certain to occur eventually. This is where a multi-stage synchroniser is typically employed. When multiple register elements in a synchronous design are using the same clock, but phase alignments or clock skew issues mean that the output from one register violates another register's setup and hold time. This may be addressed by modifying the place-and-route constraints or by changing the logic design itself.	5

Q. B1	Question	Marks
a.i.	$I_{B(max)} = \frac{I_{L(max)}}{\beta} = \frac{2.5}{70} = 35.7mA$ $I_{RS} = I_{Z(min)} + I_{B(max)} = 1.1m + 35.7m = 36.8mA$ $V_{RS(max)} = V_{in(max)} - V_Z = 20 - 8.5 = 11.5V$ $R_S = \frac{V_{RS(max)}}{I_{RS}} = \frac{11.5}{36.8} = 312.5\Omega$	1 1 1 1
ii.	$P_{RS} = \frac{(V_{RS(max)})^2}{R_S} = \frac{11.5^2}{312.5} = 0.39W$	2
iii.	$I_{Z(max)} = I_{RS(max)} = \frac{V_{RS(max)}}{R_S} = \frac{11.5}{312.5} = 36.8mA$ $P_{Z(max)} = V_Z I_{Z(max)} = 8.5 \times 36.8m = 312.8mW$	1 1
b.	The main drawback of any series regulator is that the pass transistor can be destroyed by excessive load current if the load is accidentally shorted. To avoid such an eventuality, a current limiting circuit is added to a series regulator. A current limiting circuit consists of a transistor (Q_3) and a series resistor (R_4) that is connected between base and emitter terminals. When the load current is normal, the voltage across R_4 equals the voltage across base-emitter of Q_3 and Q_3 is biased off. Under this condition, the circuit works as normal. If load current becomes excessive, the voltage across R_4 becomes large enough to turn on Q_3. The collector current of Q_3 flows through R_3, thereby decreasing the base voltage of Q_2. The decrease in base voltage of Q_2 reduces the conduction of pass transistor Q_2, preventing any further increase in load current. Thus, the load current for the circuit is limited.	6

c.

$$\phi_{JA} = \frac{T_J - T_A}{P_D}$$

$$\phi_{JA} = \frac{175 - 80}{7.5} = 12.7^\circ\text{C}/\text{W}$$

$$\text{Required } \phi_{SA} = \phi_{JA} - \phi_{CS} - \phi_{JC}$$

$$= 12.7 - 4 - 1.6 = 7.1^\circ\text{C}/\text{W}$$

$$T_S = T_J - (\phi_{JC} \times P_d) = 175 - (4 \times 7.5) = 145^\circ\text{C}$$

$$h_r = 1.47 \times 10^{-10} \times \varepsilon \left(\frac{T_s + T_A}{2} + 273 \right)^3$$

$$= 1.47 \times 10^{-10} \times 0.7 \left(\frac{145 + 80}{2} + 273 \right)^3 = 5.9 \times 10^{-3} \text{W}/^\circ\text{Cm}^2$$

For 3" sink.

$$h_c = 2.21 \times 10^{-3} \left(\frac{T_s - T_A}{3} \right)^{\frac{1}{4}}$$

$$= 2.21 \times 10^{-3} \left(\frac{145 - 80}{3} \right)^{\frac{1}{4}} = 4.77 \times 10^{-3} \text{W}/^\circ\text{Cm}^2$$

$$h = h_r + h_c = 4.77 \times 10^{-3} + 5.9 \times 10^{-3} = 10.67 \times 10^{-3} \text{W}/^\circ\text{Cm}^2$$

From nomograph

$$\alpha = 0.26$$

$$B = H/2 = 3/2 = 1.5$$

$$\eta = 94\%$$

$$\phi_{SA} = \frac{1}{2H^2 \times \eta \times h} = \frac{1}{2 \times 3^2 \times 0.94 \times 10.67 \times 10^{-3}} = 5.54^\circ\text{C}/\text{W}$$

For 2" sink.

$$h_c = 2.21 \times 10^{-3} \left(\frac{T_s - T_A}{2} \right)^{\frac{1}{4}}$$

$$= 2.21 \times 10^{-3} \left(\frac{145 - 80}{2} \right)^{\frac{1}{4}} = 5.28 \times 10^{-3} \text{W}/^\circ\text{Cm}^2$$

$$h_r = 5.9 \times 10^{-3} \text{W}/^\circ\text{Cm}^2$$

	$h = h_r + h_c = 5.28 \times 10^{-3} + 5.9 \times 10^{-3} = 11.18 \times 10^{-3} \text{ W/}^\circ\text{Cm}^2$ From nomograph $\alpha = 0.35$ $B = H/2 = 2/2 = 1$ $\eta = 95\%$ $\emptyset_{SA} = \frac{1}{2H^2 \times \eta \times h} = \frac{1}{2 \times 2^2 \times 1 \times 11.18 \times 10^{-3}} = 11.2 \text{ }^\circ\text{C/W}$ The 3" sink is therefore the better option	1 1 1
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Q.B2	Question	Marks
a.	The diagram below shows a depletion-mode n-channel MOSFET. Since the gate is negative, it means electrons are on the gate as shown. These electrons repel the free electrons in the n-channel, leaving a layer of positive ions in a part of the channel. In other words, we have depleted the n-channel of some of its free electrons. Therefore, lesser number of free electrons are made available for current conduction through the n-channel. This is the same thing as if the resistance of the channel is increased. The greater the negative voltage on the gate, the lesser is the current from source to drain. Thus by changing the negative voltage on the gate, we can vary the resistance of the n-channel and hence the current from source to drain. Because the action with negative gate depends upon depleting the channel of free electrons, the negative-gate operation is called depletion mode.	2 4
b.		3
c.	Since a D-MOSFET can be operated with either positive or negative values of V_{GS}, we can set its Q-point at $V_{GS} = 0V$ as shown below. Then an input a.c. signal to the gate can produce variations above and below the Q-point. We can only change V_{GS} because the values of I_{DSS} and $V_{GS} \text{ (off)}$ are constant for a given D-MOSFET.	2 2

We can use the simple circuit above to provide zero bias. This circuit has $V_{GS} = 0V$ and $I_D = I_{DSS}$. We can find V_{DS} as:

$$V_{DS} = V_{DD} - I_{DSS}R_D$$

Note that for the zero bias circuit a source resistor is not necessary. With no source resistor, the value of V_S is $0V$. This gives us a value of $V_{GS} = 0V$. This biases the circuit at $I_D = I_{DSS}$ and $V_{GS} = 0V$.

2

d.

Given:

$$f_{clk} = 30MHz, \quad t_{clk} = 33.3ns$$

$$a = 8MHz$$

$$t_{prop} = 6.7ns$$

$$\tau = 0.25nS$$

$$T_o = 9 \times 10^{-18} S$$

$$t_{setup} = 1ns$$

i.

$$\text{Resolution time: } t_r = t_{clk} - t_{setup} - t_{prop}$$

$$= (33.3ns - 1ns - 6.7ns)$$

$$= \underline{25.6ns}$$

1

$$MTBF = \frac{e^{\frac{t_r}{\tau}}}{T_o \times f_{clk} \times a}$$

$$MTBF = \frac{e^{\frac{25.6n}{0.25n}}}{(9 \times 10^{-18}) \times (30 \times 10^6) \times (8 \times 10^6)} = \frac{e^{102.4}}{2.16m}$$

$$= \underline{1.37 \times 10^{47} S}$$

4

Equivalent to 4.35×10^{39} years

ii.

Quadrupling the clock frequency

Given:

$$F_{clk} = 120MHz, \quad t_{clk} = 8.33ns$$

$$\text{Resolution time: } t_r = t_{clk} - t_{setup} - t_{prop}$$

$$= (40ns - 1ns - 6.7ns)$$

$$= \underline{0.63ns}$$

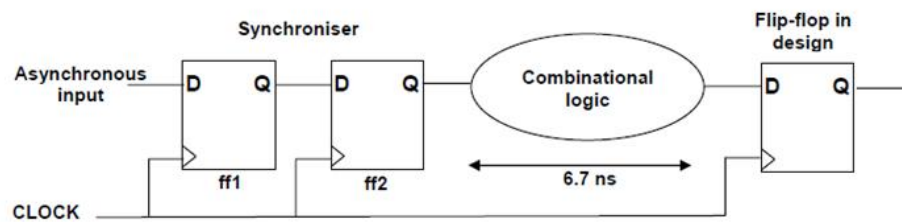
1

$$MTBF = \frac{e^{\frac{t_r}{\tau}}}{T_o \times f_{clk} \times a}$$

$$MTBF = \frac{\frac{0.63n}{e^{0.25n}}}{(9 \times 10^{-18}) \times (120 \times 10^6) \times (8 \times 10^6)} = \frac{12.43}{8.64m} = 1439s$$

Equivalent to 24 minutes.

iii.



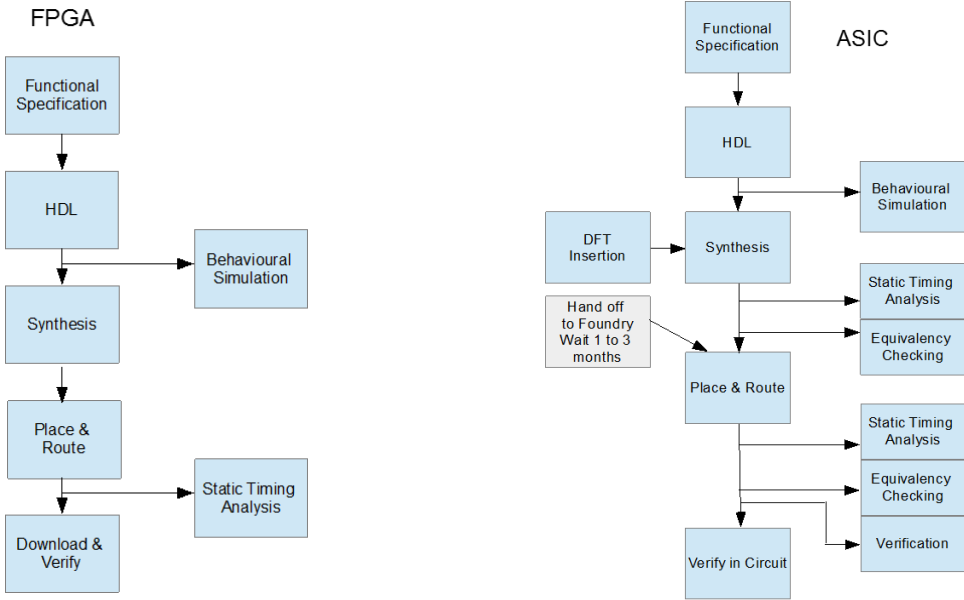
$$MTBF = \left\{ \frac{e^{\frac{t_r}{\tau}}}{T_o \times f_{clk} \times a} \right\} \times k \left\{ \frac{e^{\frac{t_r}{\tau}}}{T_o \times f_{clk}} \right\}$$

Where $k = 1$ for one extra flip-flop

$$MTBF = \left\{ \frac{\frac{0.63n}{e^{0.25n}}}{(9 \times 10^{-18}) \times (120 \times 10^6) \times (8 \times 10^6)} \right\} \times \left\{ \frac{\frac{0.63n}{e^{0.25n}}}{(9 \times 10^{-18}) \times (120 \times 10^6)} \right\}$$

New MTBF = $16.55 \times 10^{12}S$

Equivalent = 524,930 years

Q. B3	Question	Marks
a.	<u>Full Custom</u> Each transistor is hand drawn Analogue parts are done this way Highest performance, longest design time Hand optimized parts of high-end uPs Full set of masks needed <u>Standard Cell ASIC</u> Predesigned (standard) cells in a library are used These cells are connected together to form the design High performance, much shorter design time than full custom Most digital ASICs are designed this way Usually uses HDLs with logic synthesis Full set of masks needed <u>Gate Array ASIC</u> Pre-drawn transistors are on a die These transistors are connected together to form cells The cells are connected to form a design Usually digital in nature Lower performance, but very quick to fabricate Only metallization masks are needed Usually uses HDLs with logic synthesis <u>FPGA ASIC</u> Fully predesigned silicon, logic functions and interconnect Programmed with a "bit file" to configure logic and interconnect Medium performance, higher power consumption Very quick to implement, minutes Better for more limited volume applications Almost always uses HDLs plus logic synthesis No DFT structures required Popular for ASIC prototyping	2 2 2 2
b.	 The image contains two flowcharts. The left flowchart, titled 'FPGA', shows a linear process: Functional Specification → HDL → Synthesis → Place & Route → Download & Verify. There are side boxes for 'Behavioural Simulation' (connected to HDL and Synthesis) and 'Static Timing Analysis' (connected to Place & Route). The right flowchart, titled 'ASIC', shows a more complex process: Functional Specification → HDL → Synthesis → Place & Route → Verify in Circuit. Side boxes include 'Behavioural Simulation' (connected to HDL), 'DFT Insertion' (connected to Synthesis), 'Hand off to Foundry Wait 1 to 3 months' (connected to Synthesis and Place & Route), 'Static Timing Analysis' (connected to Synthesis and Place & Route), 'Equivalency Checking' (connected to Synthesis and Place & Route), and 'Verification' (connected to Verify in Circuit).	6

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[illegible]

d.	Gray State Encoding Guarantees that only one bit switches between two consecutive states. It is appropriate for controllers exhibiting long paths without branching. Minimizes hazards and glitches. Good results can be obtained when implementing the state register with T flip-flops. Can be used to minimize power dissipation. One-hot State Encoding One-Hot State Encoding is the default encoding scheme. It assigns a distinct bit of code to each FSM state. As a result, the state register is implemented with one flip-flop for each state. In a given clock cycle during operation, one and only one bit of the state register is asserted. Only two bits toggle during a transition between two states. One-Hot State Encoding is usually a good choice for optimizing speed or reducing power dissipation.	3 3
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