

1809801 Assignment 1

by Kieran Williams

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Finite State Machines

Kieran Williams

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1. Executive Summary

The aim of this assignment is to apply the theory involved in designing complex electronic circuits and to demonstrate the understanding of the need to promote sustainable development. In this assignment, critical analysis will take place of the design of a complex circuit and the design will be adapted to meet new applications.

The circuit that will be built is a traffic light system. The circuit will be built using a series of Finite State Machines. The circuit will comprise of a series of logic gates and flip-flops. The design of the circuit is split into 4 sections, a 5 second timer, a 15 second timer, a RAG controller and the final circuit design.

Analysis will be done by testing the outputs of the circuit by connecting them to a logic analyser and doing simulations on Multisim and by downloading the circuits onto the Nexys4 DDR board. Once each circuit has been tested then the final circuit will be put together by combining each sub-circuit and this will also be tested and analysed.

The modification aspect of the assignment will also be carried out using Finite State Machines. The modification will be a pressure pad addition.

A conclusion will be written to bring together any findings or results and an explanation of how the system could be implemented to promote sustainable development.

2. Research into Advanced Digital Design Techniques

Combinational logic solely contains a circuit logic gates such as NAND, NOR and NOT. Therefore, the output is directly related to the input. There is no feedback present in the circuitry. The circuit has a few uses in terms of operation, it provides arithmetic logic for two operands, conversion of code and transmission of data. They can convert code from binary to BCD and BCD to binary. The outputs of combinational circuits can be described as Boolean algebra. Sequential logic circuits combine combinational logic with memory elements. The output of a sequential logic depends on the two factors, the input state and the state of the previous output. A sequential logic has a series of feedback loops which help determine the next output and a clock is used to synchronize both elements (Electronics Coach, n.d.)

So, in summary both combinational and sequential logic circuits are the fundamental bases for digital circuits, but memory elements in the sequential logic creates the gap between them both. The outputs of both circuits are also different. The combinational logic output is relative to the input however the present input and the previous state of the output determines the output of the sequential logic circuit. A Feedback loop is present only in the sequential logic circuit in order to remember the previous output. A combinational logic circuit does not include a clock input. To design a combinational logic circuit takes less steps than designing a sequential logic circuit.

A finite state machine (FSM) is a design tool used to design coding and circuits. There are many advantages to using this type of method. It can be used on a large variety of software; the design technique is rigorous yet produces a simple and consistent coding structure if used correctly. The documentation created can be easily organised so makes fault finding a simple task. A finite state machine consists of a number of states, when something is inputted to the machine it will change its state to the next state depending on the previous state and the input state. However, inputting the same state doesn't always produce the same result because of the change in state.

Field Programmable Gate Arrays (FPGA's) are devices that are based around logic blocks that are connected by programmable interconnections. FPGA's can be easily reprogrammed to meet the demands of functionality after manufacturing. FPGA boards are ideal devices for many different markets such as aerospace, automotive industries, medical uses and video processing etc. (Xilinx, n.d.)

Application-Specific Integrated Circuit (ASIC) is a microchip that is designed for a specific application. ASIC devices can have different designs to allow for specific actions to be taken inside the device, the two design methods are gate-array and full-custom array. A gate-array design uses diffused layers consisting of transistors, predefined devices and wafers. Once the device is ready for its final design the engineer can open and close switches to allow the device to act in the required way. Full-custom design are more complex in design and can be much smaller due to the deletion of unnecessary gates that will be defined by the customer. These boards are designed specifically for one customer to provide a function required by the customer's end product (Smith, 2016)

The difference between ASIC's and FPGA's is that FPGA's can be reprogrammed to the desired application unlike ASIC's. One-time programmable (OTP) FPGA's are available, however the most popular types are SRAM based which enables them to be reprogrammed as the design evolves (Xilinx, n.d.)

Sustainability is key in digital electronics, especially circuit design. Technology is getting more advanced and more complex circuitry is able to be manufactured at a smaller size to fit in the growing demand of mobile phones and portable technology. Climate change is an ever-growing topic and the demand for industries to become more economic and more resourceful is increasing, so sustainable development of products is big part in designing circuits. Circuits can be designed to use more recyclable materials and old circuits can be disposed of correctly and potentially reused. Businesses can also choose more eco-friendly ways of transporting products to customers.

3. Design Method, Choices and Calculations

In order to create the traffic light system, a specification was written out in order to understand the inputs, outputs and sequence of the system. The traffic light system would have the sequence in the following order:

GREEN, AMBER, AMBER, RED, RED/AMBER, RED/AMBER.

The following diagram below (Figure 1) shows the connections between each FSM. When button (B) is pressed, a 5 second counter will activate which will enable the cars some time to pass without having to come to an abrupt stop. When the 5 second timer has finished timing the output (W) will go high which will activate the RAG controller, when the light turns red, it will activate a 15 second counter which allows plenty of time for the pedestrian to cross, once the 15 second delay has finished counting the output (T) will activate and will reset the RAG controller which will allow the sequence to go back to green.

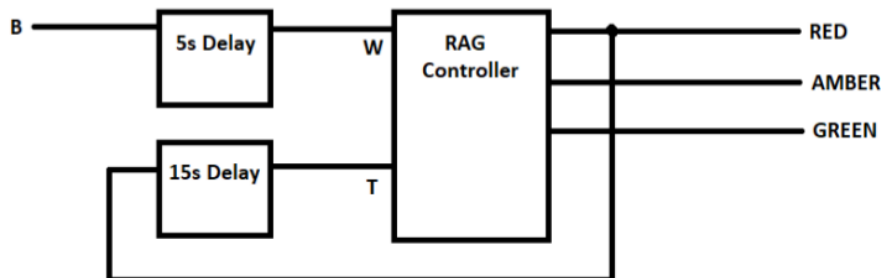


Figure 1 - Traffic Light System Diagram

Once the specification and sequence of events had been established, the next step was to create state diagrams and truth tables in order to produce the Boolean expressions needed to design the delay FSM's and RAG controller.

5 Second Delay:

S0 - Reset

S1 - 1 second

S2 - 2 second

S3 - 3 second

S4 - 4 second

S4 - 5 second

The state diagram is shown below in (Figure 2):

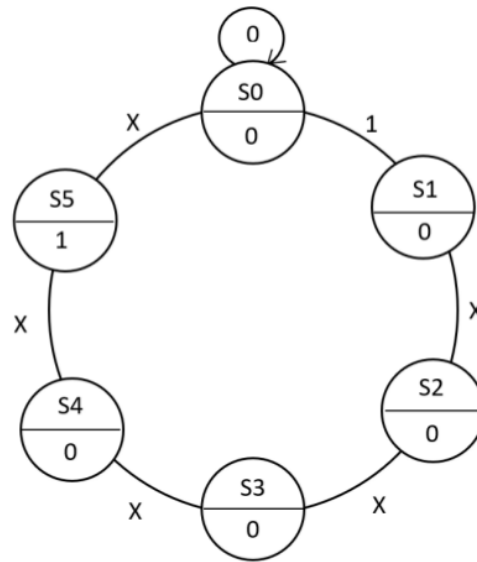


Figure 2 - 5 Second Delay State Diagram

The first state is S0, it will stay in this state until the input is activated. The input in this diagram is “B” when the button has been pressed the input will go high and therefore moving onto the next state and starting the 5 second delay. Once the sequence reaches S5 the output will go high (W) and activate the RAG controller. From the above diagram a truth table was produced:

Current	Next		Current			B = 0			B = 1			Output
	B = 0	B = 1	QA	QB	QC	QA+	QB+	QC+	QA+	QB+	QC+	
S0	S0	S1	0	0	0	0	0	0	0	0	1	0
S1	S2	S2	0	0	1	0	1	0	0	1	0	0
S2	S3	S3	0	1	0	0	1	1	0	1	1	0
S3	S4	S4	0	1	1	1	0	0	1	0	0	0
S4	S5	S5	1	0	0	1	0	1	1	0	1	0
S5	S0	S0	1	0	1	0	0	0	0	0	0	1
S6	X	X	X	X	X	X	X	X	X	X	X	X
S7	X	X	X	X	X	X	X	X	X	X	X	X

Table 1 - 5 Second Delay Truth Table

From the truth table, Boolean expressions for QA+, QB+ and QC+ and for the output W were formed by using Karnaugh maps (Figure 3):

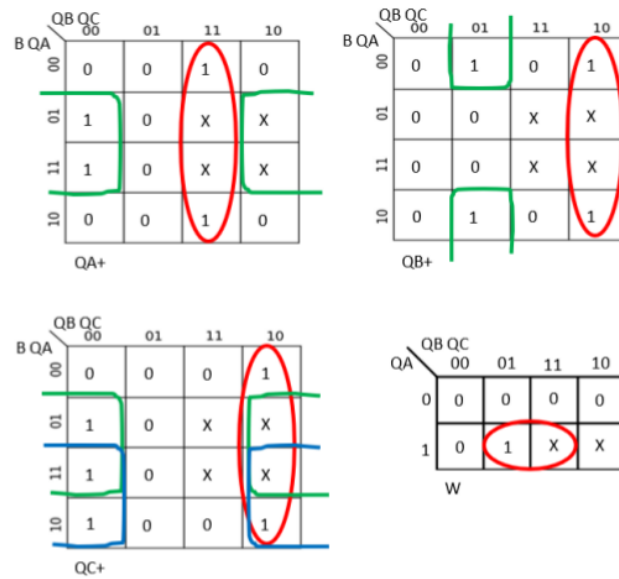


Figure 3 - 5 Second Delay Karnaugh Maps

From the Karnaugh maps, the groupings could be collected together to form Boolean expressions:

$$QA+ = QA\bar{Q}C + QBQC$$

$$QB+ = \bar{Q}A\bar{Q}BQC + QB\bar{Q}C$$

$$QC+ = QA\bar{Q}C + B\bar{Q}C + QB\bar{Q}C$$

$$W = QAQC$$

From the Boolean expressions a circuit was drawn using Multisim, the circuit design involves 3 D-type flip-flops and a series of AND gates and OR gates (Figure 4):

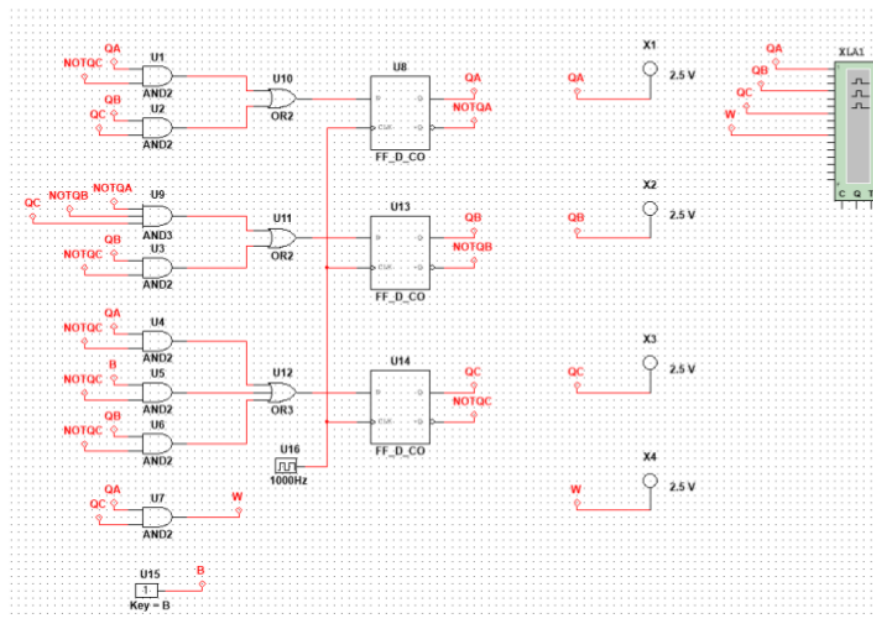


Figure 4 - 5 Second Delay Circuit

15 Second Delay:

S0 - 0 seconds

S1 - 1 second

S2 - 2 seconds

S3 - 3 seconds

S4 - 4 seconds

S5 - 5 seconds

S6 - 6 seconds

S7 - 7 seconds

S8 - 8 seconds

S9 - 9 seconds

S10 - 10 seconds

S11 - 11 seconds

S12 - 12 seconds

S13 - 13 seconds

S14 - 14 seconds

S15 - 15 seconds

The state diagram is shown below in (Figure 5):

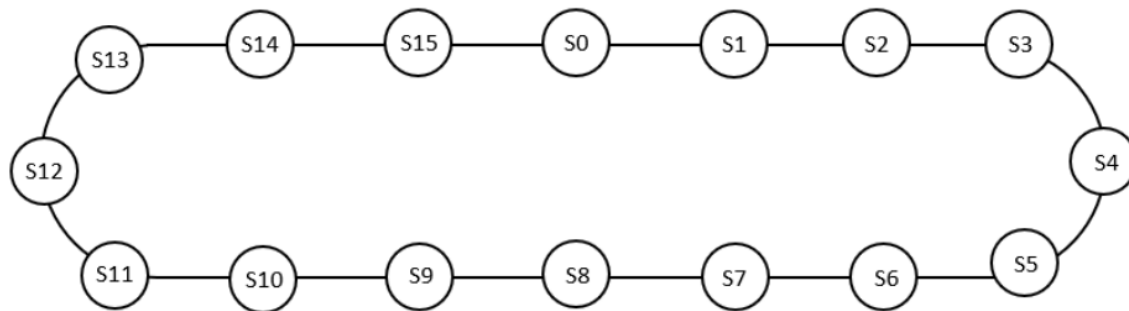


Figure 5 - 15 Second Delay State Diagram

The 15 second delay counter is activated by the RED output on the RAG controller, when this output goes high the 15 second delay will start counting. The first state is S0 which is 0 seconds and the next state is S1 which is 1 second and the pattern continues. When the counter has reached S15 it will reset the RAG controller and the lights will carry on their sequence and go back to green. From the above diagram a truth table was produced:

		Current				Next			
Current	Next	QA	QB	QC	QD	QA+	QB+	QC+	QD+
S0	S1	0	0	0	0	0	0	0	1
S1	S2	0	0	0	1	0	0	1	0
S2	S3	0	0	1	0	0	0	1	1
S3	S4	0	0	1	1	0	1	0	0
S4	S5	0	1	0	0	0	1	0	1
S5	S6	0	1	0	1	0	1	1	0
S6	S7	0	1	1	0	0	1	1	1
S7	S8	0	1	1	1	1	0	0	0
S8	S9	1	0	0	0	1	0	0	1
S9	S10	1	0	0	1	1	0	1	0
S10	S11	1	0	1	0	1	0	1	1
S11	S12	1	0	1	1	1	1	0	0
S12	S13	1	1	0	0	1	1	0	1
S13	S14	1	1	0	1	1	1	1	0
S14	S15	1	1	1	0	1	1	1	1
S15	S0	1	1	1	1	0	0	0	0

Table 2 - 15 Second Delay Truth Table

From the truth table, Boolean expressions for QA+, QB+, QC+ and QD+ were formed by using Karnaugh maps (Figure 6):

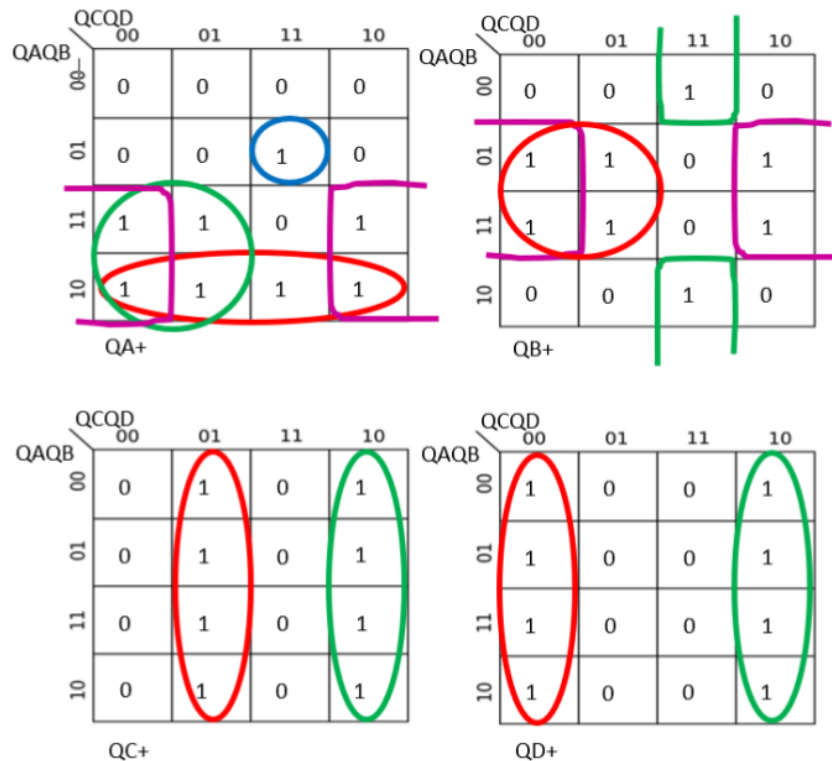


Figure 6 - 15 Second Delay Karnaugh Map

From the Karnaugh maps, the groupings could be collected together to form Boolean expressions:

$$QA+ = QA\bar{Q}\bar{D} + QA\bar{Q}C + QA\bar{Q}\bar{B} + \bar{Q}\bar{A}QBQCQD$$

$$QB+ = QB\bar{Q}\bar{D} + QB\bar{Q}C + \bar{Q}\bar{B}QCQD$$

$$QC+ = QC\bar{Q}\bar{D} + \bar{Q}CQD$$

$$QD+ = \bar{Q}\bar{D}$$

From the Boolean expressions a circuit was drawn using Multisim, the circuit design involves 4 D-type flip-flops and a series of AND gates and OR gates (Figure 7):

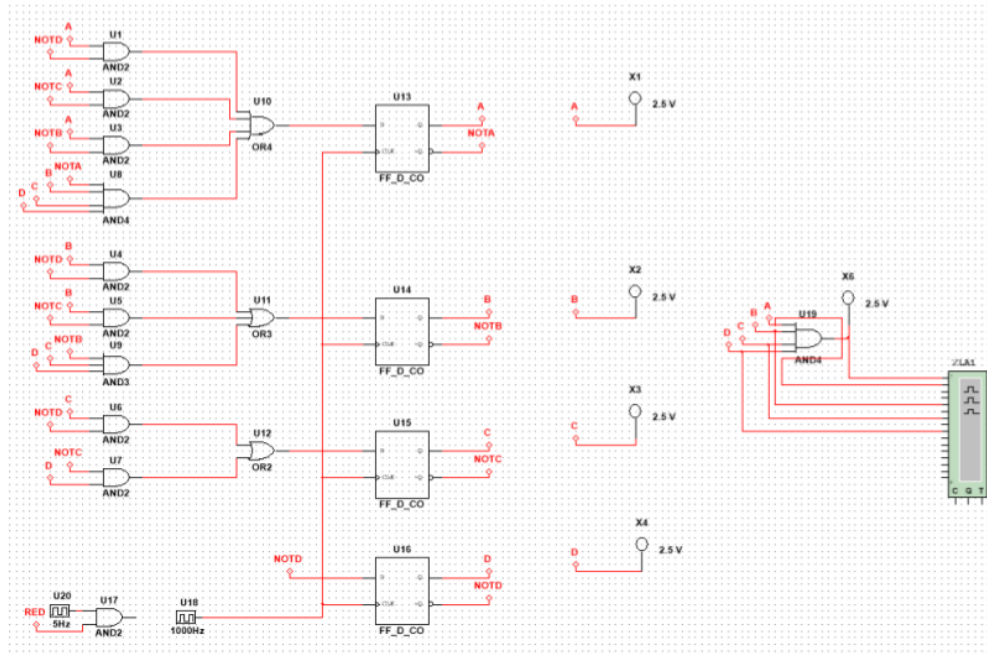


Figure 7 - 15 Second Delay Circuit

RAG Controller:

S0 - GREEN

S1 - AMBER

S2 - AMBER

S3 - RED

S4 - RED/AMBER

S5 - RED/AMBER

The state diagram is shown below in (Figure 8):

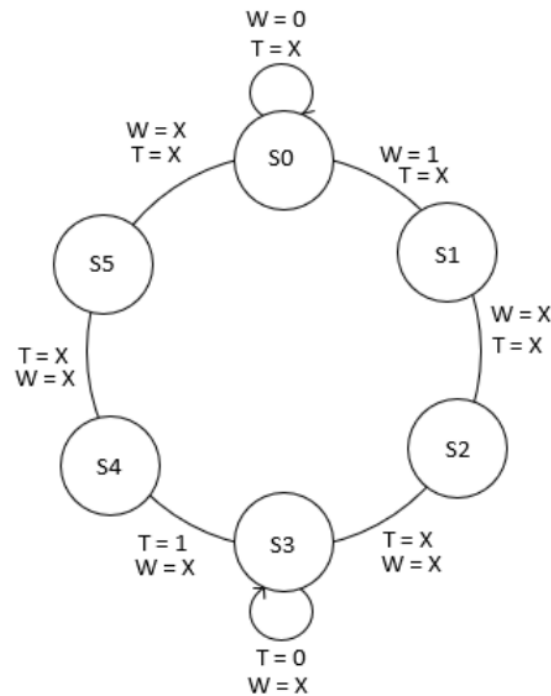


Figure 8 - RAG Controller State Diagram

At S0, if the input W is 0 then the system will stay in S0, however if the 5 second output (W) goes high then the system will move to the next state which is S1. At S3, the system will stay in this state so long as the 15 second output (T) is 0, if the output goes high then the system will move to the next state which is S4. At S3 the system is RED, the lights will stay RED until the 15 second delay has counted up and the output (T) goes high. From the above diagram a truth table was produced:

Current	Next				Current				Next										
	W = 0		W = 1		QA	QB	QC		W = 0				W = 1						
	T = 0	T = 1	T = 0	T = 1					T = 0	QA+	QB+	QC+	T = 1	QA+	QB+	QC+	Output		
S0	S0	S0	S1	S1	0	0	0		0	0	0	0	0	0	1	0	0	1	
S1	S2	S2	S2	S2	0	0	1		0	1	0	0	1	0	0	1	0	1	0
S2	S3	S3	S3	S3	0	1	0		0	1	1	0	1	1	0	1	0	1	0
S3	S3	S4	S3	S4	0	1	1		0	1	1	1	0	0	1	1	0	0	0
S4	S5	S5	S5	S5	1	0	0		1	0	1	1	0	1	1	0	1	1	0
S5	S0	S0	S0	S0	1	0	1		0	0	0	0	0	0	0	0	1	1	0
S6	X	X	X	X	X	X	X		X	X	X	X	X	X	X	X	X	X	X
S7	X	X	X	X	X	X	X		X	X	X	X	X	X	X	X	X	X	X

Table 3 - RAG Controller Truth Table

From the truth table, Boolean expressions for QA+, QB+, QC+ and the outputs R, A, G were formed by using Karnaugh maps (Figure 9):

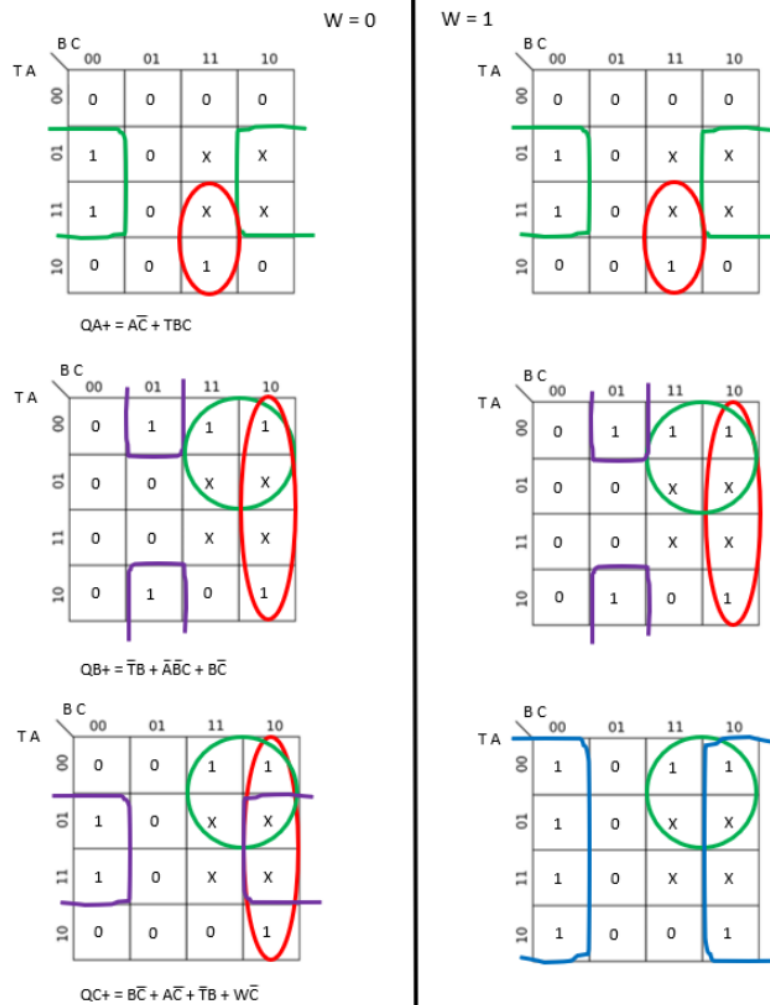


Figure 9 - RAG Controller Karnaugh Map

The Boolean expressions can be seen under each Karnaugh map. Because there were two inputs, the Karnaugh map had to be split to ensure that each of the inputs were accounted for. When T=1 or T=0 and for when W=1 or W=0. The Karnaugh map and Boolean expressions for the outputs are shown below in (Figure 10):

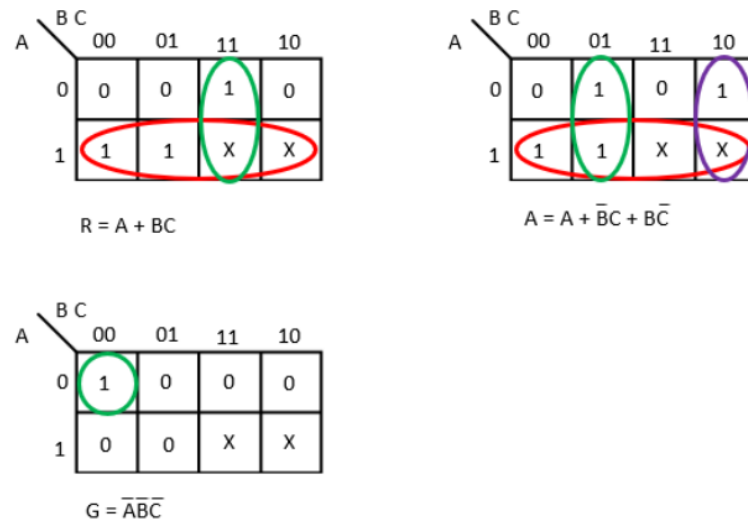


Figure 10 - RAG Controller Output Karnaugh Maps

From the Boolean expressions a circuit was drawn using Multisim, the circuit design involves 3 D-type flip-flops and a series of AND gates and OR gates (Figure 11):

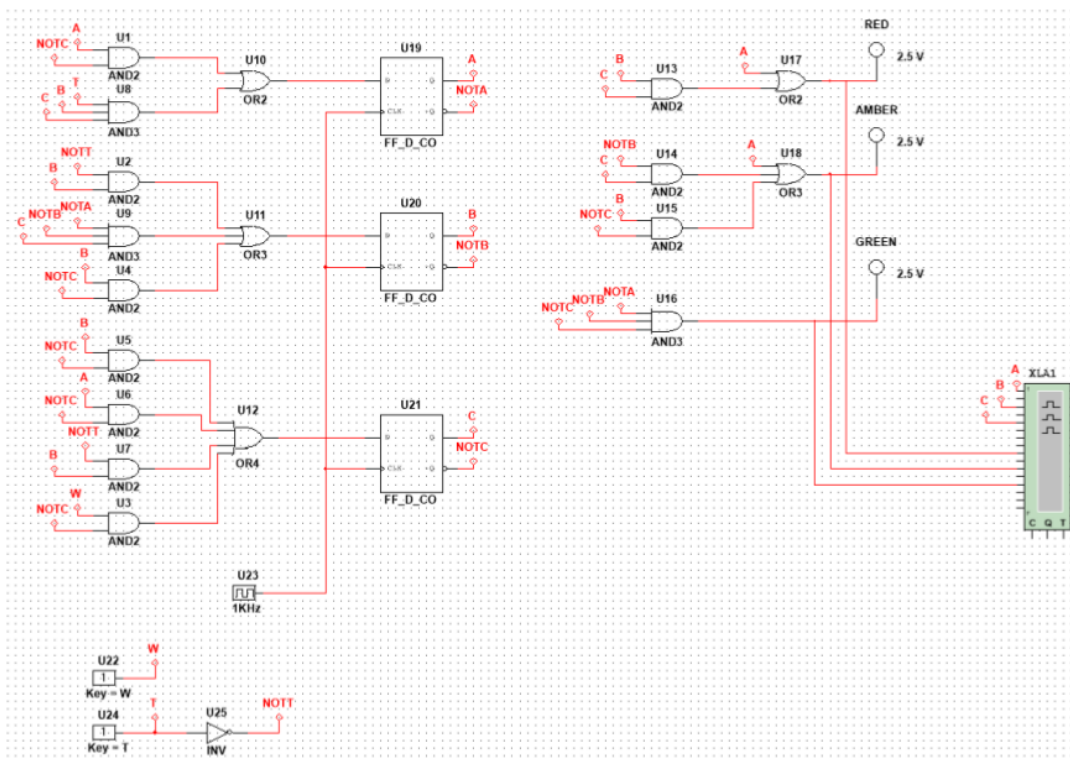


Figure 11 - RAG Controller Circuit

4. Testing, Results and Analysis

5 Second Delay:

A logic analyser was connected to the outputs of the 5 second delay to show the counting sequence, the results are shown below in (Figure 12):

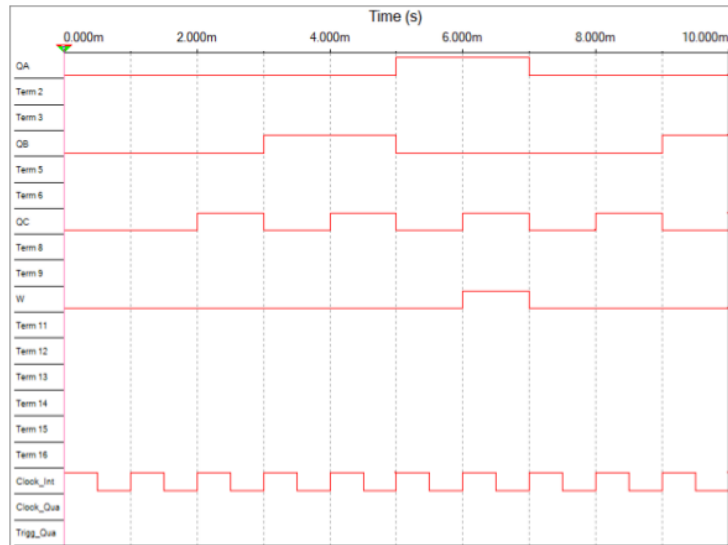


Figure 12 - 5 Second Delay Logic Analyser Results

The outputs QA, QB, QC and W were connected to the logic analyser and from the graph we can see that the output W was high when the QA, QB and QC gave an output of 101 which is 5 in binary code. Therefore, this shows that the 5 second delay operates correctly. The circuit was then converted to PLD mode in order to test the circuit on the Nexys4 DDR board. The PLD circuit is shown below in (Figure 13):

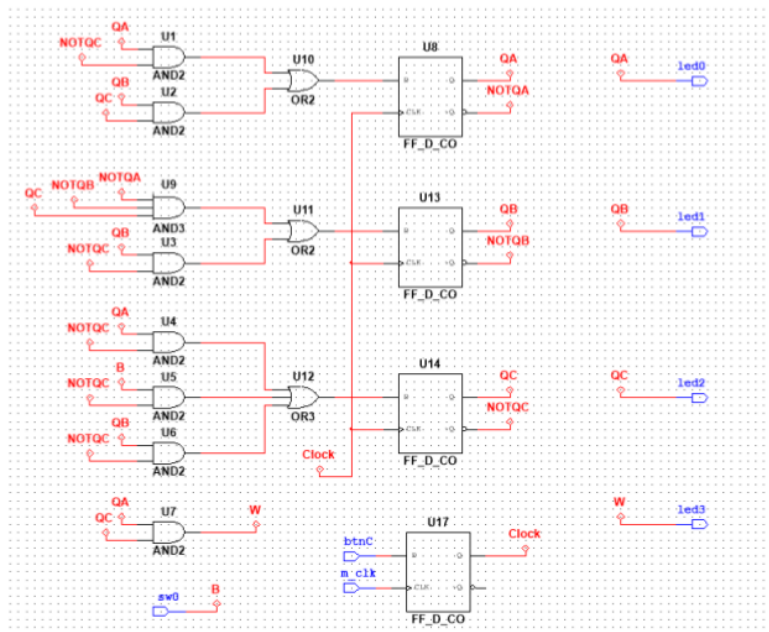


Figure 13 - 5 Second Delay PLD Mode Circuit

15 Second Delay:

A logic analyser was connected to the outputs of the 15 second delay to show the counting sequence, the results are shown below in (Figure 14):

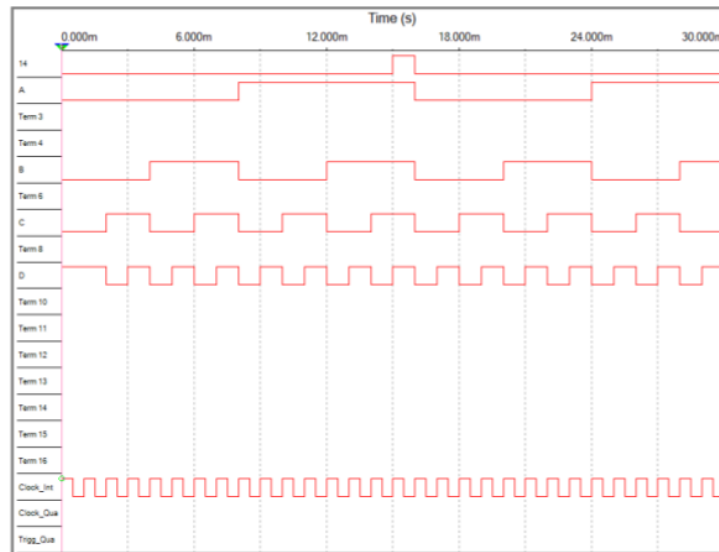


Figure 14 - 15 Second Delay Logic Analyser Results

The outputs A, B, C, D and an LED to show the 15 second count was connected to the logic analyser and from the graph we can see that the LED output was high when the A, B, C and D gave an output of 1111 which is 15 in binary code. Therefore, this shows that the 15 second delay operates correctly. The circuit was then converted to PLD mode in order to test the circuit on the Nexys4 DDR board. The PLD circuit is shown below in (Figure 15):

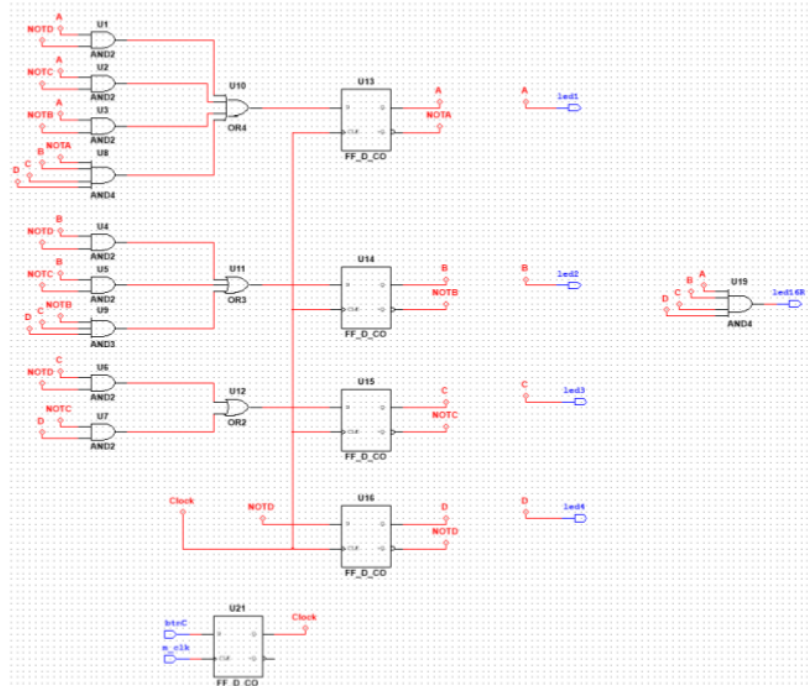


Figure 15 - 15 Second Delay PLD Mode Circuit

RAG Controller:

A logic analyser was connected to the outputs of the RAG controller to show the operating sequence, the results are shown below in (Figure 16):

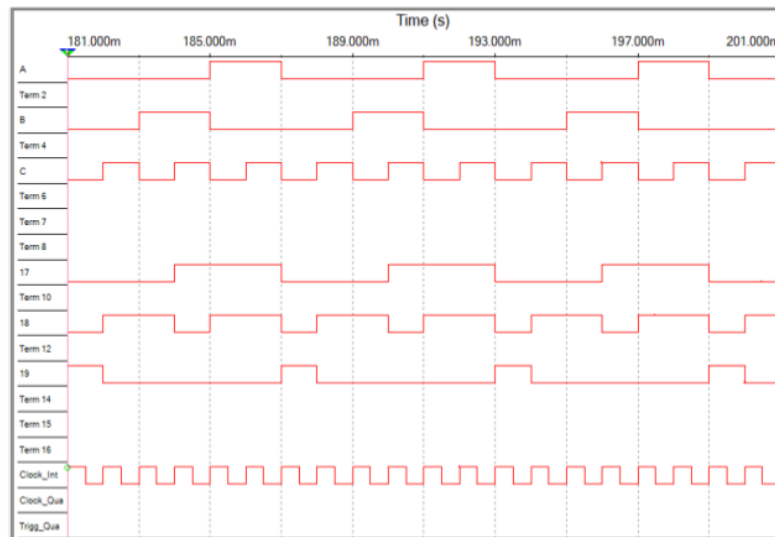


Figure 16 - RAG Controller Logic Analyser Results

The red, amber and green LED's were connected to show the sequence of the lights in the RAG controller. The outputs labelled 17 (RED), 18 (AMBER) and 19 (GREEN) on the graph show the sequence of the lights, the sequence follows the one that is stated in the specification of GREEN, AMBER, AMBER, RED, RED/AMBER, RED/AMBER. Therefore, this shows that the RAG controller is working correctly. The circuit was then converted to PLD mode in order to test the circuit on the Nexys4 DDR board. The PLD circuit is shown below in (Figure 17):

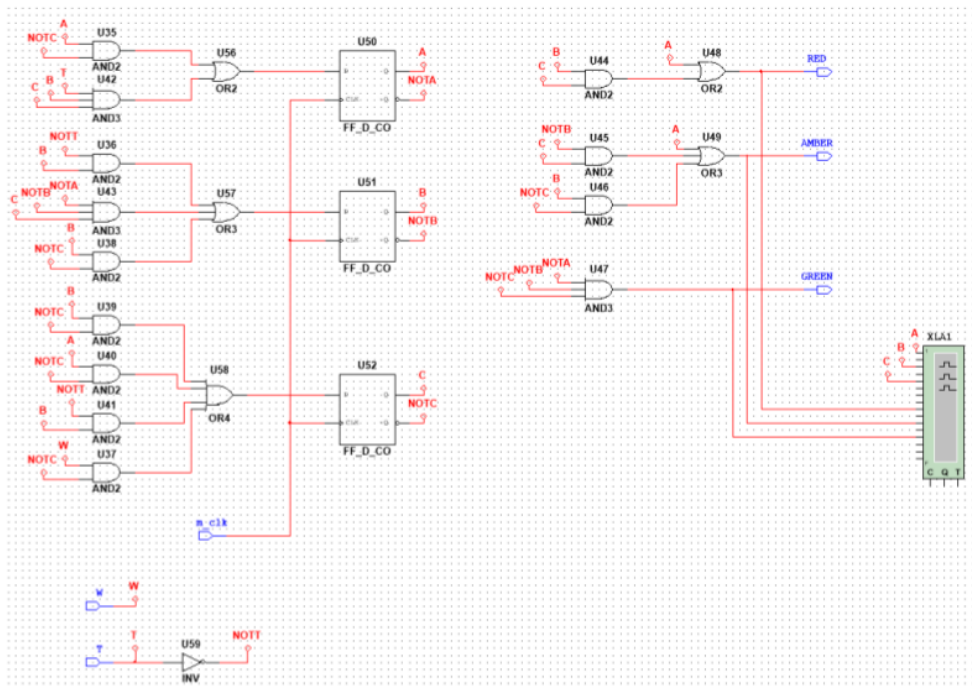


Figure 17 - RAG Controller PLD Mode Circuit

Final Circuit:

In order to create the final circuit, a new PLD mode page was created. There were three sub-circuits that were created on the page in order to link each circuit together. The circuit that was built is shown below in (Figure 18):

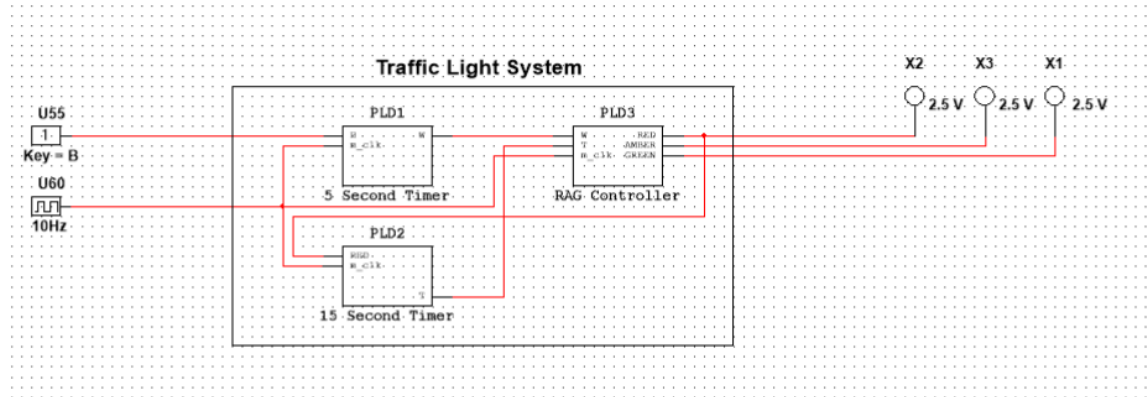


Figure 18 - Final Circuit Test

In order to test the circuit, a manually switched input was connected to the board as well as a clock of 10Hz. The outputs were red, amber and green LED's to simulate the traffic lights. When the switched input was switched to high using the button (B) the green LED stayed lit for 5 seconds before moving to amber and then red. The red LED stayed lit for 15 seconds before switching to red/amber and then back to green. The results of this test can be seen below (Figure 19):

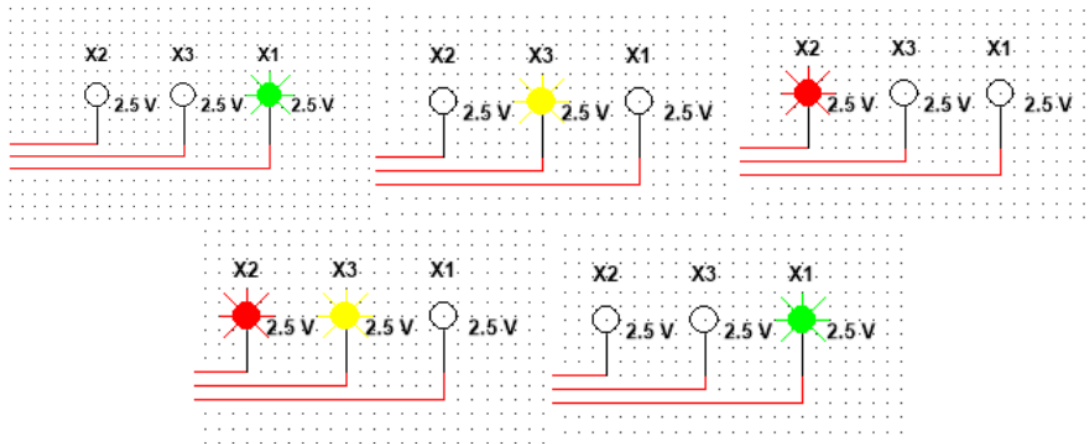


Figure 19 - Final Circuit LED Results

The circuit was then converted to PLD mode in order to test the circuit on the Nexys4 DDR board. Unfortunately, due to software issues the circuit could not be downloaded to the Nexys4 DDR board. The PLD circuit is shown below in (Figure 20):

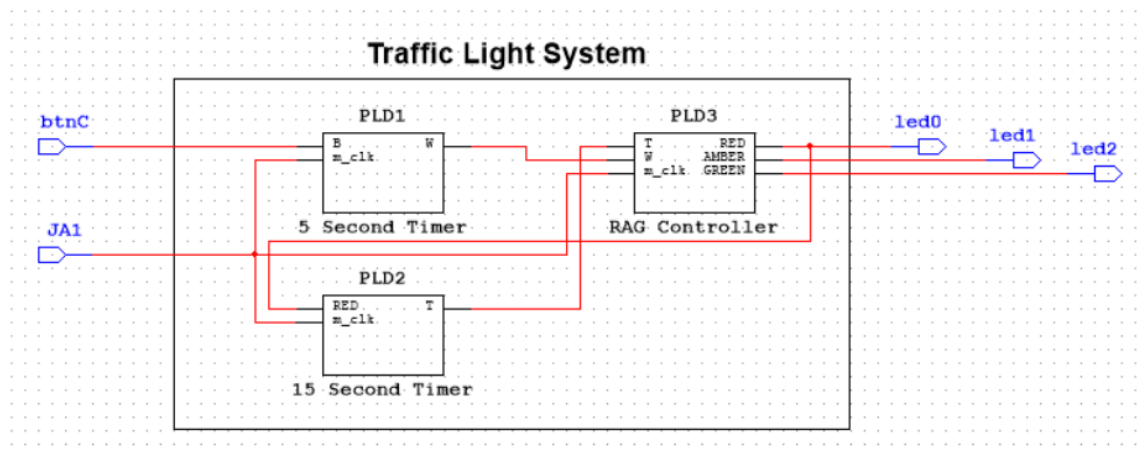


Figure 20 - Final Circuit PLD Mode

The images for tests done on the Nexys4 DDR can be found in the appendix below.

Pressure Pad Modification:

In order to create the pressure pad modification, the 5 second delay state diagram had to be modified slightly to accommodate for the second input. The pressure pad modification is incorporated to ensure that the sequence will only start if there is somebody standing at the lights. The modified state diagram is shown below in (Figure 21):

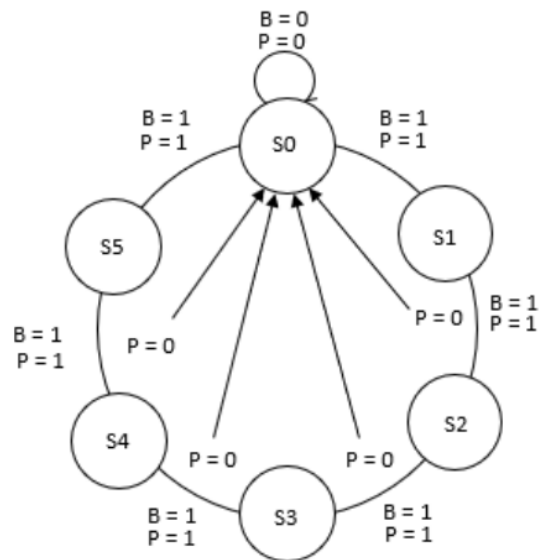


Figure 21 - Pressure Pad Modification State Diagram

If the input (P) was to equal 0 at any stage of the 5 second delay, then it would go back to state 0 and cancel the count. However, if both the inputs (B) and (P) equal 1 then it will carry on the count as normal. From the above diagram a truth table was produced:

Current	Next				Current			Next												Output
	B = 0		B = 1		QA	QB	QC	B = 0			B = 1			B = 0			B = 1			
	P = 0	P = 1	P = 0	P = 1				P = 0	P = 1	P = 0	P = 1	P = 0	P = 1	P = 0	P = 1					
								QA+	QB+	QC+	QA+	QB+	QC+	QA+	QB+	QC+	QA+	QB+	QC+	W
S0	S0	S0	S0	S1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
S1	S2	S2	S0	S2	0	0	1	0	1	0	0	1	0	0	0	0	0	1	0	0
S2	S3	S3	S0	S3	0	1	0	0	1	1	0	1	1	0	0	0	0	1	1	0
S3	S4	S4	S0	S4	0	1	1	1	0	0	1	0	0	0	0	0	1	0	0	0
S4	S5	S5	S0	S5	1	0	0	1	0	1	1	0	1	0	0	1	0	1	0	0
S5	S0	S0	S0	S0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1
S6	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
S7	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Table 4 - Pressure Pad Modification Truth Table

From the truth table, Boolean expressions for QA+, QB+, QC+ and W were formed by using Karnaugh maps (Figure 22):

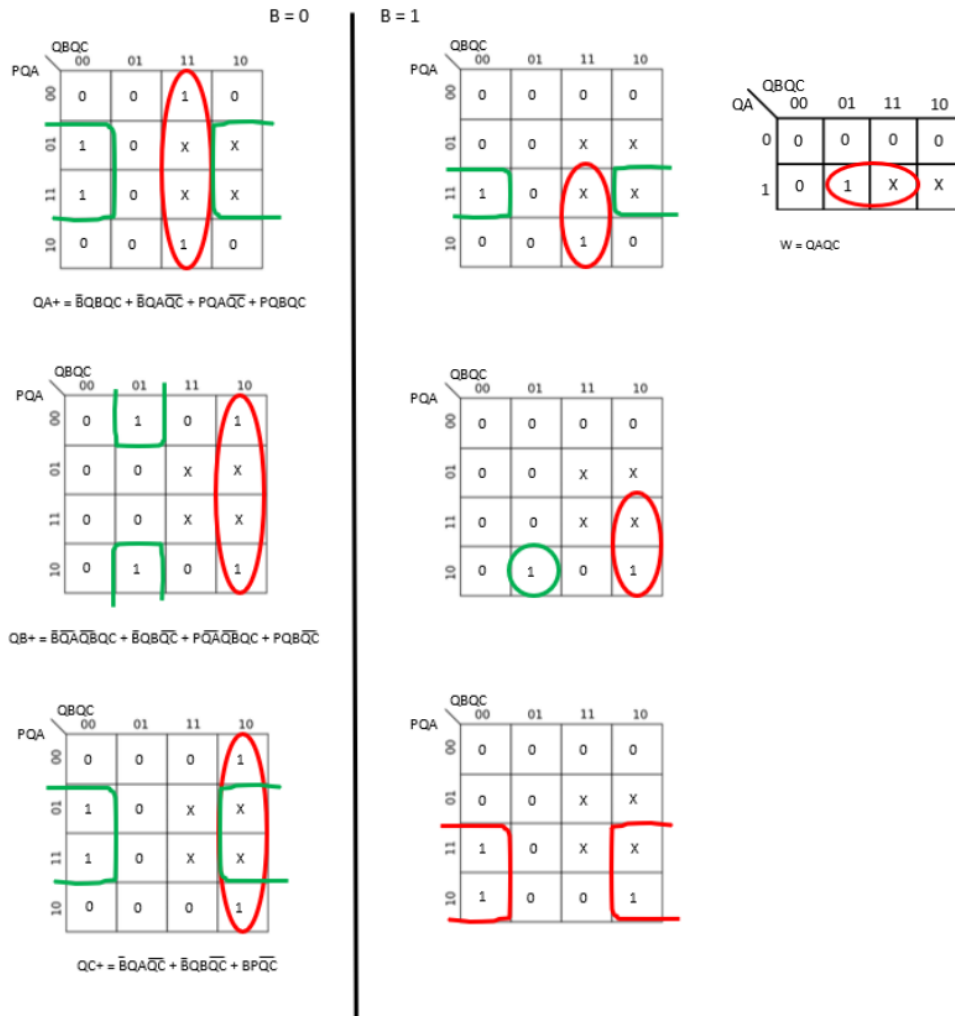


Figure 22 - Pressure Pad Modification Karnaugh Map

The Boolean expressions can be seen under each Karnaugh map. Because there were two inputs, the Karnaugh map had to be split to ensure that each of the inputs were accounted for. When B=1 or B=0 and for when P=1 or P=0.

5. Conclusions and Recommendations

The specification stated that the system would have a sequence in the following order:

GREEN, AMBER, AMBER, RED, RED/AMBER, RED/AMBER.

When button (B) is pressed, a 5 second counter will activate which will enable the cars some time to pass without having to come to an abrupt stop. When the 5 second timer has finished timing the output (W) will go high which will activate the RAG controller, when the light turns red, it will activate a 15 second counter which allows plenty of time for the pedestrian to cross, once the 15 second delay has finished counting the output (T) will activate and will reset the RAG controller which will allow the sequence to go back to green.

From carrying out analysis and testing the circuit, the system worked as the specification stated. When the button was pressed the system would run through its sequence and return back to its original state.

The output of this system was achieved by using sequential logic. From the research carried out, sequential logic combines combinational logic with a memory element. From the circuit design combinational logic was written in the form of logic gates and combined with flip-flops and a clock input the system is of a sequential logic circuit. There are many ways this system could be implemented to support sustainable development. The parts could be made of a more recyclable material to support the re-use of materials and the proper disposal of electronic components. The circuit design could be changed so that it uses less components but without impacting the end result of the system. Manufacturers could look into more eco-friendly ways of transporting goods and products. The system could be developed as an ASIC, by implementing it this way its sole purpose would be for one system only, less components would have to be used to create the system which would lower the cost of production and therefore lower the commercial risk. The downside to this is that the system would not be programmable however the cost drivers outweigh this matter of it not being an FPGA.

6. Reference list and Bibliography

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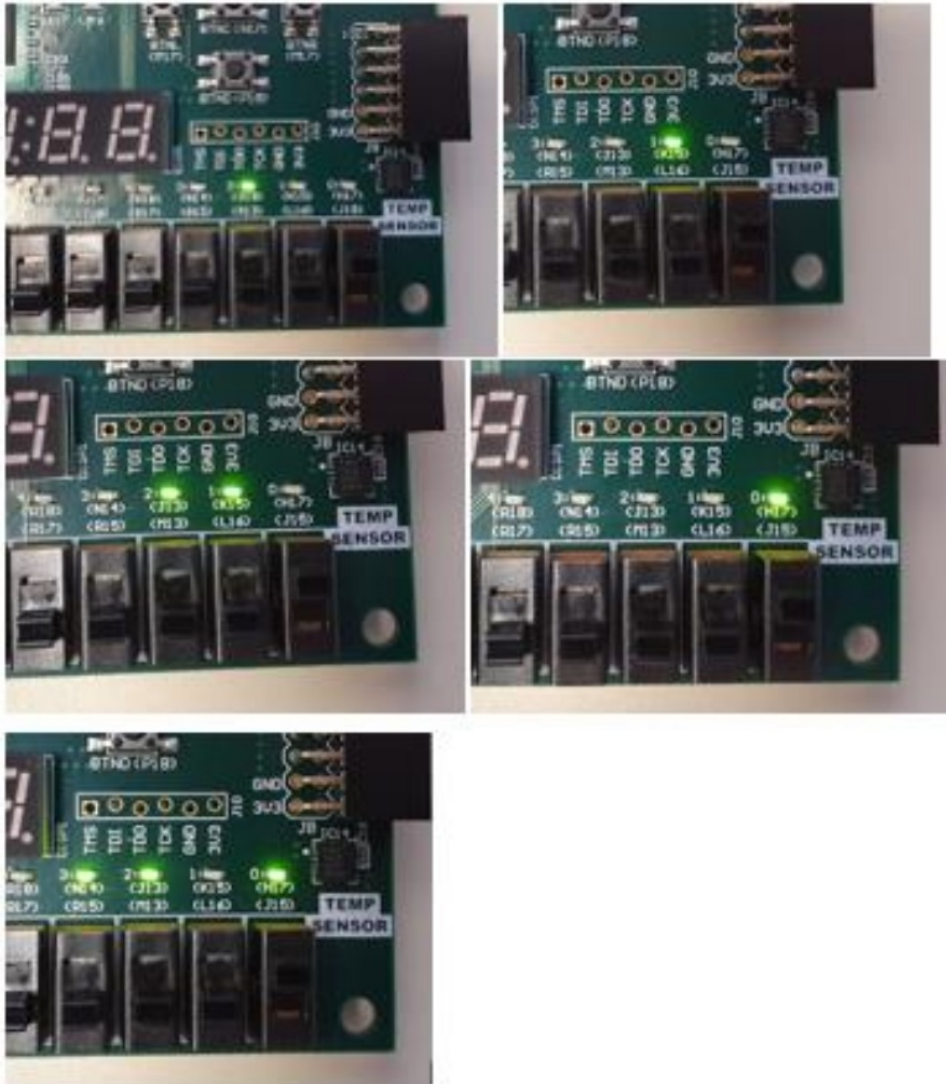
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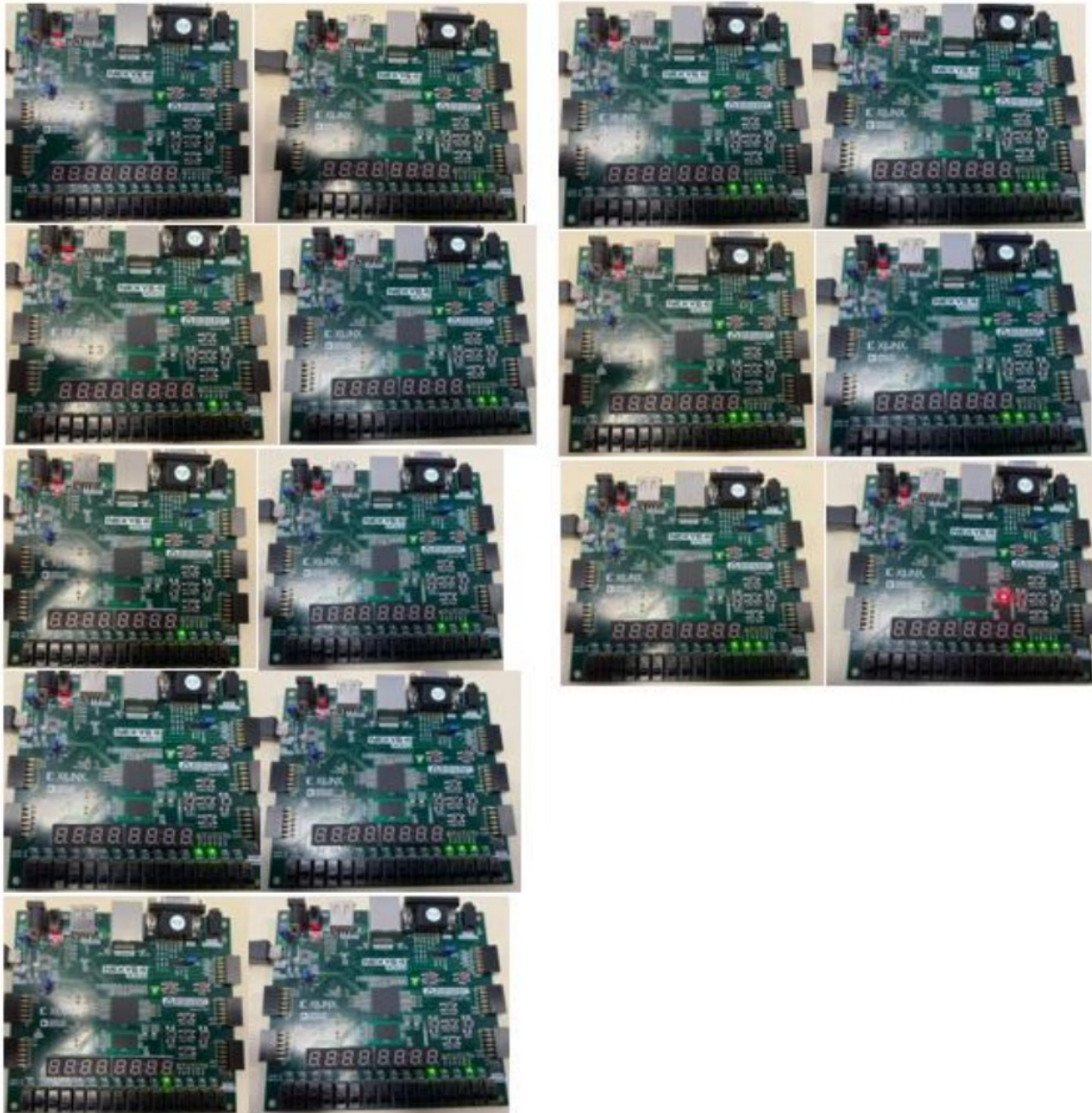
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7. Appendix
5 Second Delay:



15 Second Delay:



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GRADEMARK REPORT

FINAL GRADE

GENERAL COMMENTS

Instructor

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WILLIAMS**

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RESEARCH-INFORMED LITERATURE



There was evidence of further reading and research with the inclusion of a reference list and appropriate in text referencing. Your interpretation and understanding of the additional research was good. Your references were appropriate to the task and your reference list was of an appropriate length for this assignment. More diagrams would have helped your descriptions.

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KNOWLEDGE AND UNDERSTANDING



The knowledge and understanding of the subject

demonstrated by this assignment was generally very good. There were few gaps in your knowledge of the basic principles and your understanding of the higher level concepts was demonstrated to a high degree. You have demonstrated a competent critical understanding of the main concepts and expanded your knowledge beyond that contained in the course notes.

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ANALYSIS



Your analysis of the task was generally very good, both in class and as shown in this assignment. You have demonstrated sound critical analysis skills and your approach to the task was logical. You carried out a detailed evaluation of the results and included a good conclusion relating the practical results to researched theory. The conclusions demonstrated very good cognitive skills and the ability to interpret quantitative and qualitative data without error.

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PRACTICAL APPLICATION AND DEP.



Your application of practical skills for this task was generally excellent. You used both the basic and advanced features of the resources appropriately when designing the circuit and you used appropriate advanced options for testing and evaluating the circuit performance. You managed to design an effective circuit that functioned well within the specification and achieved this by rarely asking for assistance thus demonstrating some advanced problem solving skills. Your results were

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comprehensive and allowed for a detailed conclusion to be written.

SKILLS FOR PROFESSIONAL PRAC.



In this assignment you have demonstrated skills in working individually and also collaboratively. Your written report was written in a professional and confident style, however you still need to be more efficient with your word count. The report was very well presented, with excellent diagrams in appropriate places, good sentence/paragraph structure and clear calculations.

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