

Assignment 1 - final

by James Davies

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PSDE 6018 – Electronic Production and Test

Assignment 2 – Fault Modelling

Andrew Davies

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1. Introduction

Fault modelling is essential in electronic production. It allows for analysis of faults arising from manufacturing defects, and can aid in quick detection of these issues. This technique is widely employed in Integrated Circuit (IC) manufacturing as the gates used in these circuits are typically in the nanometre range, making any defects impossible to detect by conventional means.

Another critical issue with electronics is electro static discharge (ESD), which is brought on by statically charged surfaces.

The aim of this assignment will be to investigate fault modelling techniques, and provide both simulated and practical results in order to confirm these findings. Research into IC fabrication faults and ESD will also be required.

The following objectives will be met during this assignment:

- Research IC fabrication faults, and explain how single stuck fault modelling is carried out. Also research into the causes and prevention methods of ESD.
- Design a combinational logic circuit in NI multisim in order to test fault modelling methods. Use test vector reduction methods to derive the minimum number of test vectors required.
- Perform the same analysis in NI LabView using a logic circuit built on prototype board.
- Analyse and compare both simulated and Practical results.

2. Research

2.1 IC Fabrication Faults

It is possible for a number of faults to occur during the IC manufacturing process; these defects can result in pins being stuck at either a logic 1 or logic 0. A stuck pin will prevent correct operation of the circuit, which will result in errors during operation.

The main terms used are defined below (Li, 2009):

- Defect – A defect is a difference in the device from the hardware design that was not intended by the manufacturer. These can come as a result of a manufacturing or through use. Typical defects are issues such as missing contacts, material defects (cracks etc.) and oxidation. These defects may or may not result in faults. (Kastensmidt, 2008)
- Fault - A fault is defined as a defect that manifests itself at the functional level i.e. the function of the device is affected.
- Error – An error occurs as a result of a fault, and results in incorrect input and output states.
- Failure – A failure occurs when the circuit no longer functions as intended due to the aforementioned elements.

Figure 1 demonstrates a simple stuck at fault. In this example, input b on a NAND gate has been shorted to ground. This will result in an error for each output where b should be at logic 1.

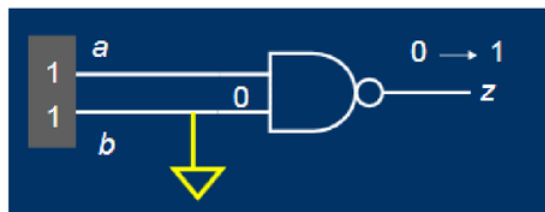


Figure 1: Stuck at fault (Kastensmidt, 2008)

The truth table for NAND gate is shown in Figure 2. From this table, it can be determined the fault will be present twice, but an error will not be apparent when input a is at logic 0 as the output will be 1 regardless. (Kastensmidt, 2008)

Input		Output
A	B	$Y = \overline{A \cdot B}$
0	0	1
0	1	1
1	0	1
1	1	0

Figure 2: NAND gate truth table (Electronics Hub Ltd. , 2015)

2.2 Single Stuck at Fault (SSF) Model

In order to be able to model the faults that can occur, it is necessary to produce a model. By modelling, it is possible to reduce the number of test vectors required, which will result in less time spent testing each circuit.

Typically, a single 'stuck-at' model is used as it provides a quick and simple method of testing.

Modelling multiple faults can quickly become time consuming even in smaller circuits, as it assumes that all combinations of faulty circuits exist. In principle, if all single faults are detected, then most multiple faults will also be found. (McIntyre, 2014)

As a rule, the number of tests required will be equal to $n+1$, where n is the number of nodes present. In comparison, the number of tests required for a multiple fault model is $3n-1$, which can become too large to handle in most circuits. (Sengupta, 2012)

With a stuck at fault model, an input or an output can be kept at either SA1 (stuck at 1) or SA0 (stuck at 0). The truth table for this gate is shown in Figure 3. The complete list of faults that can be tested from this gate are: A stuck at 0, A stuck at 1, B stuck at 0, B stuck at 1, Y stuck at 0, Y stuck at 1. From these faults a full list of test coverage can be made as shown in Figure 5. (Meixner, n.d.)

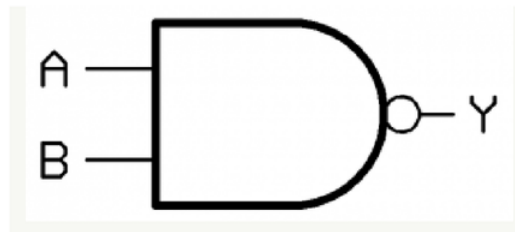


Figure 4: NAND gate (Meixner, n.d.)

A	B	Y
1	0	0
1	1	0
0	0	1
0	1	0

Figure 3: NAND gate truth table (Meixner, n.d.)

Test	Fault						
	none	A/0	B/0	Y/0	A1	B/1	Y/1
00	1	1	1	0	1	1	1
01	1	1	1	0	0	1	1
10	1	1	1	0	1	0	1
11	0	1	1	0	0	1	1

Figure 5: NAND fault testing table

In total, four tests are performed to cover each fault shown in red. The test at 00 is unnecessary, as the only fault is Y stuck at 0. This fault is covered by two other tests, meaning the test requirements are reduced to three. This is in keeping with the rule that the number tests required is $n+1$.

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2.3 Electro Static Discharge (ESD)

ESD is a natural phenomenon whereby thousands of electrostatic volts can be stored statically, and then discharged when in contact with an object at lower potential. This typically isn't an issue, but ICs can be irreparably damaged by as little as 25 electrostatic volts. Consequently, ESD protection should be utilised to prevent this damage.

A common source of ESD is from human contact. Generally, human skin will accumulate positive charges, meaning the discharge will attempt to find a path to ground. On average, human skin will store the equivalent charge to a 250pF capacitor, which will result in a 25,000V discharge.

(Michaels, 1999)

For this reason, a connection to earth should be made when handling delicate electronics. In order to provide this connection, anti-static wrist bands shown in Figure 6 can be used. These can either be connected to earth via a mains socket, or to any other earthed surfaces.



Figure 6: Anti-static wrist band (RS components , n.d.)

What these bands provide is a permanent path to earth, which will result in no static build up. This will protect any ICs being worked on. It is also possible to ground the surface being worked on for further reduction of static charge accumulation.

To protect components during transit and storage, special packaging is used as shown in Figure 7. This packaging prevents ESD from being able to damage the items within. The label shown on the yellow sticker in this image is to warn the user that the contents are ESD sensitive, and to take care when handling the components.



Figure 7: ESD packaging

Source of ESD voltage	Typical Electro Static Voltage in KV at a relative humidity of 20%
Walking across Vinyl floor	12 KV
Walking across synthetic carpet	35 KV
Opening a plastic bag	20 KV
Arising from a foam cushion	18 KV
Sliding plastic box on a carpet	18 KV
Removing plastic tape for a PC board	12 KV
Removing shrink film from PC board	12 KV
Triggering a vacuum solder remover	8 KV
Spraying aerosol freezer spray	15 KV

Figure 8: Typical voltage discharge from different sources (Storr, n.d.)

Figure 8 shows a table demonstrating the static voltage discharges from various sources at 20% relative humidity. This shows how important it is to avoid certain materials when working with electronics.

Good use of table for examples.

Figure 9 shows the susceptibility of various electronic devices to ESD. By comparing to the aforementioned table, it can clearly be seen the amount of damage that ESD can cause to components.

Device type	ESD susceptibility
Bipolar transistors	380 to 7000 Volt
CMOS logic devices	250 to 3000 Volt
EPROM devices	100 volt
Film resistors	300 to 3000 Volt
TTL logic devices	1000 to 2500 Volt
Microprocessor chips	as low as 10 Volt

Figure 9: ESD susceptibility (Storr, n.d.)

A major area of concern for ESD is in an explosive atmosphere. ESD can cause ignition in the right conditions, which could lead to an explosion. For that reason, it is important to only install devices that are not susceptible to static charges in these environments. (lgus Inc., n.d.)

Reasonable amount of research with appropriate sources.

3. Design of Assignment Requirements

In order to properly test the fault modelling techniques, it was first necessary to simulate the circuit in multisim. Figure 10 shows this circuit with no faults present. There are four logic gates used: a three-input nand, a two-input nor, a two-input and, and a two-input or.

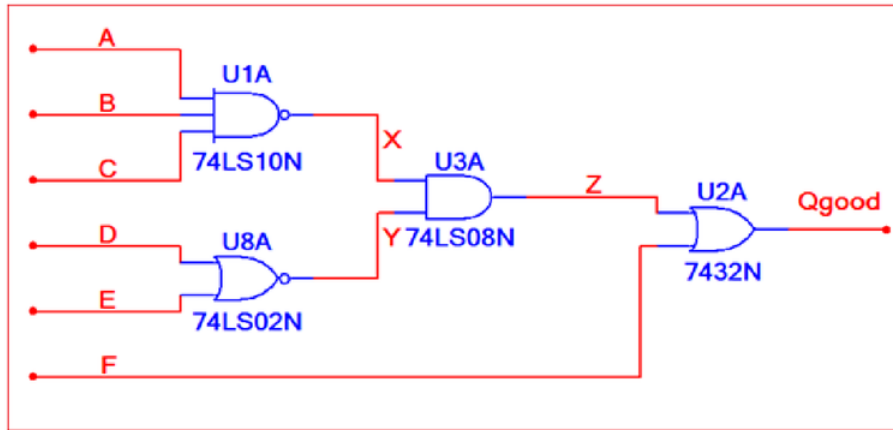


Figure 10: Multisim circuit with no faults

In order to model this circuit, it was necessary to place each fault condition in a truth table. Figure 11 shows this derived table, as well as the faults that could be detected. The single asterisk denotes that at least one of D or E or both must be at logic 1, while the double asterisk denotes that either A, B or C must be at logic 0.

Test No	A	B	C	D	E	F	Q good	HEX	X	Y	Z	Fault
1	1	1	1	0	0	0	0	70	0	1	0	A+B+C SA0 X SA1
2	0	1	1	0	0	0	1	31	1	1	1	A SA1
3	1	0	1	0	0	0	1	51	1	1	1	B SA1
4	1	1	0	0	0	0	1	61	1	1	1	C SA1
5	0*	0*	0*	0	0	0	1	01	1	1	1	D+E SA1 X+Y SA0, Z SA0
6	0*	0*	0*	1	0	0	0	08	1	0	0	D SA0
7	0*	0*	0*	0	1	0	0	04	1	0	0	E SA0
8	0*	0*	0*	0	0	0	1	01	1	1	1	X+Y SA0
9	1	1	1	0	0	0	0	70	0	1	0	X SA1
10	0*	0*	0*	1**	1** 0	0	0	0C	1	0	0	Y SA1
11	1	1	1	1**	1**	0	0	7C	0*	0*	0	F+Z SA1
12	1	1	1	1**	1**	1	1	7F	0*	0*	0	F SA0
13	0*	0*	0*	0	0	0	1	01	1	1	1	Z SA0

Figure 11: Derived table

Could have explained how each individual table has already been reduced using the formulae

The table clearly shows that for each AND or NAND gate, the input being tested remains at logic 1 whilst the others are set to logic 0. Conversely, the OR and NOR gates have the input at test set to logic 1 whilst the others are set to logic 0. This table can be further reduced by removing duplicate tests as shown in Figure 12.

Test No	A	B	C	D	E	F	Q good	HEX	X	Y	Z	Fault
1	1	1	1	0	0	0	0	70	0	1	0	A+B+C SA0 X SA1
2	0	1	1	0	0	0	1	31	1	1	1	A SA1
3	1	0	1	0	0	0	1	51	1	1	1	B SA1
4	1	1	0	0	0	0	1	61	1	1	1	C SA1
5	0* 1	0* 1	0*	0	0	0	1	01	1	1	1	D+E SA1 X+Y SA0, Z SA0
6	0*	0*	0*	1	0	0	0	08	1	0	0	D SA0
7	0*	0*	0*	0	1	0	0	04	1	0	0	E SA0
8	0*	0*	0*	1**	1** 0	0	0	0C	1	0	0	Y SA1
9	1	1	1	1**	1**	0	0	7C	0*	0*	0	F+Z SA1
10	1	1	1	1**	1**	1	1	7F	0*	0*	0	F SA0

Figure 12: Reduced table

Finally, the hexadecimal values can be checked, and any supplecates removed. Following the rules set out earlier as denoted by the asterisks, it is possible to alter test 5 to match test 4, and it is also possible to alter test 8 to match test 6. A and B were changed from logic 0 to logic 1 on test 5 to match, and E was changed from logic 1 to logic 0 on test 8 to match.

Figure 13 shows the table with all unnecessary tests removed. Seven tests remain, which is a significant amount lower than the number started with.

Test No	A	B	C	D	E	F	Q good	HEX	X	Y	Z	Fault
1	1	1	1	0	0	0	0	70	0	1	0	A+B+C SA0 X SA1
2	0	1	1	0	0	0	1	31	1	1	1	A SA1
3	1	0	1	0	0	0	1	51	1	1	1	B SA1
4	1	1	0	0	0	0	1	61	1	1	1	C SA1
5	0*	0*	0*	1	0	0	0	08	1	0	0	D SA0
6	0*	0*	0*	0	1	0	0	04	1	0	0	E SA0
7	1	1	1	1**	1**	0	0	7C	0*	0*	0	F+Z SA1
8	1	1	1	1**	1**	1	1	7F	0*	0*	0	F SA0

Figure 13: Final table

Good table reduction methods demonstrated. Good attention to detail.

With the fault vectors found, it was possible to build the circuit in multisim, as shown in Figure 14. In order to provide variable input to the circuit, piecewise voltage sources were used. These could be programmed to provide different outputs at different time intervals, a Qgood signal, corresponding with "output" in the previous tables; was also provided for comparison with the circuit. Finally, the xor gate shown would provide a pulse whenever the Qgood and Qtest differed.

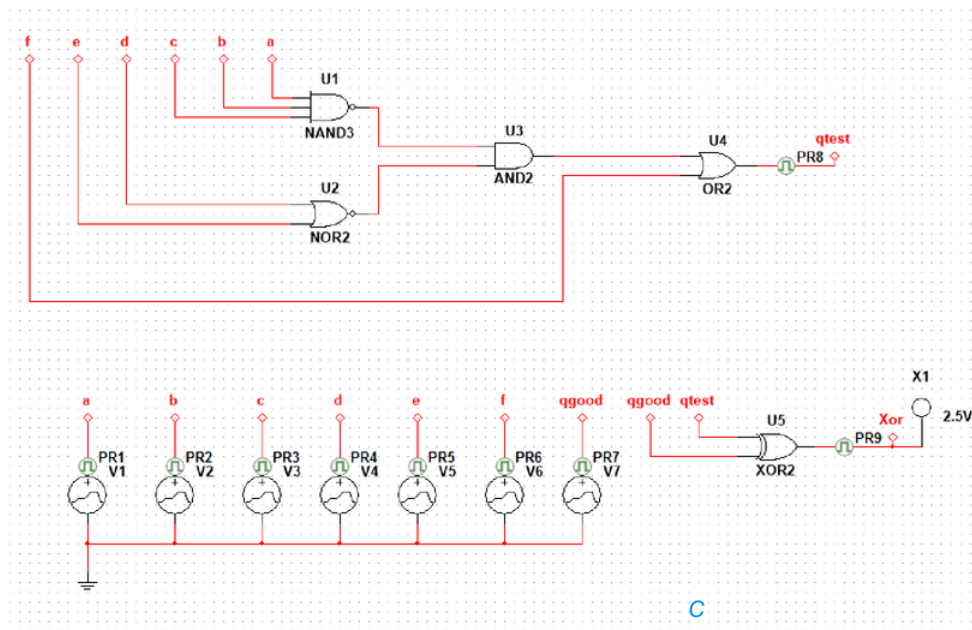
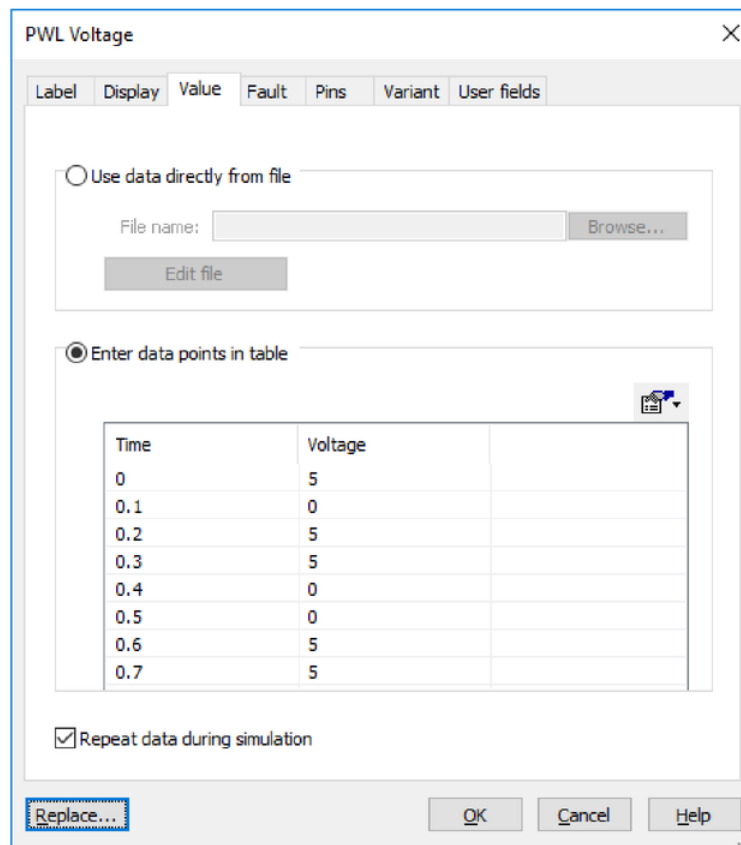


Figure 14: Test circuit

C
A
D
d
e
s
i
g
n
i

s
g
o
o
d
a
n
d
t
h
e
a
l
l
i
m
p
o
r

The piecewise settings for input “a” are shown in Figure 15. 5V represents a logic 1, and 0V represents logic 0. The variable changes once every 100mS, and then resets after 700mS. It can be clearly observed that this directly matches the truth table, and the same is true of all piecewise settings.



PWL Voltage

Label Display Value Fault Pins Variant User fields

☐ Use data directly from file

File name: Browse...

Edit file

☒ Enter data points in table

Time	Voltage
0	5
0.1	0
0.2	5
0.3	5
0.4	0
0.5	0
0.6	5
0.7	5

☒ Repeat data during simulation

Replace... OK Cancel Help

Good example of how the PLV was setup for the inputs.

Figure 15: Piecewise settings

In order to test the circuit, a transient analysis was used. The digital probes shown in the circuit would provide pulses in the graph. Figure 16 shows the test conducted with no fault present on the circuit. The output of the xor gate shown at the bottom proves that there are no faults as there are no pulses. There may be instantaneous pulses shown, but these may be due to miniscule time differences between the piecewise sources.

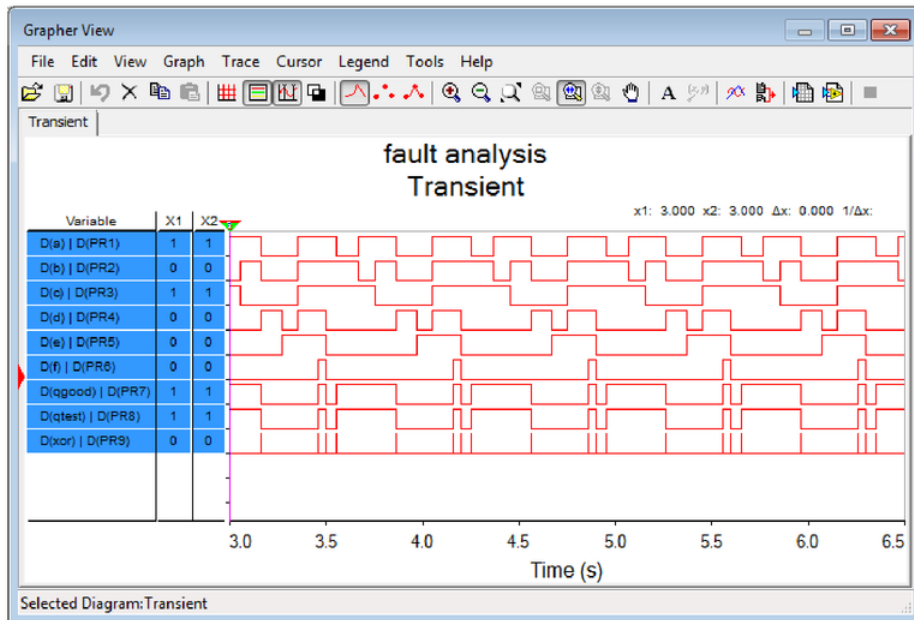


Figure 16: Test with no fault

Good analysis of this system.

The first fault tested was an A stuck at 0 fault. A logic constant was attached to pin a, and was set to 0 as shown in Figure 17. The result is shown in Figure 18, and it shows that a fault occurs when a, b and c are all logic 1, and the other inputs all remain at logic 0. Because Qtest and Qgood differ, a pulse is seen on the output of the xor gate.

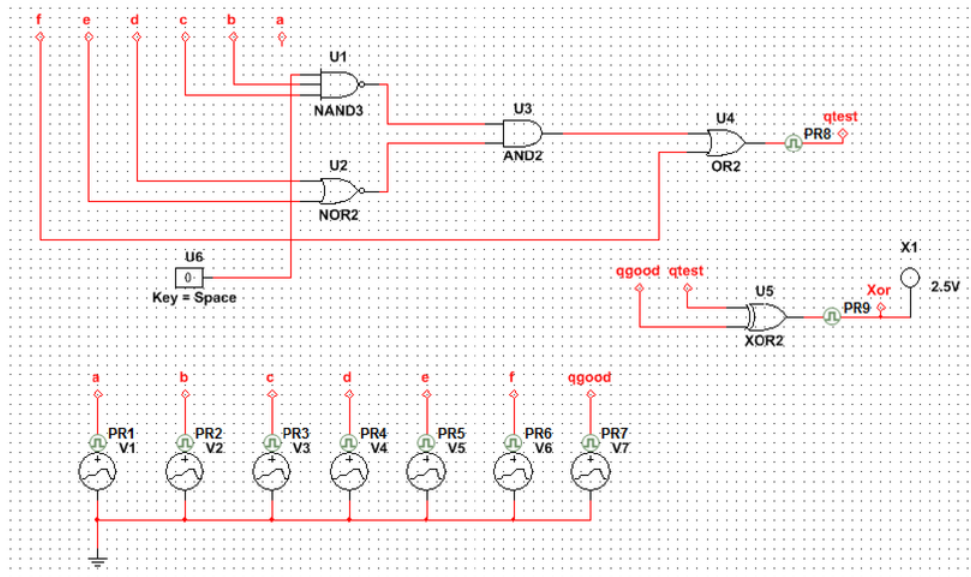


Figure 17: A tuck at 0 fault

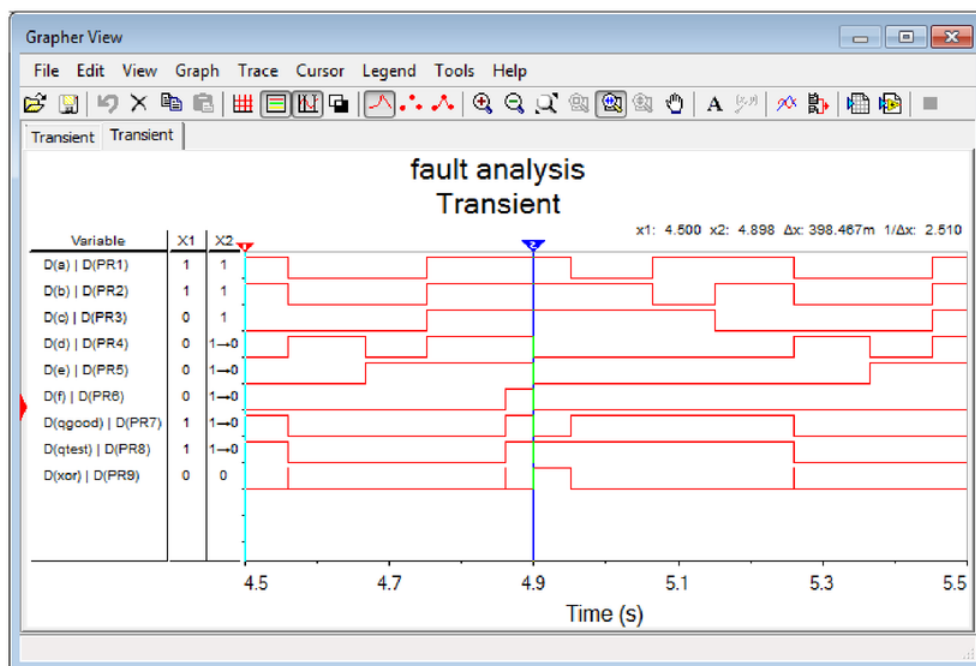


Figure 18: A stuck at 0 result

Analysis is clear and the cursors indicate the start and finish of the test interval

The second fault was F stuck at 1. The same setup was used as the first test, as shown in Figure 18. Figure 19 shows the result obtained for this test, and it can be seen that a fault occurs when input d is high and the others are low.

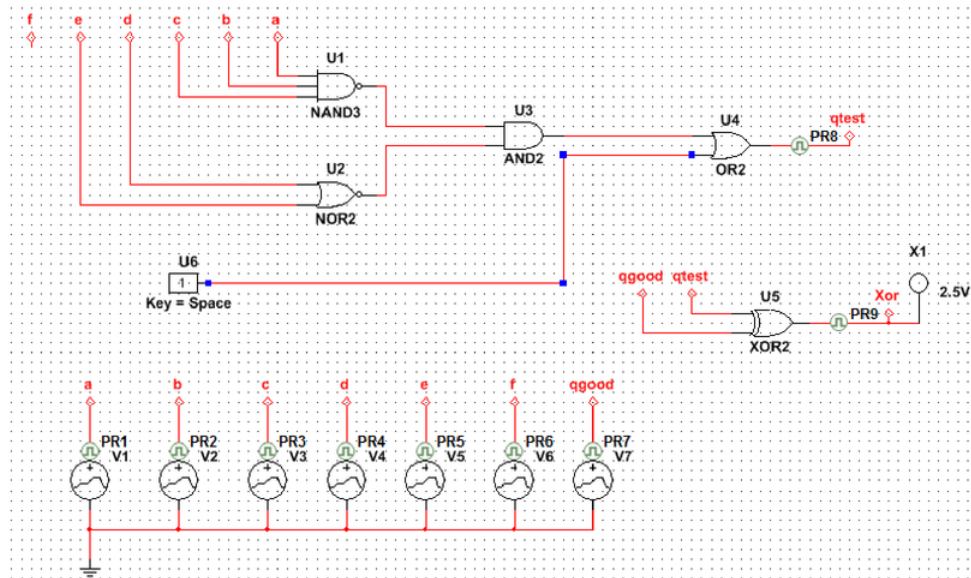


Figure 20: F stuck at 1 fault

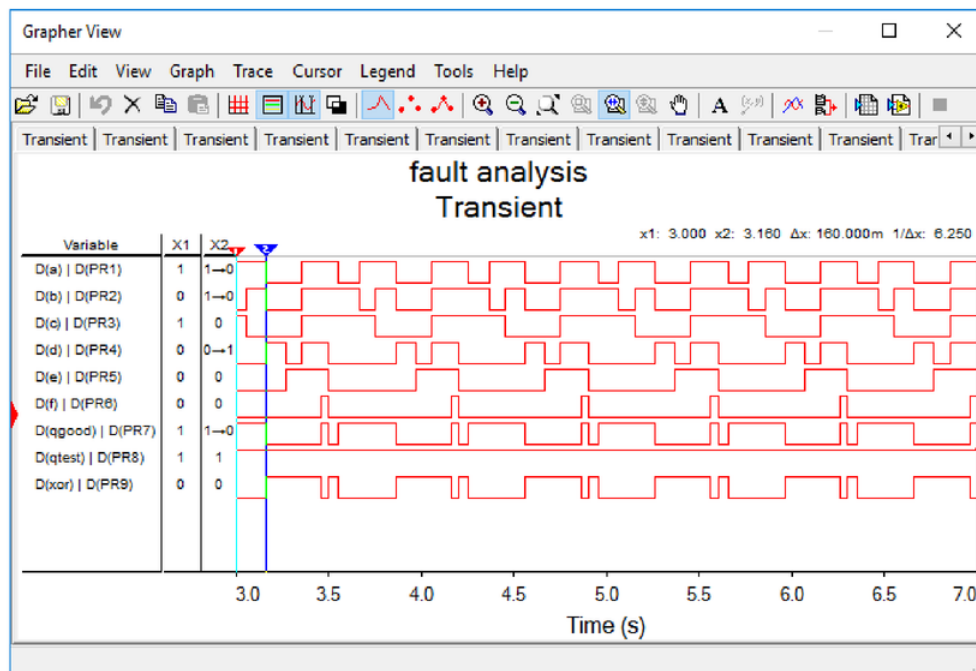


Figure 19: F stuck at 1 result

Finally, the third test was done with D stuck at 1 as shown in Figure 21. The results shown in Figure 22 demonstrate how a fault occurs when B, C and Qgood are high. The fault appears at the falling edge of input a, and the rising edge of Qgood.

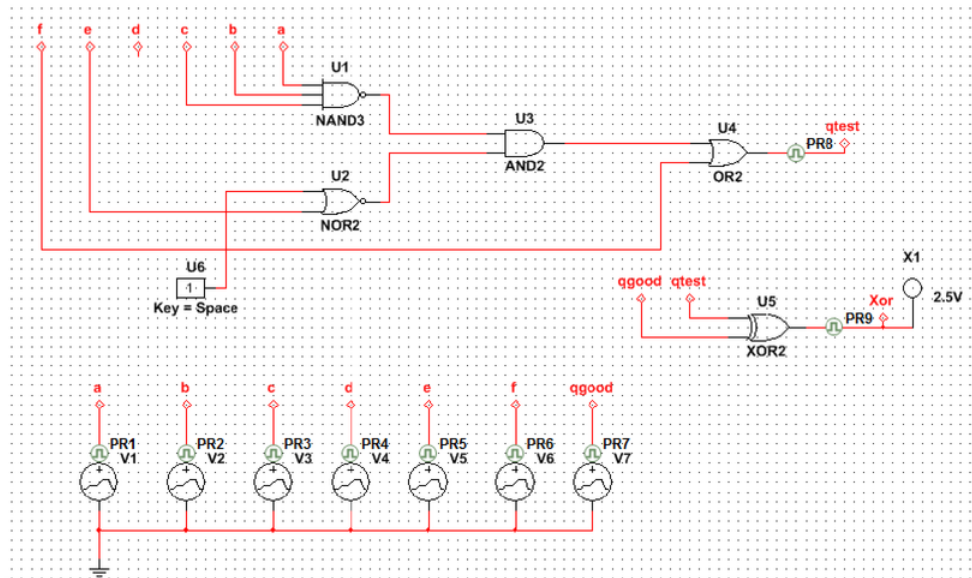


Figure 21: D stuck at 1 fault

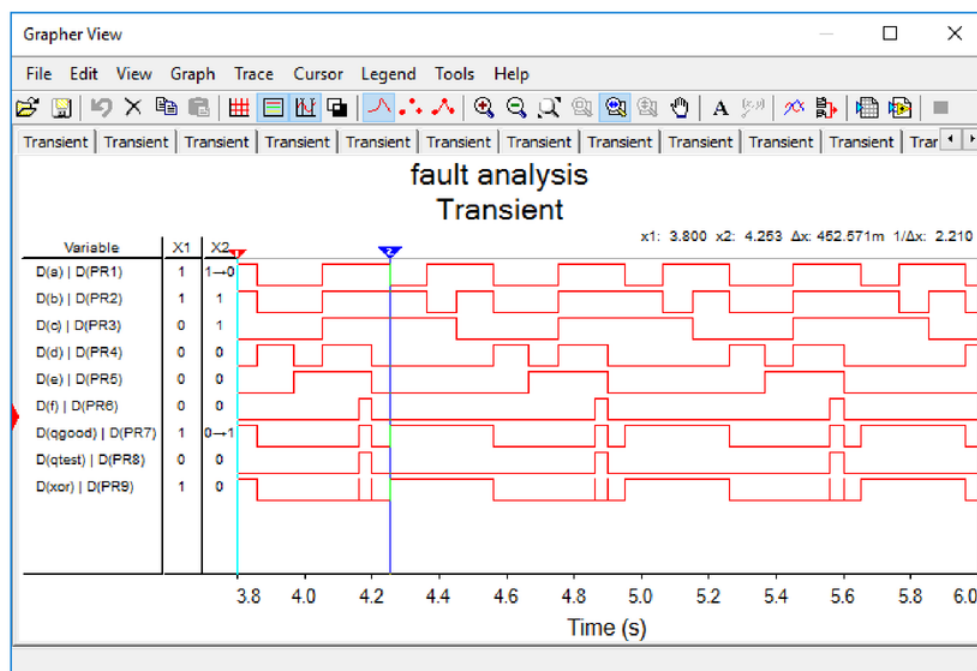


Figure 22: D stuck at 1 result

Good fault analysis. Fault conditions are clearly indicated.

The present and next states for each input are shown in Figure 23. These will be used as inputs and outputs for the D flip flops in the LFSR. These values are fed into karnaugh maps, which are used to derive Boolean expressions for each input.

A	B	C	D	E	F	A+	B+	C+	D+	E+	F+
1	1	1	0	0	0	0	1	1	0	0	0
0	1	1	0	0	0	1	0	1	0	0	0
1	0	1	0	0	0	1	1	0	0	0	0
1	1	0	0	0	0	0	0	0	1	0	0
0	0	0	1	0	0	0	0	0	0	1	0
0	0	0	0	1	0	1	1	1	1	1	0
1	1	1	1	1	0	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	0	0	0

Figure 23: Present and next states

For each karnaugh map, the present state values are at the edges, with the third and fourth values swapped in each quadrant. The next state values are fed into the middle, where they correspond with each row on the truth table above. Grouping occurs as normal. The first karnaugh map was for A+, as shown in Figure 24. The Boolean expression that was obtained for this input was as follows:

$$A \cdot B \cdot C \cdot D \cdot E + A \cdot NB \cdot C \cdot ND \cdot NE \cdot NF + NA \cdot B \cdot C \cdot ND \cdot NE \cdot NF + NA \cdot NB \cdot NC \cdot ND \cdot E \cdot NF$$

	ABC							
DEF	000	001	011	010	100	101	111	110
000			1			1		
001								
011								
010	1							
100								
101								
111							1	
110							1	

Figure 24: A+ Karnaugh map

The B+ karnaugh map is shown in Figure 25. The following expression was derived:

$$A.C.ND.NE.NF + A.B.C.D.E + NA.NB.NC.ND.E.NF$$

	ABC							
DEF	000	001	011	010	100	101	111	110
000						1	1	
001								
011								
010	1							
100								
101								
111							1	
110							1	

Figure 25: B+ karnaugh map

The C+ karnaugh map has been shown in Figure 26. The Boolean expression derived is as follows:

$$NA.B.C.ND.NE.NF + A.B.C.ND.NE.NF + A.B.C.D.E + NA.NB.NC.ND.E.NF$$

	ABC							
DEF	000	001	011	010	100	101	111	110
000			1				1	
001								
011								
010	1							
100								
101								
111							1	
110							1	

Figure 26: C+ karnaugh map

The D+ karnaugh map is shown in Figure 27, with the following Boolean expression derived:

$$NA.NB.NC.ND.E.NF + A.B.NC.ND.NE.NF + A.B.C.D.E.NF$$

	ABC							
DEF	000	001	011	010	100	101	111	110
000								1
001								
011								
010	1							
100								
101								
111								
110							1	

Figure 27: D+ karnaugh map

The E+ karnaugh map has been included in Figure 28. The following expression has been derived:

$$NA.NB.NC.ND.E.NF + NA.NB.NC.D.NE.NF + A.B.C.D.E.NF$$

	ABC							
DEF	000	001	011	010	100	101	111	110
000								
001								
011								
010	1							
100	1							
101								
111								
110							1	

Figure 28: E+ karnaugh map

Figure 29 shows the F+ karnaugh map. The expression derived is as follows:

$$A.B.C.D.E.NF$$

	ABC							
DEF	000	001	011	010	100	101	111	110
000								
001								
011								
010								
100								
101								
111								
110							1	

Figure 29: F+ karnaugh map

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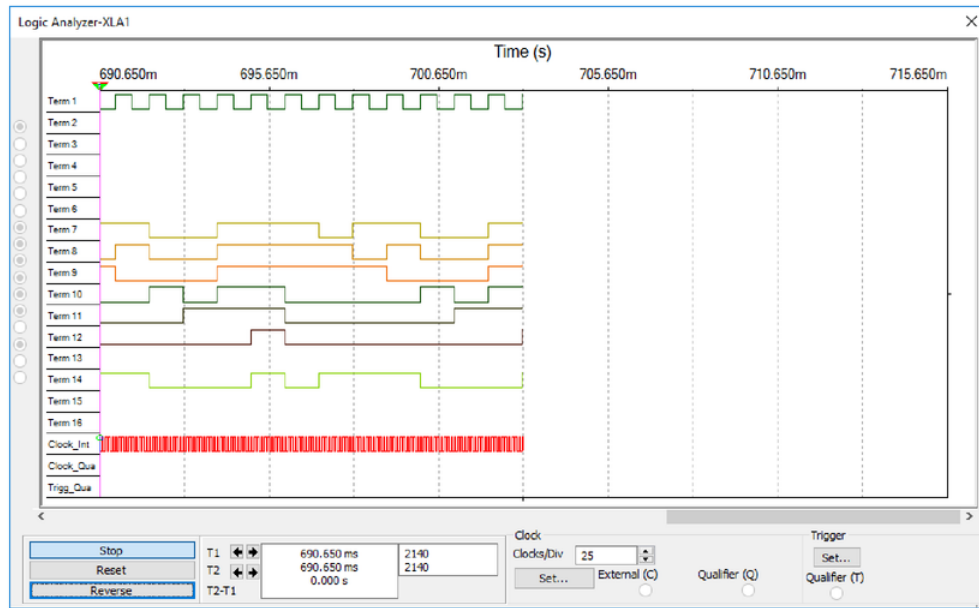


Figure 31: Equivalent circuit results

Good analysis for the pattern generator. Could have indicated i.e. labelled the 8 test vectors.

4. Analysis of NI Multisim Results

With all of the multisim results obtained, the results can be fed into the table shown in Figure 32. This table shows the logic analyser results obtained from both the simulated circuit and the PID circuit, and they are both identical. This is proof that the circuit works as intended, and that the fault modelling methods were successful.

Input	A	B	C	D	E	F
Simulated	1	1	1	0	0	0
	0	1	1	0	0	0
	1	0	1	0	0	0
	1	1	0	0	0	0
	0	0	0	1	0	0
	0	0	0	0	1	0
	1	1	1	1	1	0
	1	1	1	1	1	1
PID	1	1	1	0	0	0
	0	1	1	0	0	0
	1	0	1	0	0	0
	1	1	0	0	0	0
	0	0	0	1	0	0
	0	0	0	0	1	0
	1	1	1	1	1	0
	1	1	1	1	1	1

Figure 32: multisim results

The
results
are
correct
. Good

use of
the
table
for
compa
rison.

5. Practical Build and Test Using LabView

In order to carry out a separate practical test for comparison, it was necessary to create a file in LabView. This would be connected to the NI Elvis board where the IO could be used to interact with a logic circuit built on breadboard. The circuit is shown in Figure 33 with no faults applied. The pins of each IC have been connected to the appropriate IO on the Elvis board.

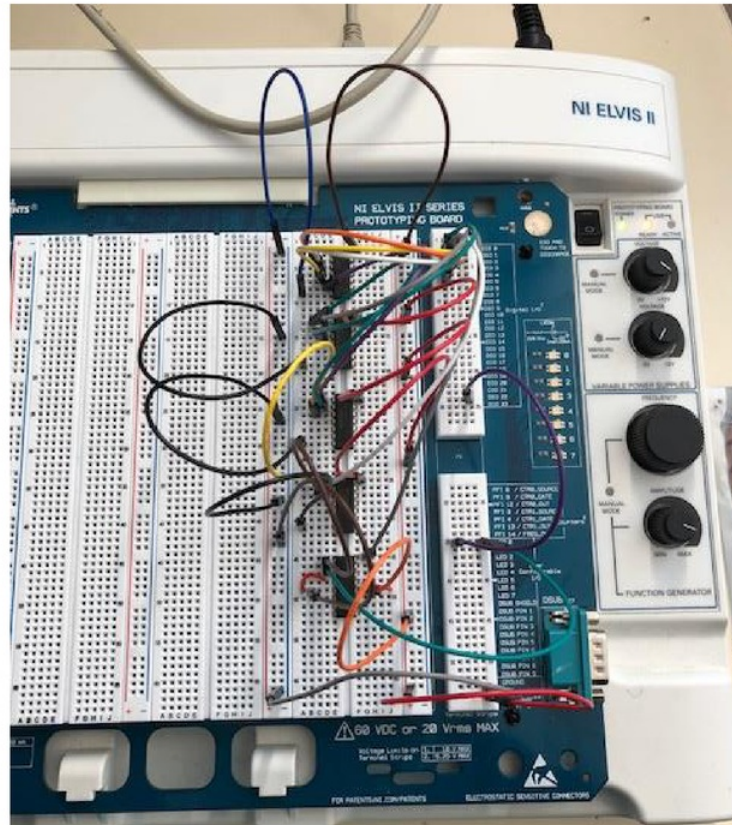
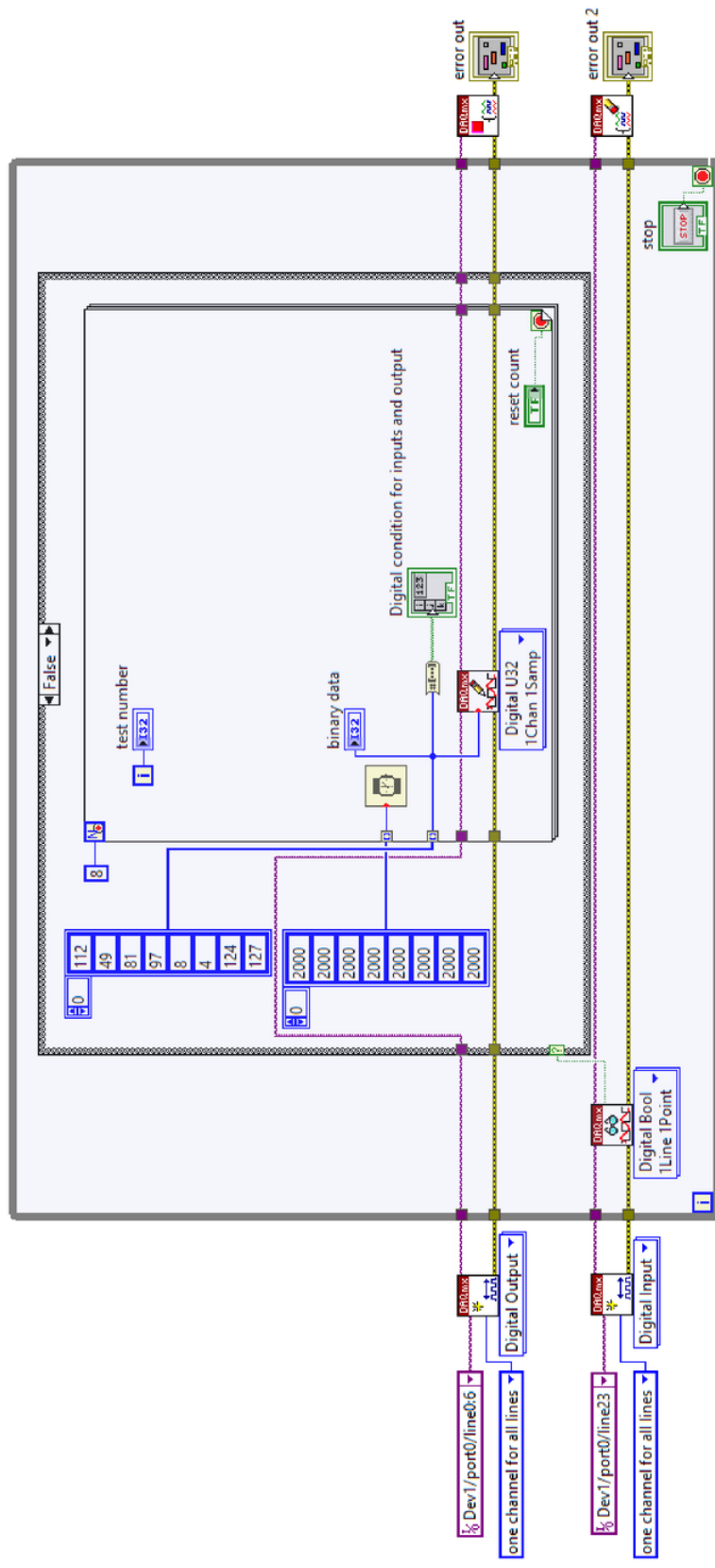


Figure 33: Logic circuit on breadboard

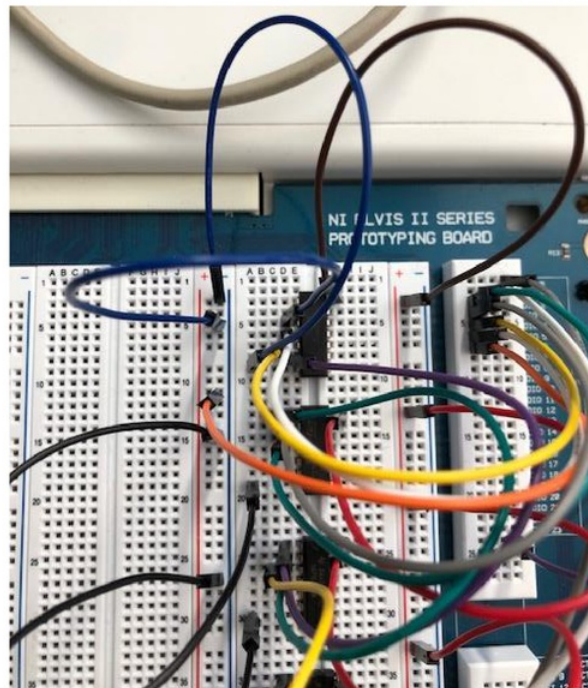
Figure 34 shows the block diagram in the Labview program. The while loop is the solid grey block, and this continues program operation until it is stopped by the user. Inside, there is a conditional loop represented by the criss-crossed pattern, whose behaviour will be determined by its state. The state is controlled by a Boolean input. The contents of the false state provide the eight binary outputs for the logic circuit. These are fed into a write program block to send the value to the Elvis IO pins. A Boolean array is used to provide a display on the labview front panel. An iterative loop has been used to control which value is sent at a time, and a 2 second timer determines the rate at which each loop lasts.



Good program analysis and explanation.

Figure 34: Labview block diagram

The same faults were introduced as in the simulation. First Figure 35 shows the A stuck at 0 fault, and the result is shown in Figure 36. The fault lamp is high when A, B and C are at logic 1, which corresponds with the simulation.



Clear image which identifies the CUT on ELVIS development board.

Figure 35: A stuck at 0 fault

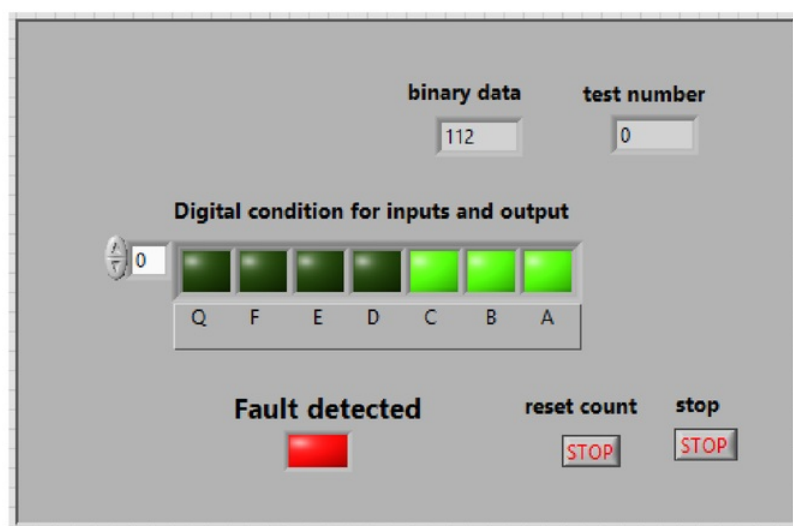


Figure 36: A stuck at 0 result

The second test, done with F stuck at 1, is show in Figure 38. The result in Figure 37 shows that a fault occurs when D is logic 1. This again corresponds with the simulation.

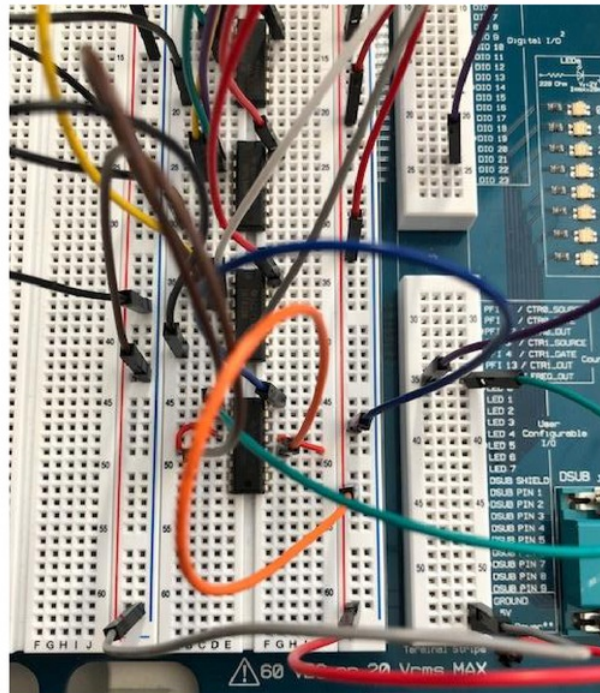


Figure 38: F stuck at 1 fault

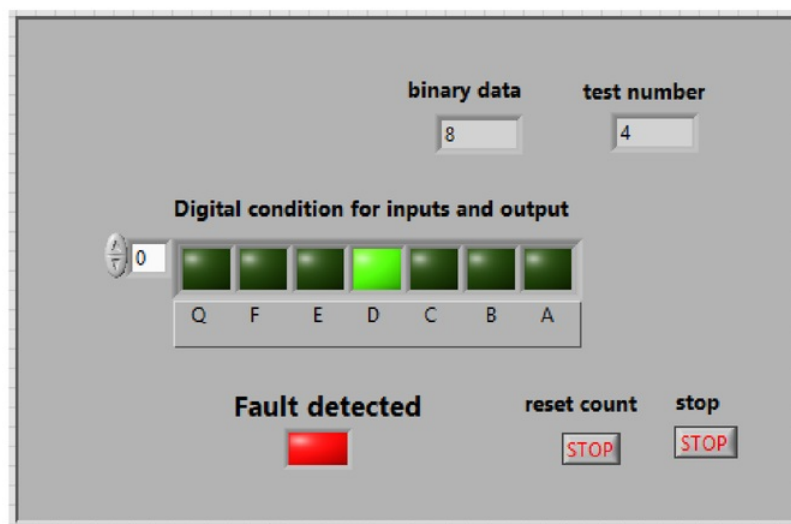


Figure 37: F stuck at 1 result

The final fault, shown in Figure 40, was done with D stuck at 1. The result shown in Figure 39, and occurs when Q, C and B are high. This corresponds with the simulation as with the other two tests.

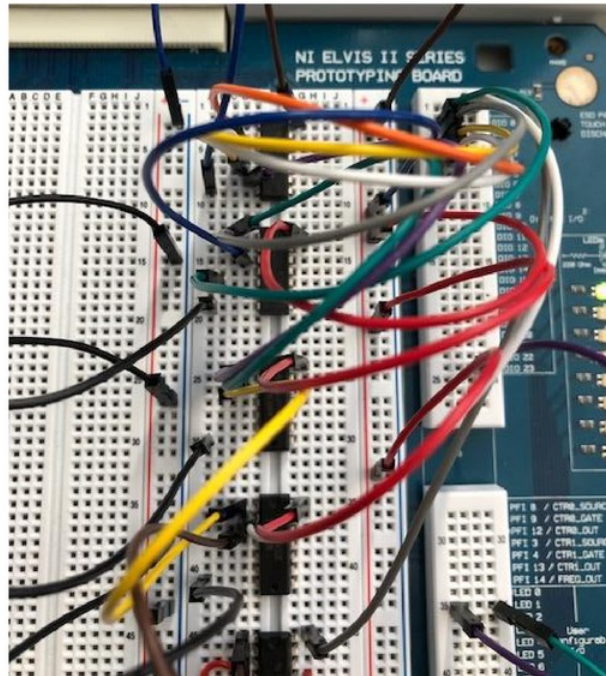


Figure 40: D stuck at 1 fault

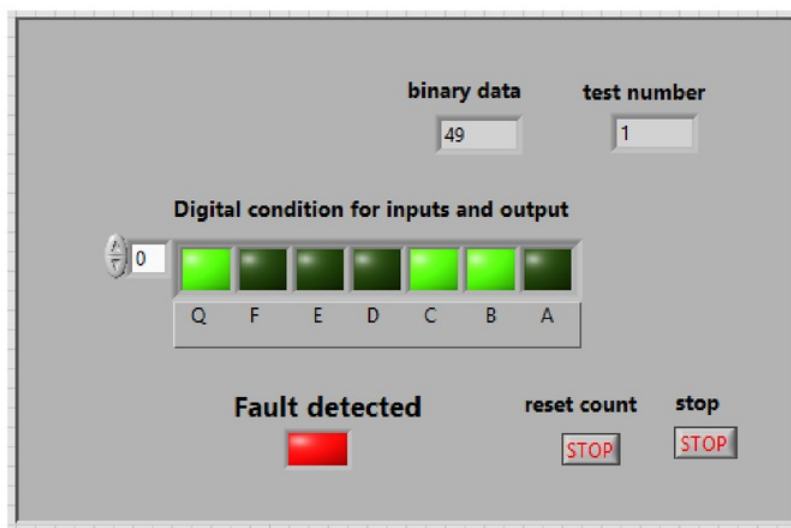


Figure 39: D stuck at 1 result

6. Conclusions and Recommendations

In conclusion, there has been a good amount of correlation between the results. The simulated and practical results provide sufficient evidence that the single stuck at fault modelling techniques are an effective form of circuit testing. The simulated circuit proved that the derivation of the fault vectors was effective in reducing the number of tests required, while the PID test reaffirmed the results obtained from the simulation.

Research into the relevant topics provided a greater insight into how faults could be introduced to a system, as well as the effect of ESD on delicate ICs. The fault modelling techniques had also been researched, which made the process easier for the assignment circuit.

The LabView tests were performed as further proof that the techniques were effective, with the same faults being tested as the simulation. The results were conclusive in demonstrating how the two methods obtained the same results.

Test	Simulated result	Practical result
A s@0	A,B,C fault	A,B,C fault
F s@1	D fault	D fault
D s@1	Q,B,C fault	Q,B,C fault

Figure 41: Results comparison

A recommendation for the future would be to use an FPGA to simulate a larger circuit. This could prove the effectiveness of single stuck at modelling, and how time can be saved by reducing the number of tests required.

*Reasonable
conclusion.
How effective
is the fault
model method
for larger
circuits? How
much does the
model save on
time and
process?*

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Assignment 1 - final

GRADEMARK REPORT

FINAL GRADE

GENERAL COMMENTS

Instructor

68/100

PAGE 1

PAGE 2

PAGE 3

Text Comment. Good list of contents

PAGE 4

PAGE 5

PAGE 6

PAGE 7

Text Comment. Good example of fault modelling.

PAGE 8

PAGE 9

Text Comment. Good use of table for examples.

PAGE 10

Text Comment. Reasonable amount of research with appropriate sources.

PAGE 11

Text Comment. Could have explained how each individual table has already been reduced using the formulae.

PAGE 12

Text Comment. Good table reduction methods demonstrated. Good attention to detail.

PAGE 13

Text Comment. CAD design is good and the all important x-or gate is included. The PLV logic shows innovation.

PAGE 14

Text Comment. Good example of how the PLV was setup for the inputs.

PAGE 15

Text Comment. Good analysis of this system.

PAGE 16

Text Comment. Analysis is clear and the cursors indicate the start and finish of the test vectors.

PAGE 17

PAGE 18

Text Comment. Good fault analysis. Fault conditions are clearly indicated.

PAGE 19

PAGE 20

PAGE 21

Text Comment. Good effort with the k_maps and the use of the mirror method.

PAGE 22

Text Comment. Should have included the x-or gate here.

PAGE 23

Text Comment. Good analysis for the pattern generator. Could have indicated i.e. labelled the 8 test vectors.

PAGE 24

Text Comment. The results are correct. Good use of the table for comparison.

PAGE 25

PAGE 26

Text Comment. Good program analysis and explanation.

Text Comment. Clear image which identifies the CUT on ELVIS development board.

Text Comment. Good implementation and analysis of Labview with DAQMX system. The fault analysis is clear.

Text Comment. Reasonable conclusion. How effective is the fault model method for larger circuits? How much does the model save on time and process?

Text Comment. Good relevant sources.

GRADING FORM: CSG-RUBIC

JAMES DAVIES

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RESEARCH-INFORMED LITERATURE



Research is good. Some key points are not there such as types of SA faults. IC fabrication - 2.5/5
ESD - 3.5/5 SAF - 3/5

9/15

KNOWLEDGE AND UNDERSTANDING



Understanding is clearly demonstrated. Minimum test vectors have been derived for the design. - 7/10
LabVIEW design is good with good explanation of the design function - 7.5/10
ECAD design and

21/30

ANALYSIS



Analysis covers most aspects. Minor points left out such as individual gate models. ECAD testing for the design is good and proven - 7.5/10 Comparison to theory is clear and in a logical sequence. 3.5/5

11/15

PRACTICAL APPLICATION AND DEP.



Practical application has been applied very well with good explanations. Could have indicated the 8 test vectors in Labview using DAQMX. Prototyping of test circuit is good - 7/10 LabVIEW application is good - 11/15

18/25

SKILLS FOR PROFESSIONAL PRAC.



Report is good. Use of appropriate media - good 3/5 Report layout is good - 3/5 Conclusion is reasonable, could have included the alternative PLD against LabVIEW comparison - 3/5

9/15