

LEVEL 4 ASSESSMENT SPECIFICATION

Student name:	Maia Hough	Student ID number:	
Programme:	HNC Electrical/Electronic Engineering		
Module:	Electronics		
Module code:	PCEE4006	Contribution to Overall Module Assessment (%):	50%
Lecturer:	Jason Pointer	Internal Verifier:	Nigel Richards
Assignment Title:	Digital Systems	Word count (or equivalent):	2000
Submission deadline:	11/05/23	Return date of provisional marks & written feedback:	25/05/23
Submission method:	All written assessments, where practical and possible, must be submitted via Turnitin unless otherwise instructed by the Lecturer. (Please DO NOT put this assessment specification into Turnitin or it will match many similarities with other students' submissions.) Alternative submission method (if applicable): Late submission of the assessment will result in a late penalty mark. Penalties for late submission: Up to one week late, maximum mark of 40%. Over one week late, 0%. Only the Extenuating Circumstances Panel may approve a change to submission dates.		
Academic honesty / referencing:	Academic honesty is required. In the main body of your submission you must give credit to authors on whose research and ideas your work is based. Append to your submission a reference list that indicates the books, articles, etc. that you have used, cited or quoted in order to complete this assessment.		

Module Learning Outcomes (from module syllabus)

1. Demonstrate an understanding of semi-conductor components and characteristics and their application in analogue and **digital** electronic circuits.
2. To design, simulate, build, test and evaluate analogue and **digital** electronic circuits using information gained from datasheets.

STUDENT FEEDBACK FORM

This section details the *extent* to which the assessment criteria are demonstrated by you, which in turn determines your mark. The marks available for each category of skill are shown. Lecturers will use the space provided to comment on the achievement of the task(s), including those areas in which you have performed well and areas that would benefit from development/improvement.

Generic Assessment Criteria	Marks available	Marks awarded
1. Engagement with Literature Skills	10	3.5
Poor engagement with essential reading, there are a few text books listed. No evidence of wider reading and reliance on inappropriate sources. Inconsistent and weak use of referencing.		
2. Knowledge and Understanding Skills	45	21.8
Task 1 & 2 achieved 42%. Task 3 & 4 achieved 55%. Limited knowledge and understanding for some of the basic underlying concepts and principles within digital systems. Showed a good understanding of logic gates and counter design but there were issues with some of the Boolean algebra.		
3. Cognitive and Intellectual Skills	10	4
Some evidence to support emerging arguments and judgements but in some places they are underdeveloped.		
4. Practical Application Skills	25	16.9
Task 1 & 2 achieved 70%. Task 3 & 4 achieved 65%. Some good application of practical work for all tasks, generally good use of the Multisim to obtain the required test results.		
5. Transferable Skills for Life and Professional Practice	10	4
Fairly coherent, organised and accurate work, in a suitable structure and is for the most part clearly expressed.		

Assessment Mark (Assessment marks are subject to ratification at the Exam Board. These comments and marks are to give feedback on module work and are for guidance only until they are confirmed.)

Late Submission Penalties (tick if appropriate)

Up to 1 week late (40% Max)

Over 1 week late (0%)

50%

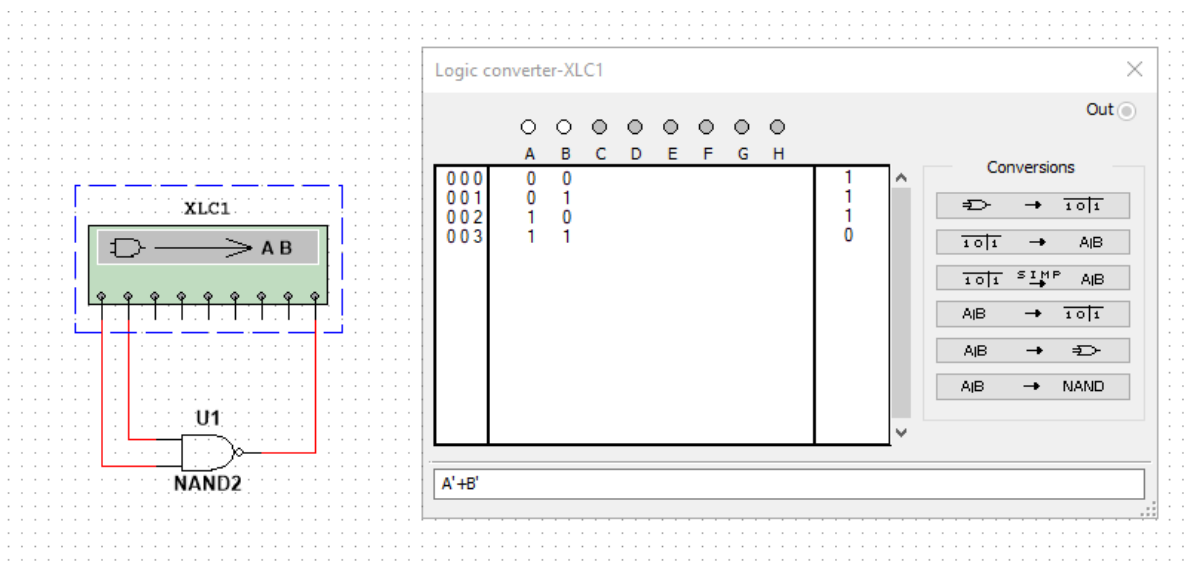
Assignment 2 PCEE4006 Electronics for Jason Pointer

1(a)

A	B	X
0	0	1
0	1	1
1	0	1
1	1	0

' = NOT

$$X = 'A.'B + 'A.B + A.'B = ('A.(B+'B)) + ('B.(A+'A)) = 'A.1 + 'B.1 = 'A+'B = \overline{A.B}$$

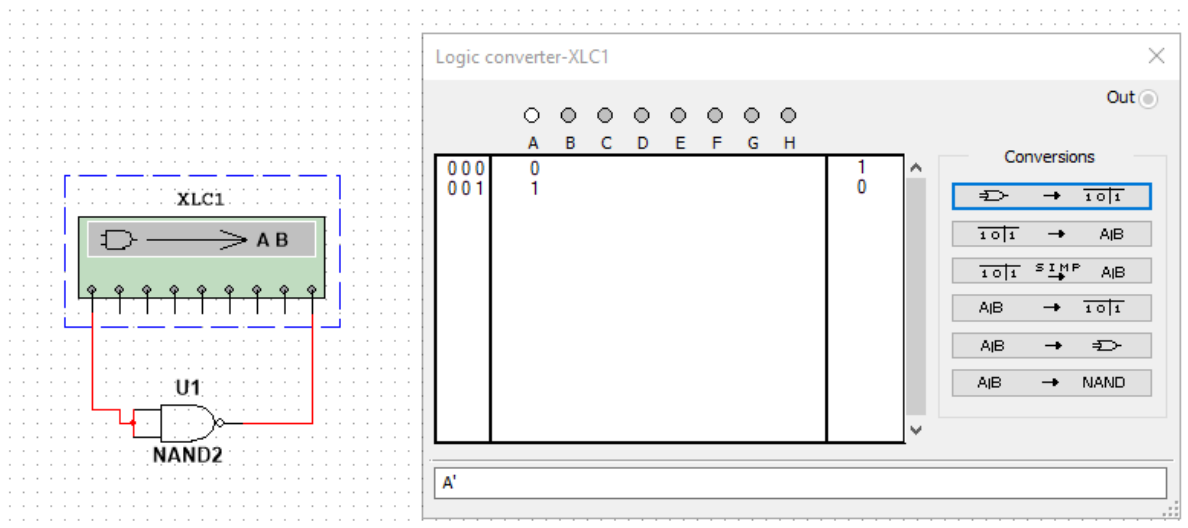


Multisim confirms predicted Boolean expression is correct.

1(b)

A	X
0	1
1	0

$$X = A'$$



Multisim confirms predicted Boolean expression is correct.

1(c)

A	B	C	W	X	Y
0	0	0	0	1	0
0	0	1	0	1	0
0	1	0	0	1	0
0	1	1	0	1	0
1	0	0	0	1	0
1	0	1	0	1	0
1	1	0	1	1	0
1	1	1	1	0	1

$$Y = A.B.C$$

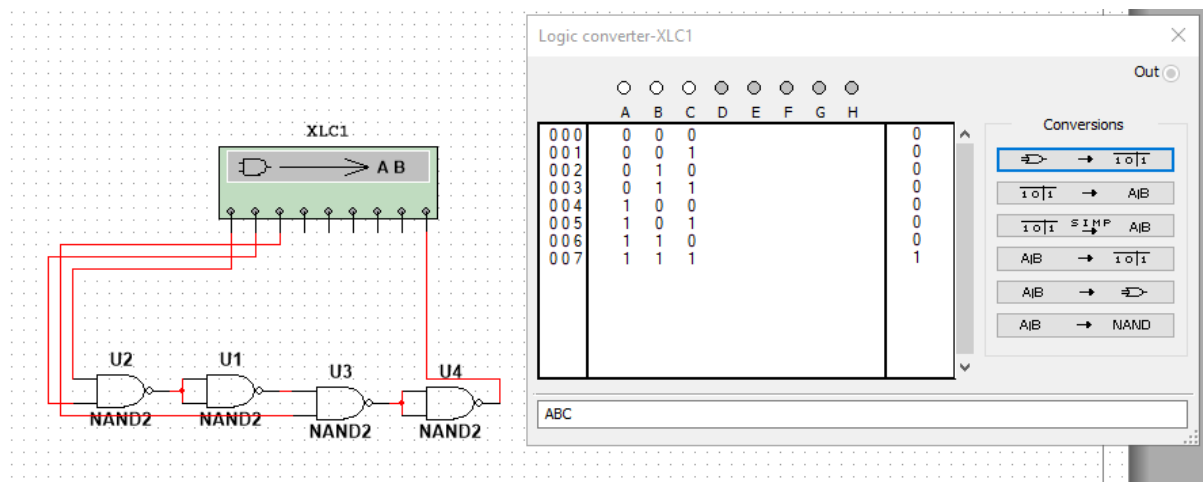
This is a 3 input AND gate

$$X = (A.B.C)'$$

This is a 3 input NAND gate

$$W = A.B$$

This a 2 input AND gate



Multisim confirms predicted Boolean expression is correct.

1(d)

A	B	C	M	N	P	Q
0	0	0	0	1	1	1
0	0	1	0	1	0	1
0	1	0	0	1	1	1
0	1	1	0	1	0	1
1	0	0	0	1	1	1
1	0	1	0	1	0	1
1	1	0	1	0	1	1
1	1	1	1	0	0	0

$$Q = 'A.'B.'C + 'A.'B.C + 'A.B.'C + 'A.B.C + A.'B.'C + A.'B.C + A.B.'C$$

$$Q = ('A.'B.(C+'C)) + 'A.B.C + (A.'B.('C+C)) + ((A+'A).B.'C$$

$$Q = ('A.'B.1) + (A.'B.1) + (1.B.'C) + ('A.B.C)$$

$$Q = ((A+A).'B) + (B.'C) + ('A.B.C)$$

$$Q = 'B + B.'C + 'A.B.C$$

OR

$$Q = 'A.'B.'C + 'A.'B.C + 'A.B.'C + 'A.B.C + A.'B.'C + A.'B.C + A.B.'C$$

$$Q = ('A.'B.(C+'C)) + ('A.B.('C+C)) + (A.'C.('B+B))$$

$$Q = ('A.'B.1) + ('A.B.1) + (A.'C.1)$$

$$Q = ('A.('B+B)) + (A.'C)$$

$$Q = 'A + A.'C$$

Looks more 'right'

OR

$$Q = 'A.'B.'C + 'A.'B.C + 'A.B.'C + 'A.B.C + A.'B.'C + A.'B.C + A.B.'C$$


$$Q = A + 'A.C$$

Not completed.

	A	B	C	D	Q
0	0	0	0	0	0
1	0	0	0	1	0
2	0	0	1	0	0
3	0	0	1	1	0
4	0	1	0	0	0
5	0	1	0	1	0
6	0	1	1	0	0
7	0	1	1	1	0
8	1	0	0	0	0
9	1	0	0	1	0
10	1	0	1	0	1
11	1	0	1	1	1
12	1	1	0	0	1
13	1	1	0	1	1
14	1	1	1	0	1
15	1	1	1	1	1

1f BCD

$$Q = (A \cdot \bar{B} \cdot C \cdot (\bar{D} + D)) + (A \cdot B \cdot \bar{C} \cdot (\bar{D} + D)) + (A \cdot B \cdot C \cdot (\bar{D} + D))$$

$$Q = (A \cdot \bar{B} \cdot C) + (A \cdot B \cdot (\bar{C} + C)) \quad Q = (A \cdot C + (\bar{B} + B)) + (A \cdot B \cdot \bar{C})$$

$$Q = (A.B) + (A.\bar{B}.C)$$

Figure 1. The effect of the concentration of the *Agrobacterium* suspension on the transformation efficiency of *Agrobacterium* strains.

Logic converter-XLC1

Out ☐

	☐ A	☐ B	☐ C	☐ D	☒ E	☒ F	☒ G	☒ H	
003	0	0	1	1					0
004	0	1	0	0					0
005	0	1	0	1					0
006	0	1	1	0					0
007	0	1	1	1					0
008	1	0	0	0					0
009	1	0	0	1					0
010	1	0	1	0					1
011	1	0	1	1					1
012	1	1	0	0					1
013	1	1	0	1					1
014	1	1	1	0					1
015	1	1	1	1					1

Conversions

- ☐ $\rightarrow \overline{1\ 0\ 1}$
- $\overline{1\ 0\ 1} \rightarrow A/B$
- $\overline{1\ 0\ 1} \xrightarrow{\text{IMP}} A/B$
- $A/B \rightarrow \overline{1\ 0\ 1}$
- $A/B \rightarrow \text{XOR}$
- $A/B \rightarrow \text{NAND}$

$AB'CD' + AB'CD + ABC'D' + ABCD' + ABCD$

Multisim output simplified Boolean expression

Logic converter-XLC1

Out ☐

Conversions

$\Rightarrow$ $\rightarrow$ $\overline{101}$

$\overline{101}$ $\rightarrow$ $A|B$

$\overline{101}$ **SIMP** $A|B$

$A|B$ $\rightarrow$ $\overline{101}$

$A|B$ $\rightarrow$ $\Rightarrow$

$A|B$ $\rightarrow$ NAND

AB+AC

Multisim circuit output from simplified Boolean expression

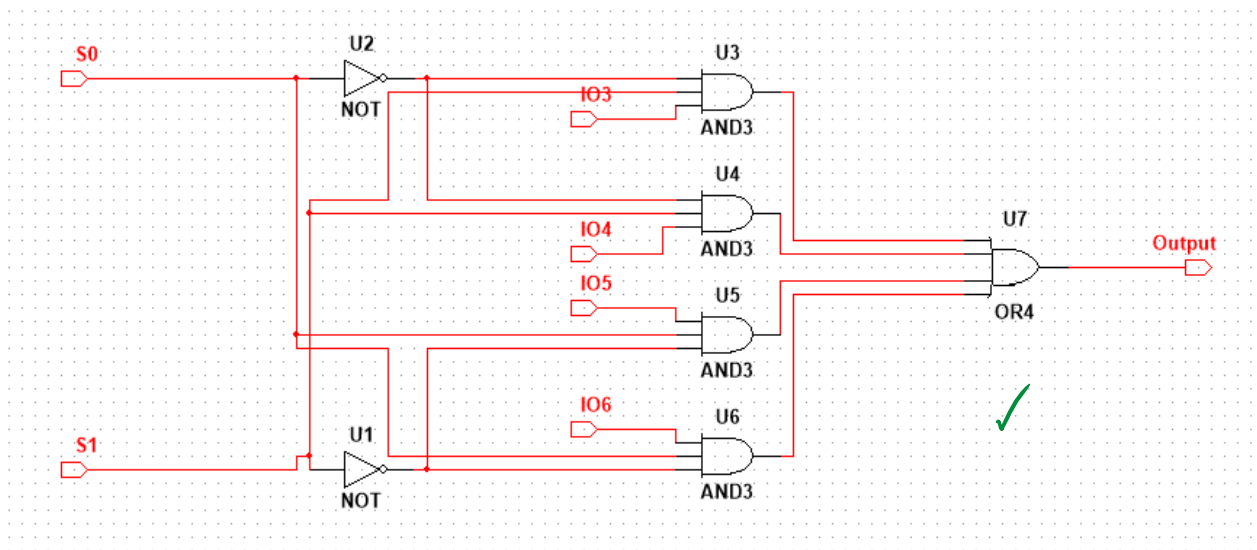
The benefits of using NAND gate only circuits include: using one component means no time wasted ordering, sorting, separating, finding different components; mass production of one component drives up supply and costs down; any circuit can be taken apart and reconstituted or altered by anybody as everybody knows what the components are; money saved on time; easy automation of design.

Multiplexer Truth Table		
Input Selectors		Output at Q
S1	S2	Q
0	0	Input 0
0	1	Input 1
1	0	Input 2
1	1	Input 3

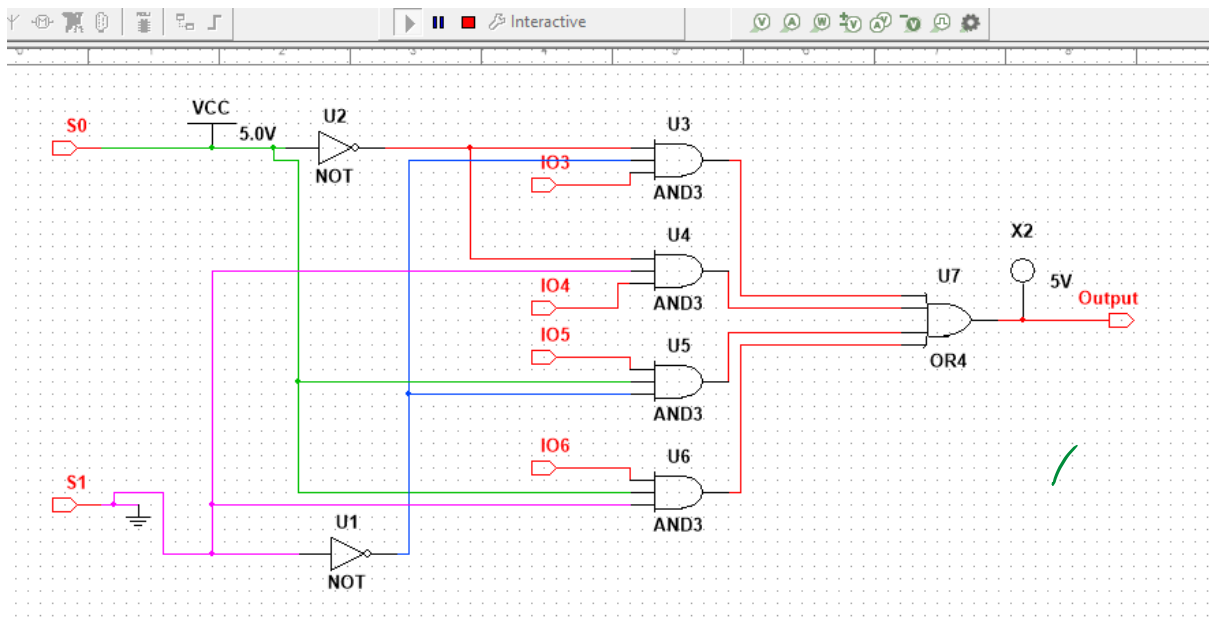
Boolean equation:

$$\text{Output} = ('S1.'S2 = I0) + ('S1.S2 = I1) + (S1.'S2 = I2) + (S1.S2 = I3)$$

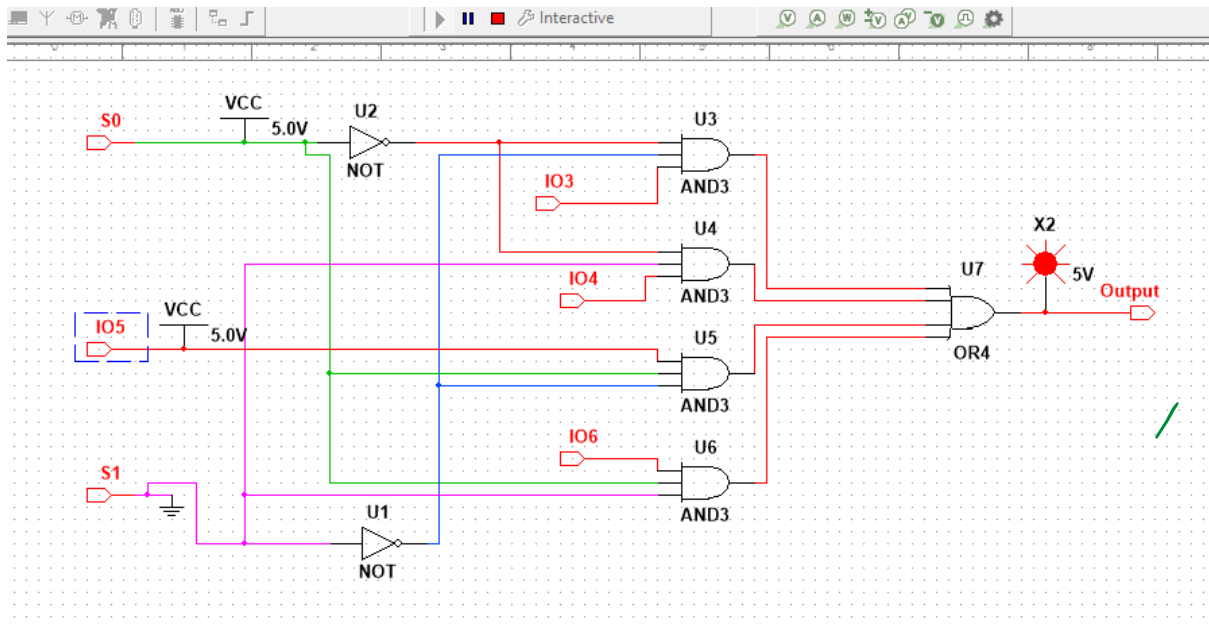
Multiplexer design using logic gates in Multisim.



Multiplexer simulation showing no input so no output (probe off).

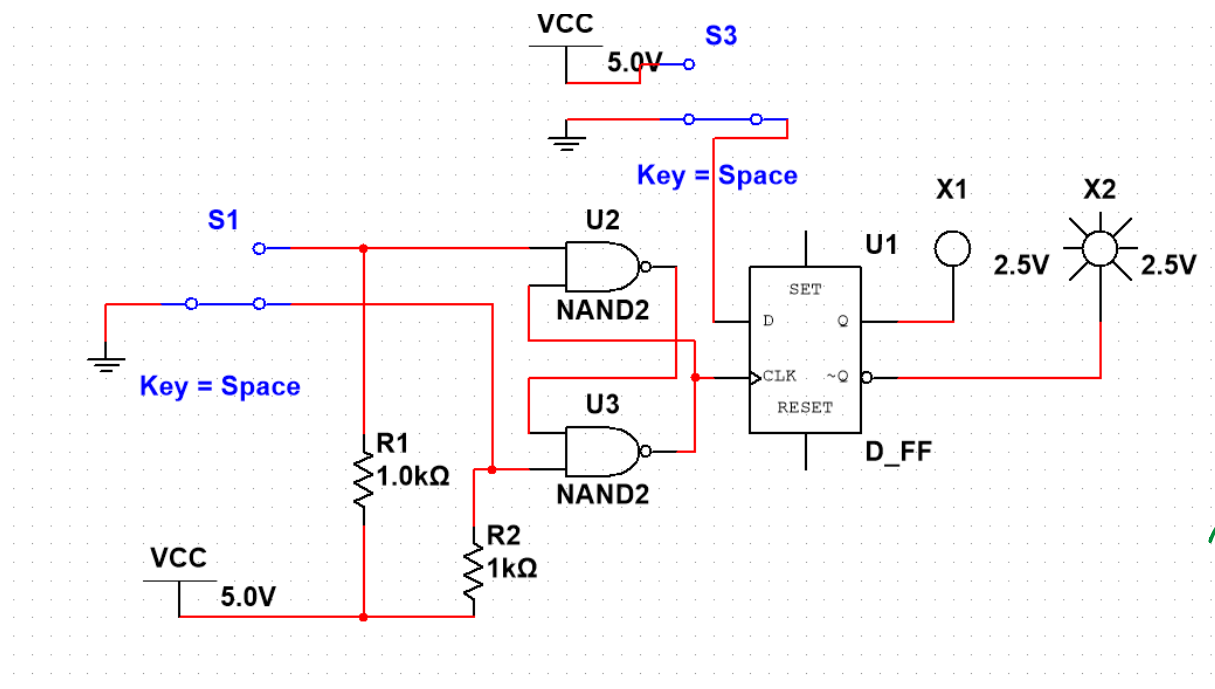


Multiplexer simulation showing live input matching selection conditions (S0 live S1 zero).

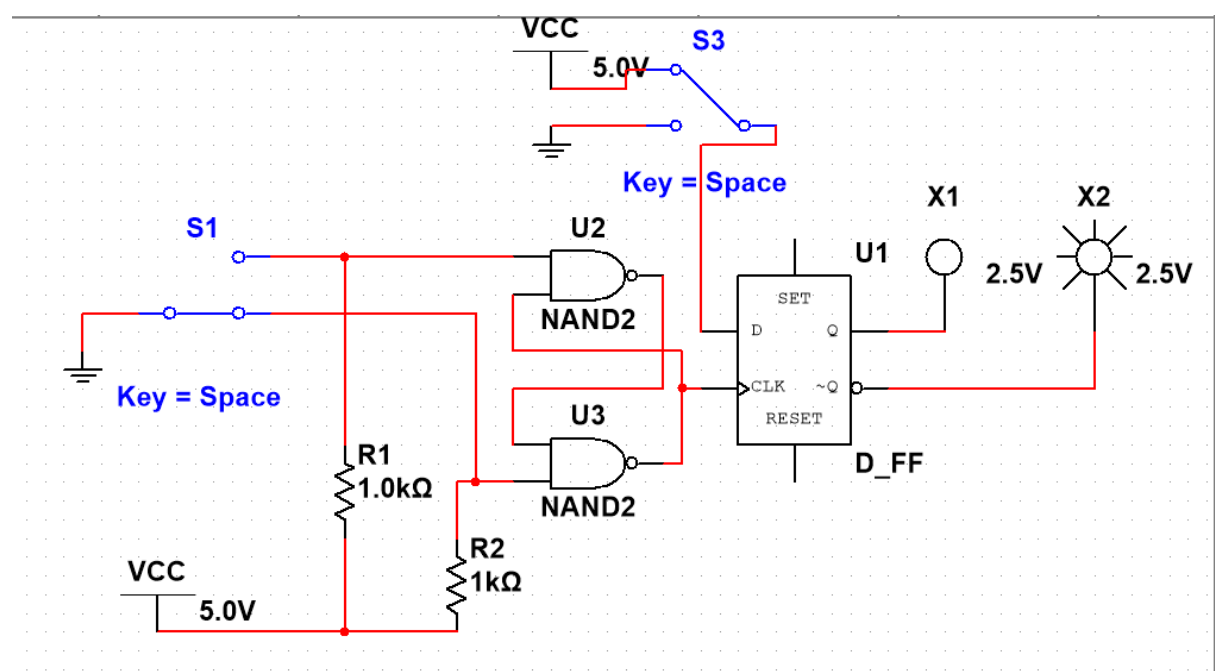


The circuit test for all combinations and was found to be correct.

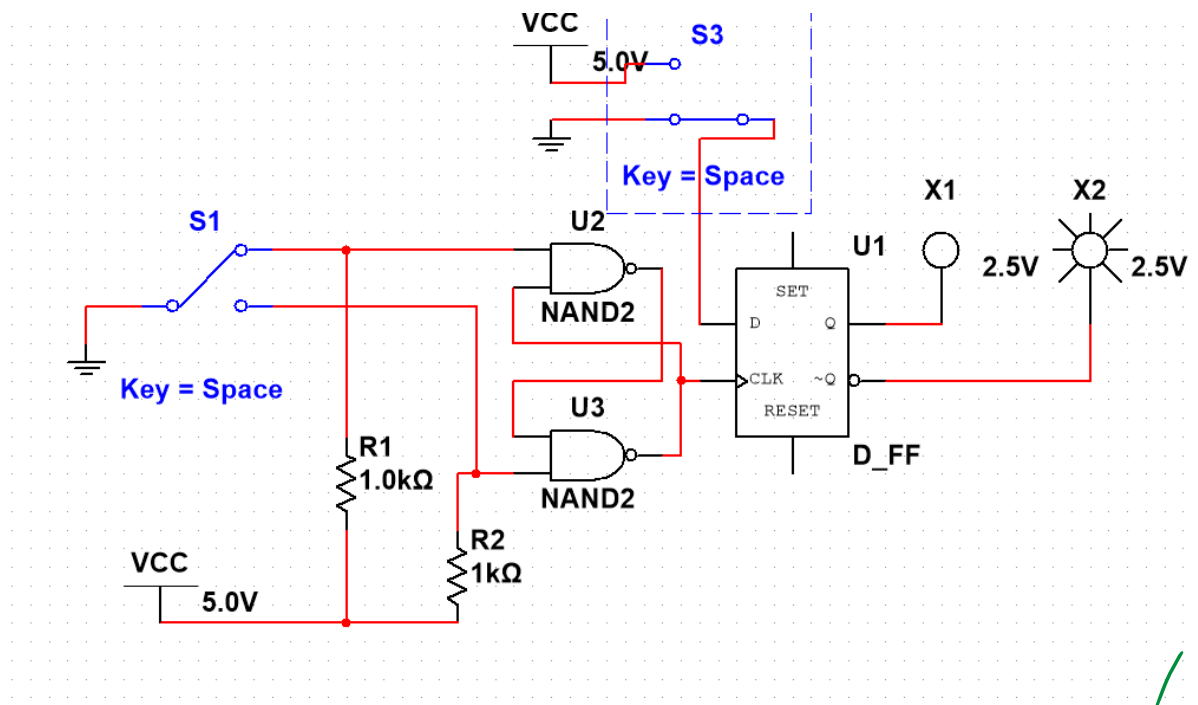
Task 5-1



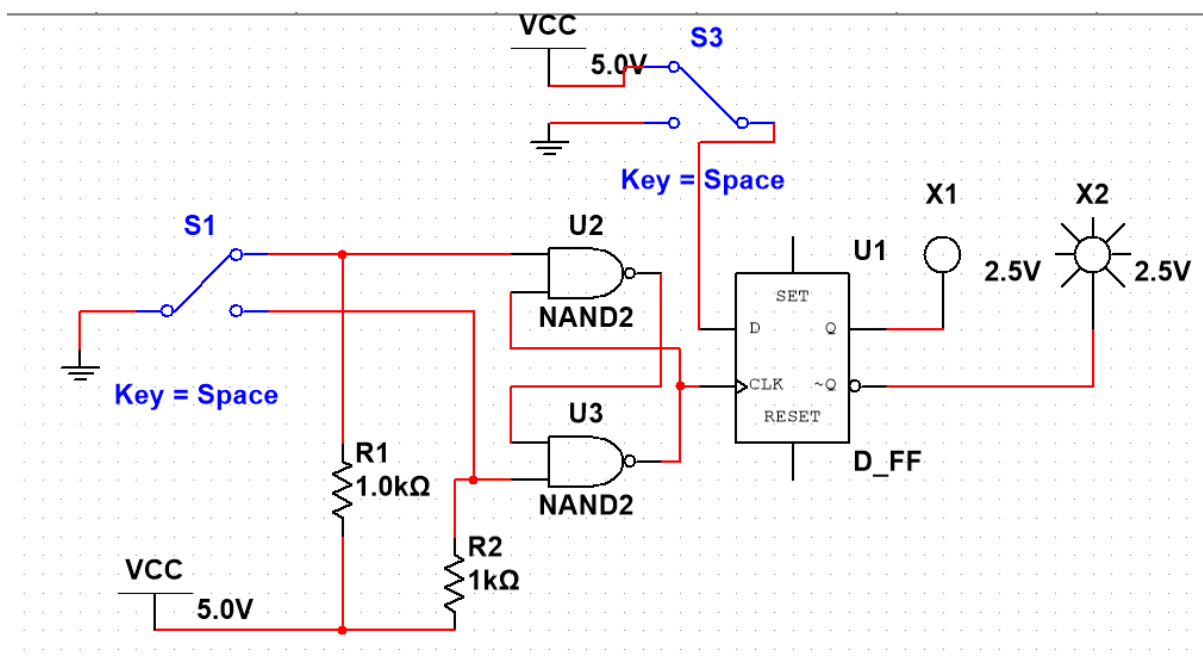
Task 5-2



Task 5-3



Task 5-4



Input	Outputs	
D	Q	
0	0	1
1	1	0

D-type truth table

The cross-coupled NAND gates are for switch debouncing. Why are they needed and how do they work?

Mechanical switches transfer the slight vibration from their action as signal noise. In analogue systems this causes some transition noise, but in digital systems it sends additional, unintended, positive and negative signals. These need eliminating so that, first, mistaken signals are not sent and, second, that this does not lead to signals being out of synchrony: viz, a false positive moves one rail to transmit its 'second' signal whilst the others are really signaling their second signal, so all coherence is lost.

Electrical signals are fast and fleeting. Logic needs to operate on one piece of data but electrical signals cannot be preserved. However, they can set switches which remain latched, transmitting constantly a signal that can be held and referred back to by the logical operations.

4)

J-K flip-flop truth table for binary counter cycling through 0 to 6.

	Present state of Q			Next state of Q								
	Qa	Qb	Qc	Qa	Qb	Qc	Ja	Ka	Jb	Kb	Jc	Kc
0	1	1	0	0	0	0	X	1	X	1	0	X
2	0	0	0	0	1	0	0	X	1	X	0	X
4	0	1	0	1	0	0	1	X	X	1	0	X
6	1	0	0	1	1	0	X	0	1	X	0	X

Karnaugh maps for Ja Ka flip-flops

KARNAUGH MAPS JA					KA				
Qbc					QBC				
Qa	00	01	11	10	QA	00	01	11	10
0	X	X	X	0	0	1	X	X	X
1	1	X	X	X	1	0	X	X	0

Karnaugh maps for Jb Kb flip-flops

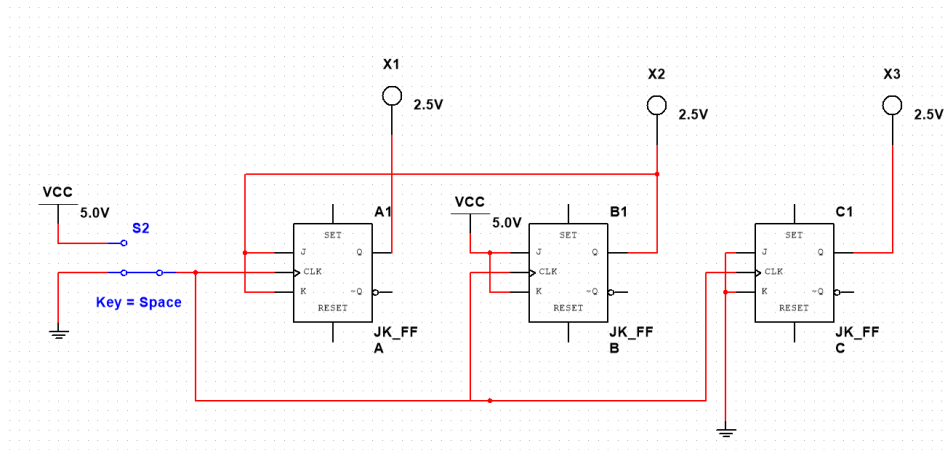
Jb					Kb				
	Qbc					Qbc			
Qa	00	01	11	10	Qa	00	01	11	10
0	X	X	X	1	0	1	X	X	X
1	X	X	X	1	1	1	X	X	X

Karnaugh maps for Jc Kc flip-flops

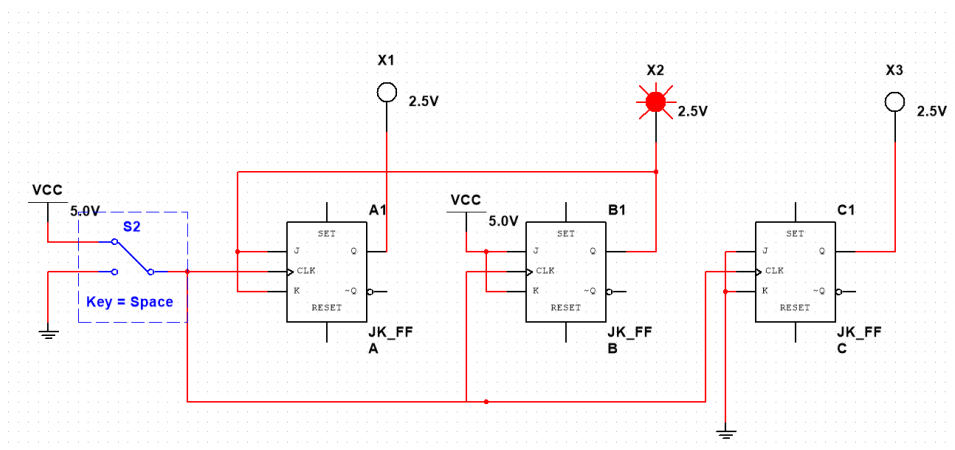
Kc				
	Qbc			
Qa	00	01	11	10
0	X	X	X	X
1	X	X	X	X
Jc				
	Qbc			
Qa	00	01	11	10
0	0	X	X	0
1	0	X	X	0

J-K flip-flop binary counter cycling through 0 to 6 running on Multisim.

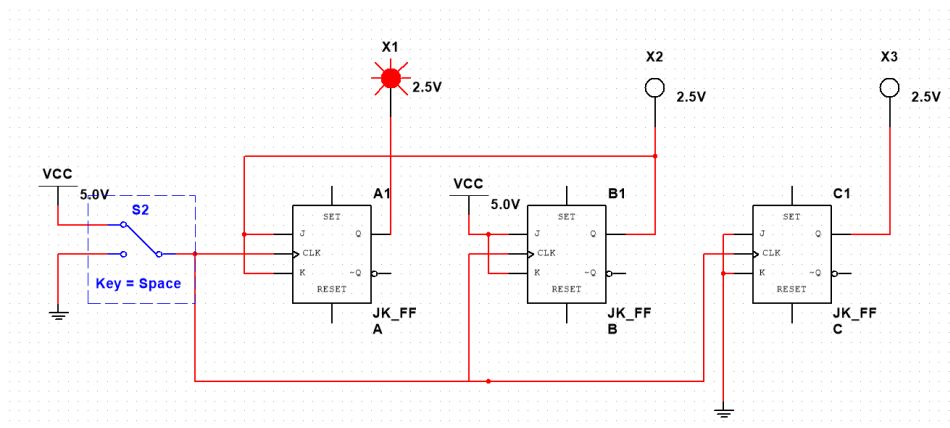
“0”



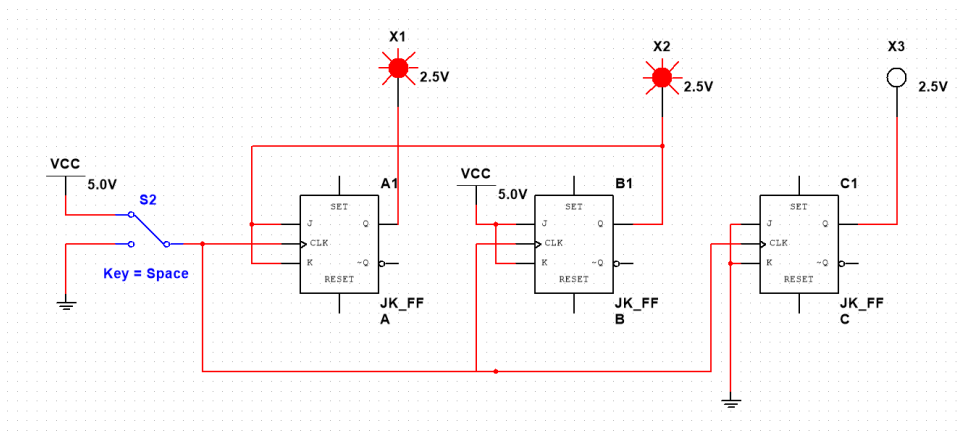
“2”



“4”



“6”



Logic in electronics and industry

George Boole (1815–1864) formulated binary mathematics, which uses only the numbers 0 and 1. In 1936, George Shannon wrote his MSci thesis on “how the logical algebra of 19th-century mathematician George Boole could be implemented using electronic circuits of relays and switches [using] the most fundamental feature of digital computers' design - the representation of "true" and "false" and "0" and "1" as open or closed switches.” (2) Whilst working on cryptography, he formulated a mathematical representation of information as mathematics, so it could be binary encoded, and analysed how to transmit encoded information without errors, for instance by using checksums and by measuring and staying within bandwidth.

When circuits enact Boolean logic as electrical signals this is “combinatorial logic” which is used for live processes, for instance to carry out mathematical operations in the Arithmetic Logic Unit of a microprocessor. Circuit outputs result only from input values so are extremely fast, but cannot incorporate memory-variable dependent functions such as feedback. An example of a combinatorial circuit is an Analogue-to-Digital converter, which translates input analogue signal to digital scaled output. Any single-logic circuit element affecting live signal only, such as a multiplexer selecting an input or a diode restricting current flow in one direction is combinatorial. Even within processing chips, the majority of

processes are combinatorial signals with dedicated sequential logic elements where necessary.

Sequential logic operates also on stored variables, such as clock counts or encoded data. Because electricity is live, any value must be held as an on/off state, as by JK flipflops, so sequential logic runs on a sequential circuit, with latched binary states storing bits of information. Computer memory and digital clocks are examples. In the absolute encoder, the previous position is stored as a binary string within a list of variables which can be fed into the logic operation so it can adjust its movement to the next position. Microprocessing functions include carry and add, registers for storing current or previous states or addresses, and buffers which allow signals to be synchronised.

Although quantum logic is more powerful than binary logic, because it cannot give unique discrete answers it cannot be combined with electricity for most simple applications (3) however they are faster where running multiple solutions is necessary, such as “Boolean satisfiability solvers, also known as SAT solvers” to detect flaws in microchips, or modelling financial markets.(4)

Footnotes

2 <https://www.scientificamerican.com/article/claude-e-shannon-founder> Collins, G. in Scientific American, 14/8/2002

3 <https://www.nist.gov/physics/introduction-new-quantum-revolution/quantum-logic-gates>

4 <https://www.ibm.com/downloads/cas/6PRYZJLV>

References

Tooley, M. *Electronic Circuits: Fundamentals and Applications* 4th Edn. London: Routledge. 2015

Bird, J. *Electrical Circuit Theory and Technology* 7th Edn. London: Routledge. 2021

Cusick, T. & Stanica, P. *Cryptographic Boolean Functions and Applications* 2nd Edn. New York: Academic Press. 2017

Could have included more sources.