

PSDE4004 Assignment 2

by Thomas Phillips

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HNC Electrical Electronic Engineering
PSDE4004 Electronics
Assignment 2

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1. Introduction, Aims and Objectives

This assignment will contain the design, simulation, construction and testing of digital circuits. These circuits include a decade counter, 0-5 counter and a 0-9 counter. They will be designed, simulated, constructed and tested on Multisim. This will imitate the same design as a digital stopwatch that can count from 0-59 and the numbers will be displayed on 2 separate displays. One display will show up to 5 and the second one will show up to 9. Research will be carried out on the differences between combinational and sequential logic circuit. Also, the pros and cons of ASIC and FPGA will be discussed and the differences between each other.

2. Research

Combinational and Sequential Logic Circuits

According to Elprocus.com, combinational logic circuits can only retain the memory of its current inputs whereas sequential logic circuits can retain the memory of both its current and previous inputs at the same time. (ELPROCUS, 2017)

Combinational circuits are used in Boolean and arithmetic operations whereas sequential circuits are mostly used for storing data so in RAM on computers.

From the images below it can be explained easier as to the differences between combinational and sequential circuits. The image on the left is of a standard combinational logic circuit and the one on the right is of a combinational logic circuit that has been converted into a sequential one.

In the left image, the input goes into the circuit and outputs go out of it. It doesn't retain the memory of the previous input; it just relies on what happens there and then. (See Figure 1)

In the right image, the input goes into the circuit and any outputs go out. Also, a positive feedback is sent out to the memory used which is then brought back into the circuits. This shows that it doesn't lose the memory of its previous inputs. The output depends on both the current input being put in and the input that has been put in beforehand. The memory part of the circuit is latch that can be called flip-flops. (See Figure 2)

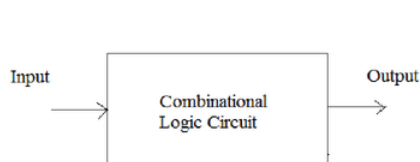


Figure 1: Combinational Logic Circuit

(Dewansh, 2015)

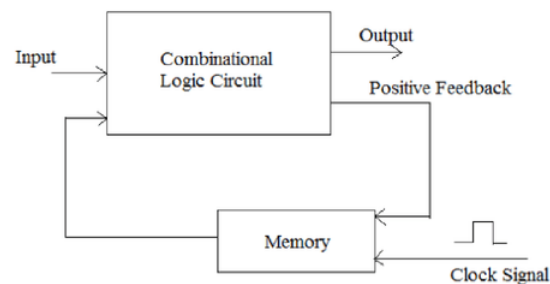


Figure 2: Sequential Logic Circuit

(Dewansh, 2015)

ASIC

'An ASIC (application-specific integrated circuit) is a microchip designed for a special application, such as a particular kind of transmission protocol or a hand-held computer.' (Rouse, 2005)

These are similar to an FPGA in the sense that they are both specialized chips that are used for different functions whilst operating at high performance levels. The one problem is that ASICs cannot be reprogrammed after they are made. This means that the cost will go up due to a new one having to be made for certain modifications. However, they are cheaper to use when used in high volume applications such as routers.

[FPGA](#)

'Field Programmable Gate Arrays (FPGAs) are semiconductor devices that are based around a matrix of configurable logic blocks (CLBs) connected via programmable interconnects.' (Xilinx, 2015)

A positive to using FPGA is it's flexible to use. This means that when programming the logic, the ability to reprogram it is there to use. This is helpful in the instance if a customer wants it for a specific application. This allows it also to be reprogrammed out in the field for example when upgrading a router for a customer so the lifespan is extended. FPGAs have contained within them loads of gates and programming logic. However, the downside to this is that most of the logic is not needed in certain applications because additional logic is required to connect the gates together. This means that an FPGA is not optimized to the fullest it can be.

3. Design Method

7 Segment Encoder

A 7 segment Encoder consists of 7 LEDs that when activated come on to display the corresponding light. For example, to display the number 3 for example, segments a, b, c, d and g would need to be illuminated. If a different number was to be made then a different set of segments would need to be illuminated. For a 7 segment display we can produce a truth table to determine what segments make each number which is shown in Table 1.

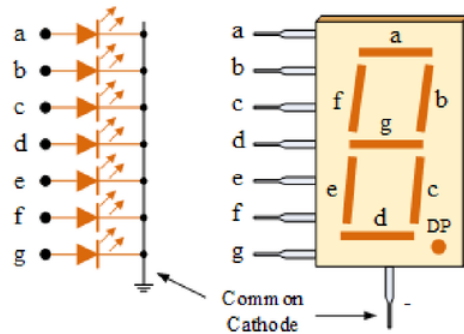


Figure 3: 7 Segment Display Diagram

(Electronics Tutorials, 2015)

As shown above, if b and c were to be true then the number '1' will be displayed. If all segments (a, b, c, d, e, f and g) were to be true then number '8' will be displayed. Below is the truth table for a 7 segment display.

Decimal Digit	a	b	c	d	e	f	g
0	1	1	1	1	1	1	0
1	0	1	1	0	0	0	0
2	1	1	0	1	1	0	1
3	1	1	1	1	0	0	1
4	0	1	1	0	0	1	1
5	1	0	1	1	0	1	1
6	1	0	1	1	1	1	1
7	1	1	1	0	0	0	0
8	1	1	1	1	1	1	1
9	1	1	1	0	0	1	1

Table 1: Truth Table for 7 Segment Encoder

Binary Coded Decimal is made up of 4 bits with the first number equalling 1, the second equalling 2, the third equalling 4 and fourth equalling 8. BCD only goes from 0 to 9 with the pattern being 1001 everything going from 1010 to 1111 is invalid and are not used. This works in conjunction with a 7 segment decoder because the number 0 to 9 can be displayed on the display.

(Electronic Tutorials, 2016)

$$a = A + C + \overline{B} \overline{D} + BD$$

AB/CD	00	01	11	10
00	1	0	1	1
01	0	1	1	1
11	X	X	x	x
10	1	1	x	X

$$b = \overline{B} + \overline{C} \overline{D} + CD$$

AB/CD	00	01	11	10
00	1	1	1	1
01	1	0	1	0
11	X	X	x	X
10	1	1	x	X

$$c = B + \overline{C} + D$$

AB/CD	00	01	11	10
00	1	1	1	0
01	1	1	1	1
11	X	X	x	x
10	1	1	x	X

$$d = A + \overline{B} \overline{D} + \overline{B} C + C \overline{D} + B \overline{C} D$$

AB/CD	00	01	11	10
00	1	0	1	1
01	0	1	0	1
11	X	X	x	x
10	1	1	x	X

$$e = \overline{B} \overline{D} + C \overline{D}$$

AB/CD	00	01	11	10
00	1	0	0	1
01	0	0	0	1
11	X	X	x	x
10	1	0	x	X

$$f = A + B + \overline{C} \overline{D}$$

AB/CD	00	01	11	10
00	1	0	0	0
01	1	1	1	1
11	X	X	x	x
10	1	1	x	X

$$g = A + B \overline{C} + \overline{B} C + C \overline{D}$$

AB/CD	00	01	11	10
00	0	0	1	1
01	1	1	0	1
11	X	X	x	x
10	1	1	x	X

Below is the circuit that was constructed on Multisim using the expressions that were calculated.

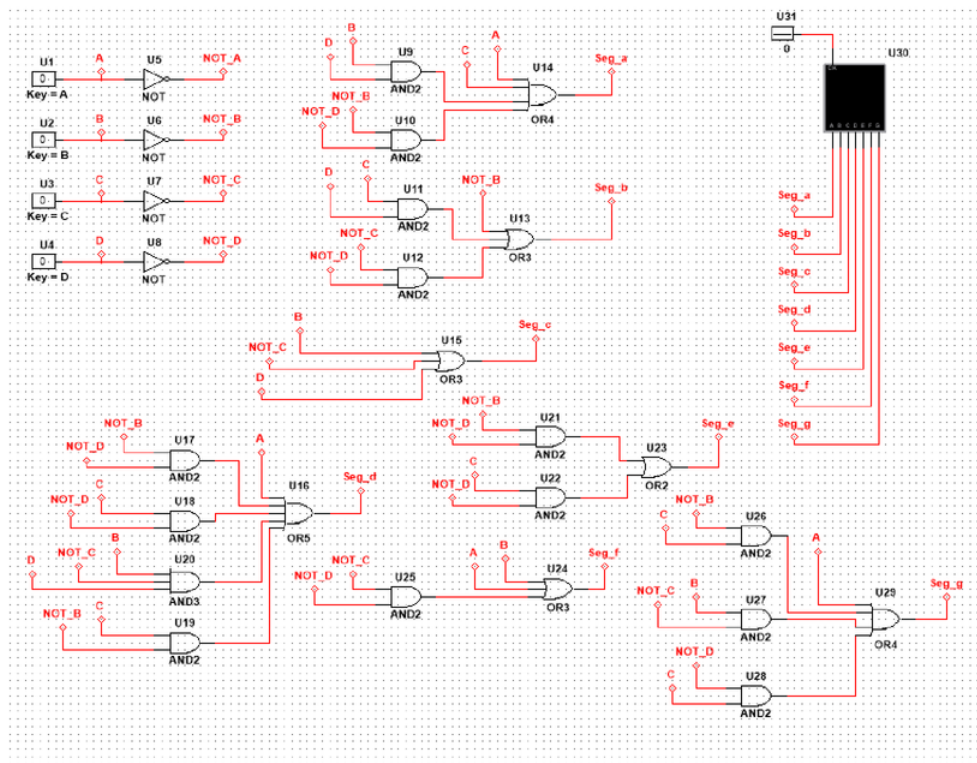


Figure 4: 7 Segment Encoder

0-5 Counter

A 0-5 counter counts from 0-5 then resets itself. Below shows the state table for this. The following Boolean expressions were used to construct the 0-5 counter circuit on Multisim.

Current	Next	Current			Next		
		Q ₁	Q ₂	Q ₃	Q _A +	Q _B +	Q _C +
S ₀	S ₁	0	0	0	0	0	1
S ₁	S ₂	0	0	1	0	1	0
S ₂	S ₃	0	1	0	0	1	1
S ₃	S ₄	0	1	1	1	0	0
S ₄	S ₅	1	0	0	1	0	1
S ₅	S ₀	1	0	1	0	0	0

Table 2: State Table for 0-5 Counter

$$Q_{A+} = A \overline{C} + BC$$

$$Q_{B+} = BC + \overline{A} \overline{B} C$$

A/BC	00	01	11	10
0	0	0	1	1
1	1	0	x	x

A/BC	00	01	11	10
0	0	1	0	1
1	0	0	x	x

$$Q_{C+} = \overline{C}$$

A/BC	00	01	11	10
0	1	0	0	1
1	1	0	x	x

Below is the circuit that was constructed using these expressions.

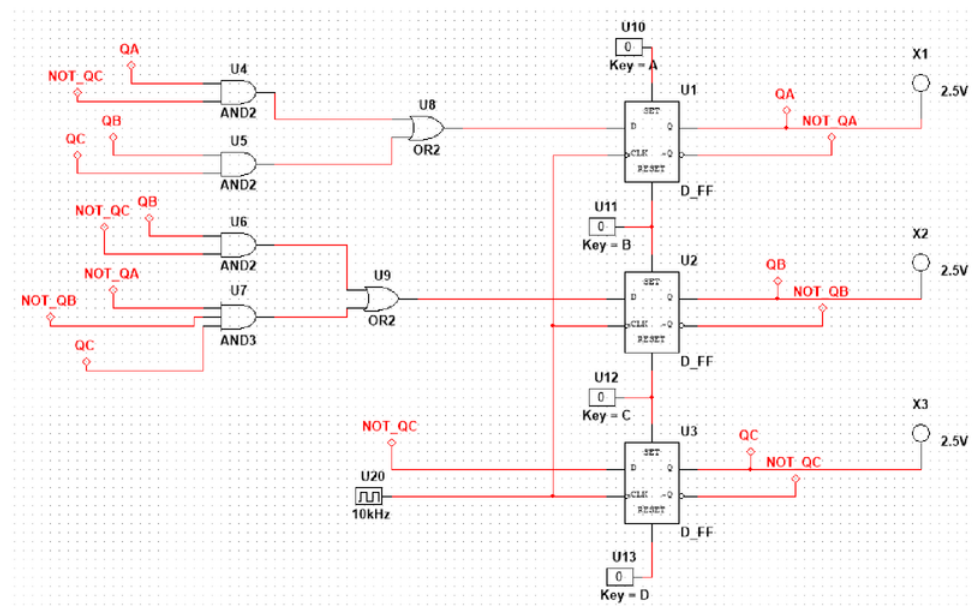


Figure 5: 0-5 Decade Counter

0-9 Counter

A 0-9 counter counts from 0-9 then resets itself. Below is the state table and Boolean expressions. The Boolean Expressions were then used to create the circuit using flip-flops.

Current	Next	Current				Next			
		Q ₁	Q ₂	Q ₃	Q ₄	Q _A +	Q _B +	Q _C +	Q _D +
S ₀	S ₁	0	0	0	0	0	0	0	1
S ₁	S ₂	0	0	0	1	0	0	1	0
S ₂	S ₃	0	0	1	0	0	0	1	1
S ₃	S ₄	0	0	1	1	0	1	0	0
S ₄	S ₅	0	1	0	0	0	1	0	1
S ₅	S ₆	0	1	0	1	0	1	1	0
S ₆	S ₇	0	1	1	0	0	1	1	1
S ₇	S ₈	0	1	1	1	1	0	0	0
S ₈	S ₉	1	0	0	0	1	0	0	1
S ₉	S ₀	1	0	0	1	0	0	0	0

Table 3: State Table for 0-9 Counter

$$Q_{A+} = A \overline{D} + BCD$$

AB/CD	00	01	11	10
00	0	0	0	0
01	0	0	1	0
11	X	X	x	x
10	1	0	x	X

$$Q_{B+} = B \overline{C} + B \overline{D} + \overline{B} CD$$

AB/CD	00	01	11	10
00	0	0	1	0
01	1	1	0	1
11	X	X	x	x
10	0	0	x	X

$$Q_{C+} = C \overline{D} + \overline{A} \overline{C} D$$

AB/CD	00	01	11	10
00	0	1	0	1
01	0	1	0	1
11	X	X	x	x
10	0	0	x	X

$$Q_{D+} = \overline{D}$$

AB/CD	00	01	11	10
00	1	0	0	1
01	0	1	0	1
11	X	X	x	x
10	1	x	x	X

Below is the 0-9 Decade Counter circuit that was constructed using these expressions.

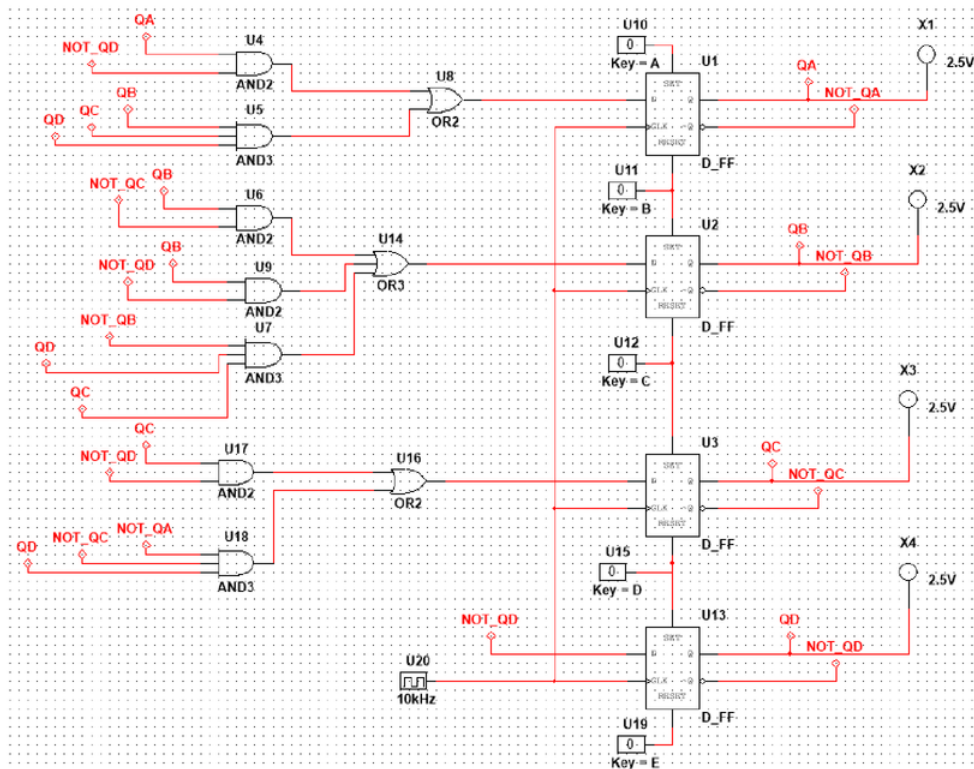


Figure 6: 0-9 Decade Counter

4. Analysis of Results

When testing the 7 segment encoder, the binary decimals can be changed which are displayed as A, B, C and D. In Figure 7, B and D are on which is 1010. This displays the number 5 on the 7 segment display. If A and D were on then the number 9 would appear. However, if A and B are on then the number that should appear would be 12 but because the BCD numbers only go from 0-9 this isn't possible.

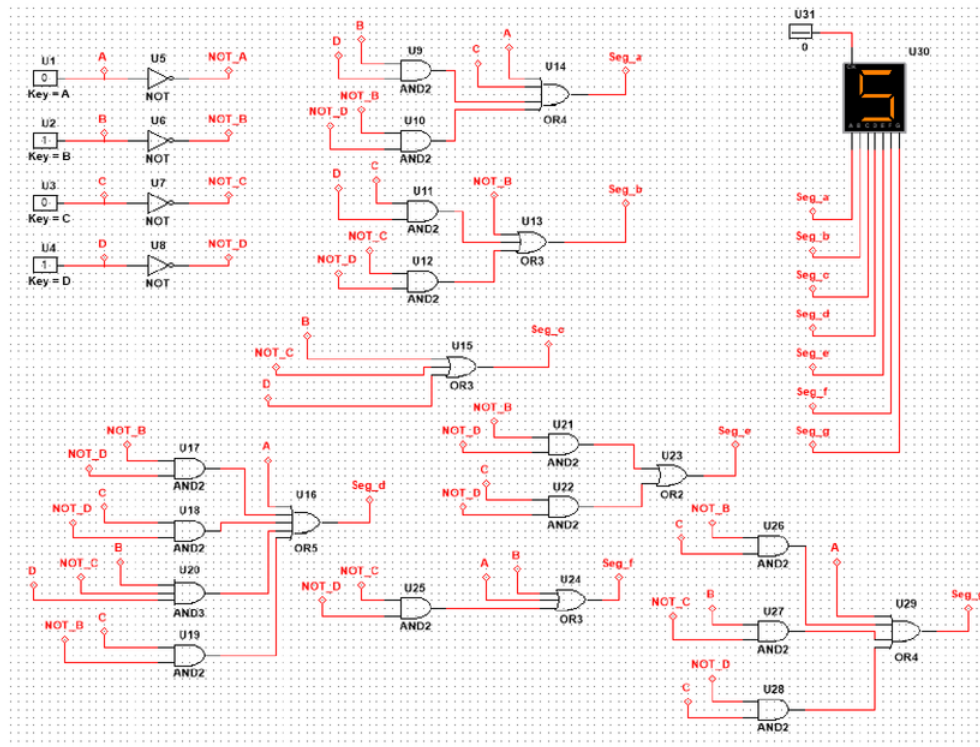


Figure 7: Testing for 7 Segment Encoder

When testing the combined circuit that includes the 7 segment encoder and 0-5 counter, the display will start to count from 0-5 then reset and start again. If the 0-9 counter was to be implemented instead of the 0-5 then same result would appear when compared to the testing of the 7 segment encoder circuit. The one difference of this is that it counts by itself and doesn't require a manual input to activate the BCD numbers.

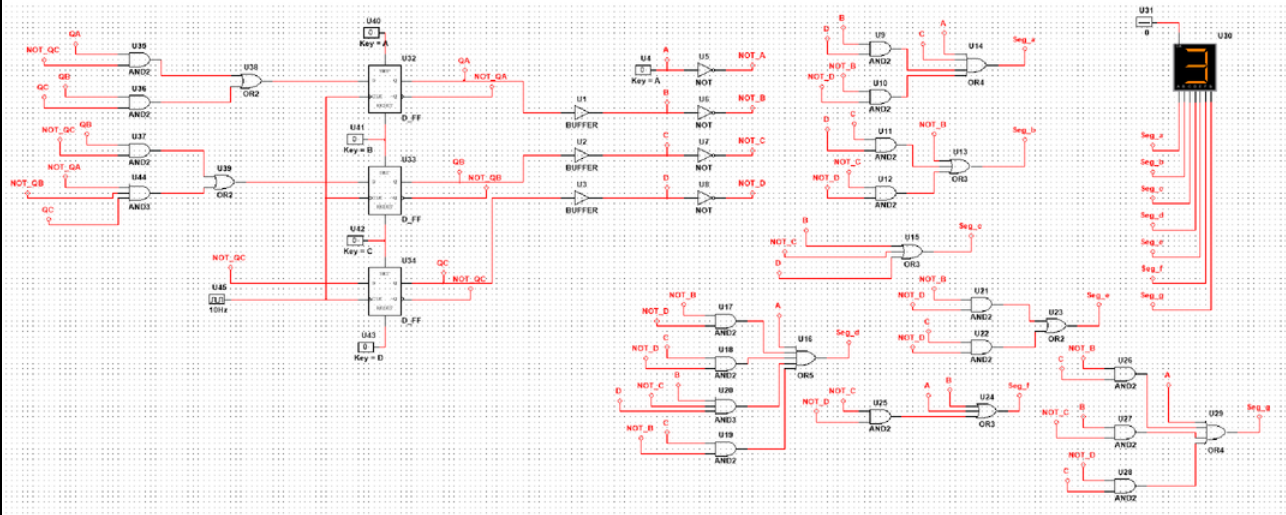


Figure 8: Combined Circuit

To clearly see what is going on during the testing stage, a logic analyser was inserted into the circuit. Figure 9 shows the analyser when the circuit is running. When the red line goes up and across, this means that it's the time that input was on. However, when the red line goes down and across this indicates the time that the input has gone off.

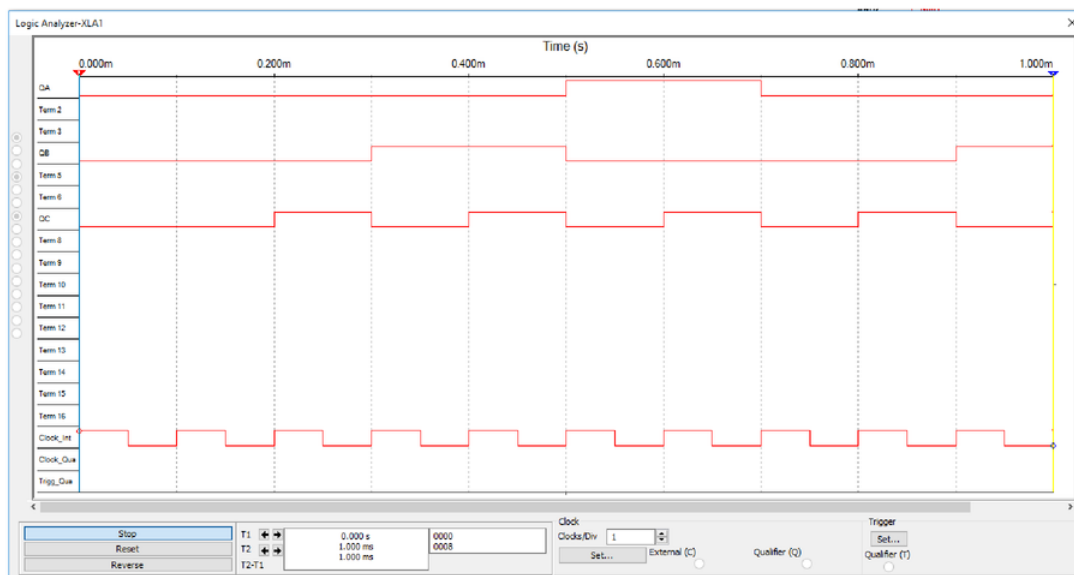


Figure 9: Logic Analyser on Combined Circuit

5. Conclusions

The final circuit partially met the specification. The circuit could count from 0-9 and 0-5 when the 7 segment encoder is integrated with the 0-9 or 0-5 decade counter. However, both counters weren't incorporated in the same circuit together so they couldn't count from 0-59 using 2 displays. A finite state machine was used when constructing both decade counters. The circuits constructed all worked individually but all weren't incorporated at once. An improvement could be made to this circuit which would be adding 2 0-9 decade counters so 0-99 could be displayed on 2 different displays.

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GRADEMARK REPORT

FINAL GRADE

GENERAL COMMENTS

Instructor

48/100

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GRADING FORM: CSG-RUBIC

THOMAS PHILLIPS

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RESEARCH-INFORMED LITERATURE

 There was evidence of further reading and research with the inclusion of a reference list however there was no evidence of any in-text referencing. Your interpretation and understanding of the additional research was satisfactory. Your references list was short for this the task.

3

KNOWLEDGE AND UNDERSTANDING

 The knowledge and understanding of the subject demonstrated by this assignment was generally acceptable. The circuits worked and the explanation of how this was achieved had good detail. Your research lacked depth and detail at times and didn't really extend your knowledge beyond that contained in the course notes. Further work – Research results need to be in much more detail and written in a more logical and clearer way.

14

ANALYSIS

 Your analysis of the task was brief and lacked a lot of the required detail. You have demonstrated reasonable analytical skills and your approach to the task was logical. You carried out a reasonable evaluation of the results, but the conclusions were very brief.

7

PRACTICAL APPLICATION AND DEP.

Your application of practical skills for this task were



generally OK, you used the resources appropriately when carrying out the experiment and you used appropriate options for testing and evaluating the circuit performance - albeit to a limited fashion. Testing generally lacked a lot of the required detail however and you should have included a comprehensive set of results for each stage.

17

SKILLS FOR PROFESSIONAL PRAC.



In this assignment you have demonstrated skills in working individually and also collaboratively. Your written report was of an appropriate length, you could however be more efficient with your word count. The report was well presented, with good diagrams in appropriate places, good sentence/paragraph structure and clear calculations.

7