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Complete, fold and seal
(see note 2 below)

SURNAME: Atkinson

FORENAME(S): Oliver

Examination Answer Books

12 Pages

Instructions to Candidates

1. Please give the information requested in the boxes below.
2. Enter your name in the space provided to the right, fold over and seal down (using the label provided) to hide your name.
3. The answers must be legibly written. The Examiners can either ignore illegible script or have it typed and the expense of typing charged to the candidate.
4. Write your answers in ink.
5. Begin each answer on a fresh page. Do all rough work in the answer book and cross it through.
6. No part of this book is to be torn out; it must be handed in complete.
7. If more books than one are used, fasten them together using the tags available from the invigilator(s).
8. Every book must be handed in. In no circumstances may answer books, used or unused, be taken out of the examination venue.

1	Student Number	2311854
2	Title of Examination Paper	Micros, Peripherals and interfaces
3	Module Code	ACDA4004
4	Date and Time of Examination	8/1/25 9:00am
5	Examination Venue	IQ310
6	Seat Number	034
7	Number of Answer Books handed in	1

List the numbers of the questions you have attempted	Office Use
1	9 1/2
2	9
3	3
4	10
5	8 1/2
6	4
	44
	x 2
Total	88 1/2

9 1/2
9
3
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44.

- 1) ?
↓
- Return "Return to main stack"
- It returns from a subroutine to the location in the main function where it was called from
 - SLEEP "low energy mode"
- The code/compiler waits in a low energy mode for something like an interrupt to occur
 - ADDLW "Add the contents of literal to the working register"
- The contents of the working register and the literal value are added together. The result is placed in the working register
 - BCF f, b "Bit clear file f register, binary"
- This clears a specified bit on the PIC chip
 - DECf "Decrement f"
- decrease the value in f by 1, Place the result in the file register.

2

2

2

2

2

2

1 1/2

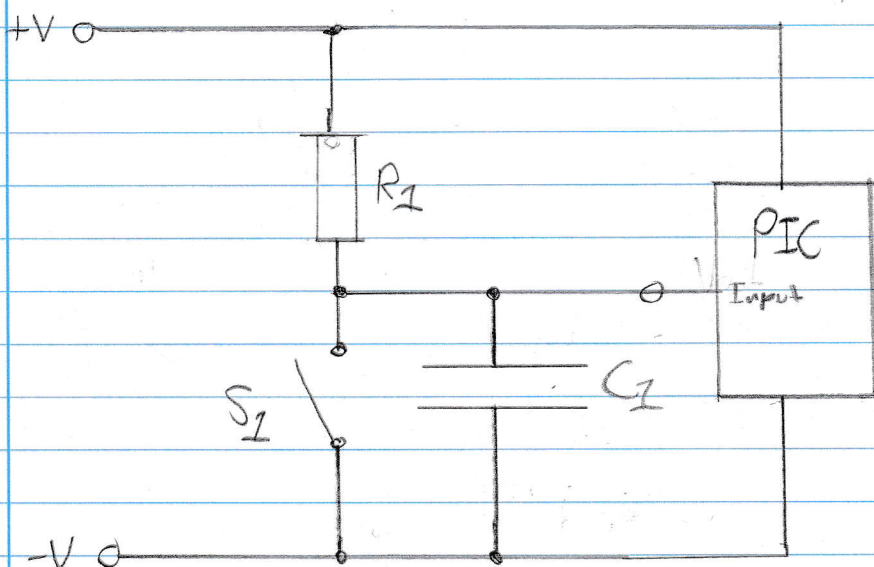
1 1/2

2

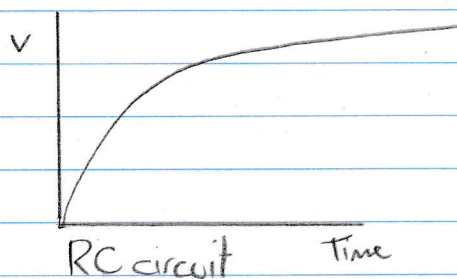
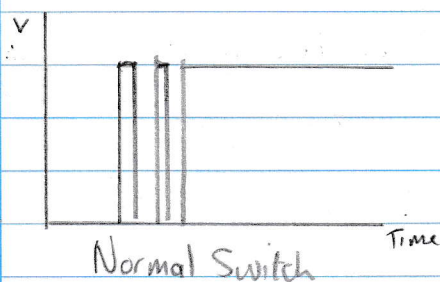
2

9 1/2

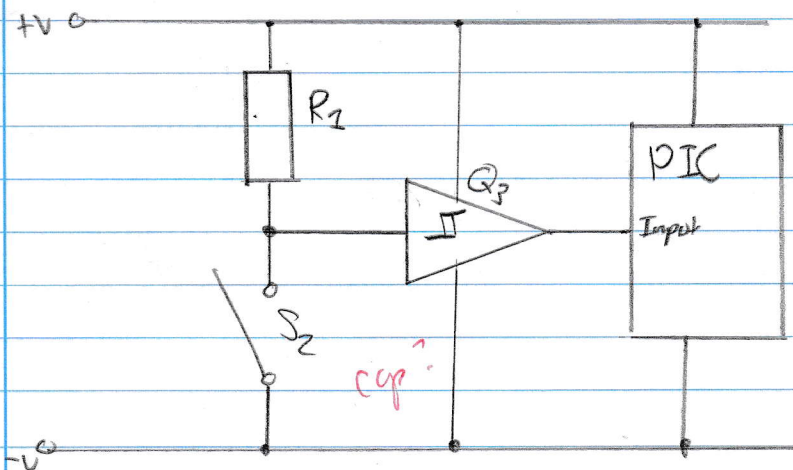
2) R-C circuit



The introduction of the capacitor C_1 creates an RC circuit. This means it will take 5 time constants to fully switch reducing the false inputs that occur when switch bounce occurs.

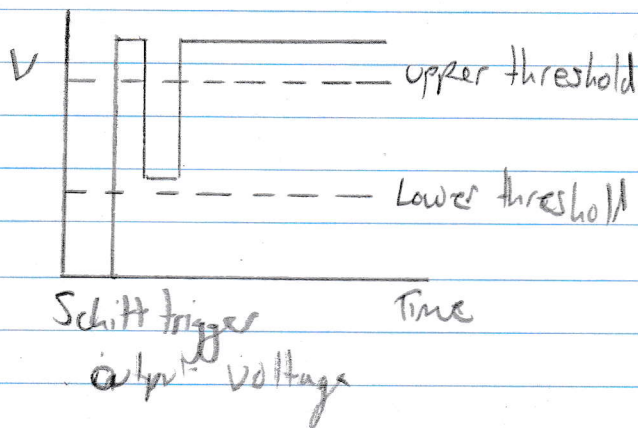


Schmitt trigger



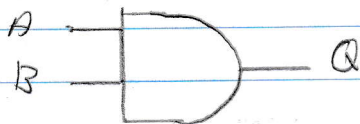
Schmitt triggers have two thresholds where it is able to switch. One at $3/4$ of full Voltage and one at $1/4$ full voltage. In order to switch on the V_{in} has to reach the upper threshold. In order to turn off again the voltage has to drop below the low threshold. This won't happen even with switch bounce.

So the Schmitt mitigates switch bounce by not letting the voltage drop below.



even though the voltage drops it doesn't go below the threshold.

3)



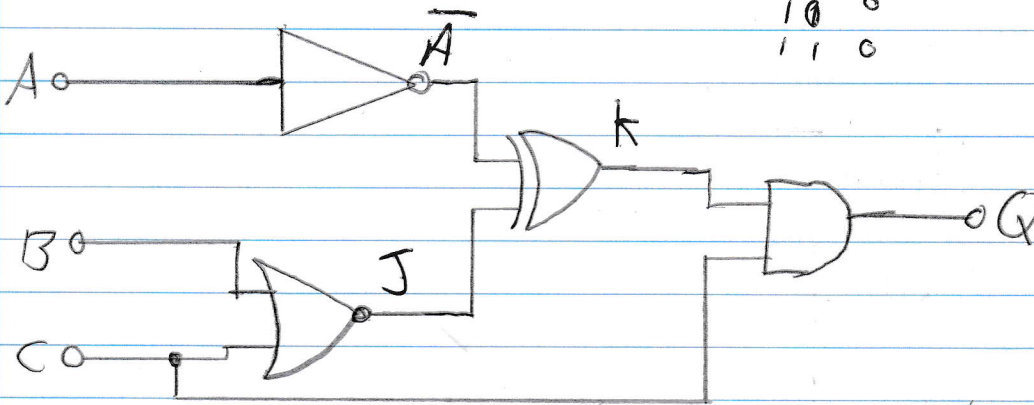
B	A	Q
0	0	0
0	1	0
1	0	0
1	1	1

3

3

NOR

00	1
01	0
10	0
11	0

4)
a)

C	B	A	$\bar{A}$	J	K	Q
0	0	0	1	1	0	0
0	0	1	0	1	1	0
0	1	0	1	0	1	0
0	1	1	0	0	0	0
1	0	0	1	0	1	1
1	0	1	0	0	0	0
1	1	0	1	0	1	1
1	1	1	0	0	0	0

$$Q = J + K$$

$$J = B + C$$

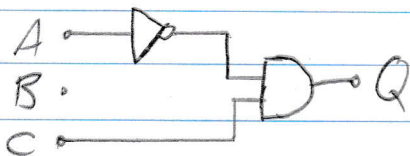
$$K = (\overline{B+C}) + \bar{A} = J \oplus \bar{A}$$

$$Q = K \cdot C$$

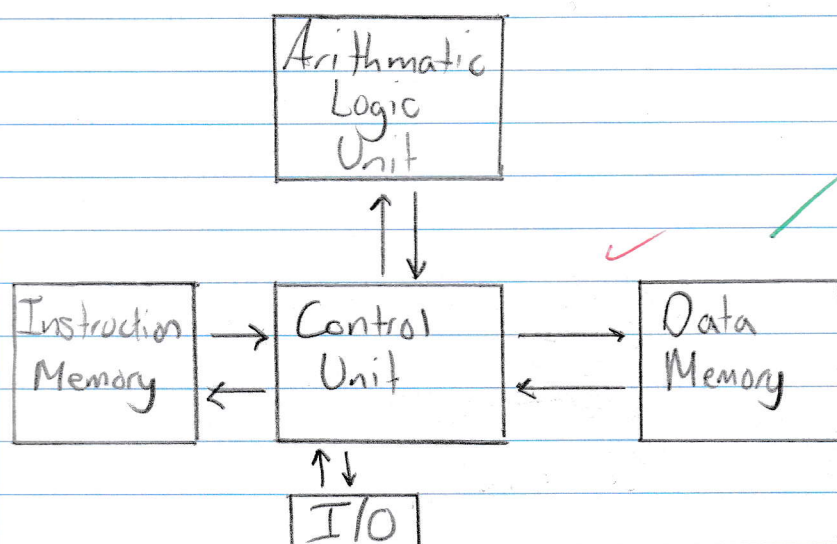
C	B	A	$\bar{A}$	J	K	Q
0	0	0	1	1	0	0
0	0	1	0	1	1	0
0	1	0	1	0	1	0
0	1	1	0	0	0	0
1	0	0	1	0	1	1
1	0	1	0	0	0	0
1	1	0	1	0	1	1
1	1	1	0	0	0	0

b) $Q = 1$ when C and $\bar{A}$ are One

$$\therefore Q = C \cdot \bar{A}$$



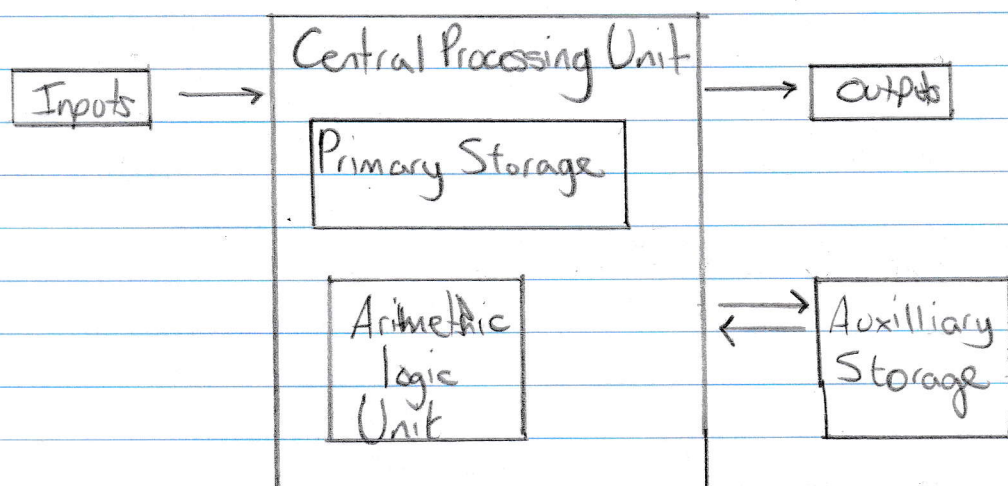
5) Harvard



Harvard has parallel processing due to separate storage for data and instructions. This also has separate information buses for data and instructions.

This means harvard can read/write data and fetch instructions at the same time. Overcoming the bottleneck provided by Von neumann's serial processing single storage method.

Von neumann



Like mentioned previously this von neumann architecture has a single primary storage for both data and instructions in also has a single bus to transfer data on.

Whilst this creates a bottleneck in the system, it makes a von neumann processor cheaper and simpler to manufacture due to it's simplicity. This is why most general purpose electronics/computers use von neumann processors and only incredibly specific microprocessors within embedded systems use harvard.

8 1/2

6) PWM:

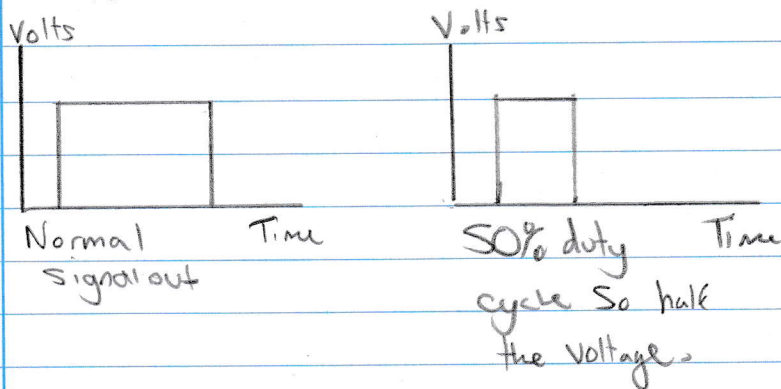
Pulse width modulation

The altering of output voltage level levels via the extension of a signal. ?

Duty cycle is the percentage time spent on. ✓

Using the duty cycle at 50% produces an output voltage of half the $+V$. ✓

Using the PIC and preconfigured variables in the built in PWM module, the duty cycle can be altered producing different V_{out} s. *how?*



4

4.