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Abstract

This report contains the written reflection and evidence on the application of the skills covered during the course of this module. This includes results obtained from practical tests carried out and evidence of the method used. This experiment required the learner to test an RLC circuit in Proteus and on a breadboard and then compare the results to each other and the theory. The results obtained revealed to the student that the breadboard simulation results differed from the Proteus simulation and theory due to several real-world physical properties that the simulation doesn't consider.

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List of Abbreviations

IC	Integrated Circuit
FM	Frequency Modulation
nH	Nano Henries
pF	Pico Farads
MHz	Mega Hertz
k Ω	Kilo Ohms
μ F	Micro Farads
mH	Milli Henries
kHz	Kilo Hertz
V	Volts
dB	Decibels
Hz	Hertz
Q	Quality Factor
R	Resistance
L	Inductance
C	Capacitance
A	Cross-Sectional Area

f_r	Resonant Frequency
V_{out}	Output Voltage
V_{in}	Input Voltage
f_1	Frequency 1 (Obtained from the -3 dB point)
f_2	Frequency 2 (Obtained from the -3 dB point)
BW	Bandwidth
ρ	Resistivity
$^{\circ}\text{C}$	Degrees Celcius
Ωm	Ohmic Metres
P	Power
I	Current

1 Introduction

In this task, the learner was required to build and simulate an RLC circuit in Proteus, test it on a breadboard and then compare the outcomes from both methods with each other and theoretical calculations. RLC circuits are electrical circuits that combine resistors, inductors, and capacitors connected in either a series or parallel arrangement. RLC circuits are often combined in modern communication systems to form complete integrated circuits (IC's) [1]. An example of this is radio receivers, where RLC circuits are used to select specific frequencies from a broad spectrum. For example, a circuit with a 100 nH inductor and a 25 pF capacitor will produce a resonance frequency at approximately 100 MHz, which is suitable for FM radio tuning. Other applications include oscillators, wireless communication, and signal filtering for audio equipment, where RLC circuits help block unwanted frequencies and pass desired signals, improving sound quality [2]. In this experiment, one equation that will be used is the resonance frequency formula, which can be seen in Equation 1 below.

Equation 1: Resonance frequency formula

$$f_r = \frac{1}{2\pi\sqrt{LC}}$$

Additionally, the Q factor (or quality factor) will be calculated using Equation 2 below.

Equation 2: Q factor formula

$$Q = R \sqrt{\frac{C}{L}}$$

Also, the formula used to calculate attenuation for both simulations can be seen in Equation 3 below.

Equation 3: Attenuation formula

$$dB = 20 \times \log_{10} \left(\frac{V_{out}}{V_{in}} \right)$$

Throughout this report, the results of the experiment will be recorded in tables and visually represented with graphs. Any variation or similarity in results will then be discussed and justified.

2 Simulation Circuit

2.1 Proteus Setup

The first step of this experiment was to simulate the RLC circuit in Proteus. The circuit included a 1 k Ω resistor, which was connected in series to a 1 μ F capacitor, and a 1 mH inductor, which was connected in parallel, as displayed in Figure 1. The circuit was set up to measure the voltage across the inductor and capacitor at a range of frequencies from 1 kHz to 20 kHz. Once the voltage had been measured, the ratio gain was calculated, and then the attenuation at each frequency was obtained using Equation 3. The input voltage (V_{in}) was a constant 2 V peak-to-peak sine wave for all frequencies. As the attenuation began nearing zero, smaller increment measurements were taken in order to attain a more accurate resonant frequency. Evidence of the circuit simulated in Proteus can be seen in Figure 1 & 2.

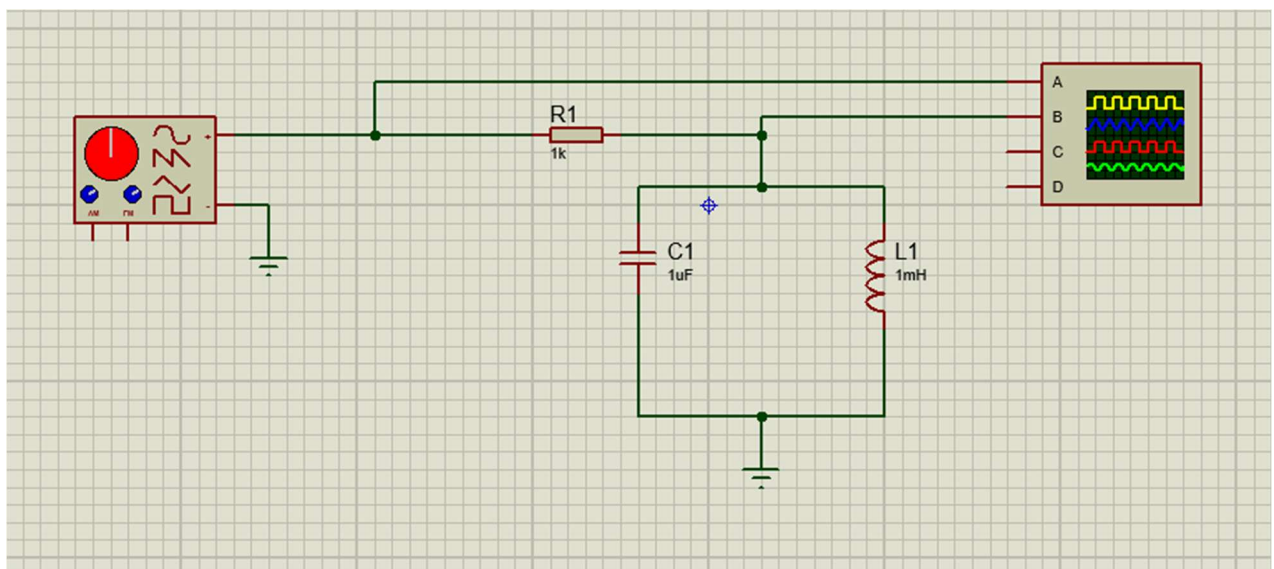


Figure 1: Circuit designed in Proteus

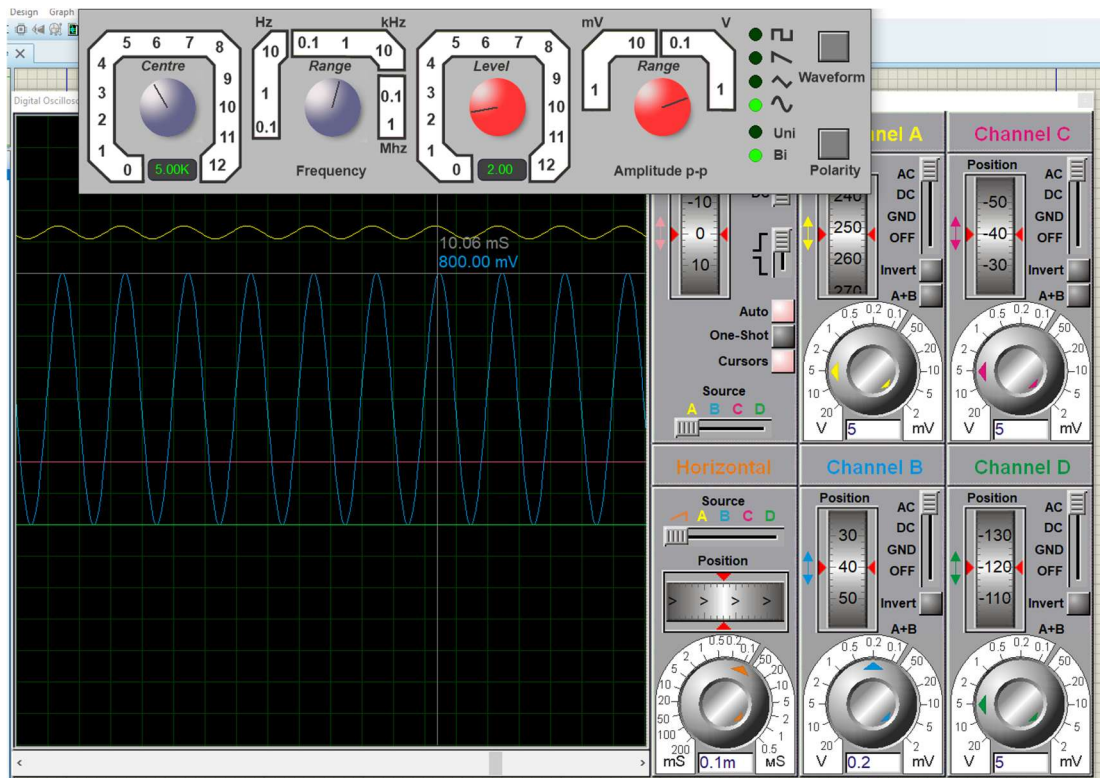


Figure 2: Circuit in Proteus being simulated

2.2 Results from Proteus Simulation

Once the circuit had been tested for all frequencies between 1 kHz and 20 kHz, the results were then recorded in Table 1 below.

Table 1: Results from Proteus simulation

Frequency (Hz)	V _{in} (V)	V _L (V)	Gain (ratio)	Attenuation (dB)
1000	2	0.01	0.005	-46.0206
2000	2	0.03	0.015	-36.4782
3000	2	0.06	0.03	-30.4576
3500	2	0.09	0.045	-26.9357
4000	2	0.15	0.075	-22.4988
4500	2	0.32	0.16	-15.9176
4800	2	0.84	0.42	-7.53501
4900	2	1.44	0.72	-2.85335
5000	2	1.61	0.805	-1.88408
5100	2	0.96	0.48	-6.37518
5200	2	0.63	0.315	-10.0338
5300	2	0.46	0.23	-12.7654
5400	2	0.36	0.18	-14.8945
6000	2	0.16	0.08	-21.9382
7000	2	0.09	0.045	-26.9357
10000	2	0.04	0.02	-33.9794
20000	2	0.02	0.01	-40

From the results obtained in Table 1 above, a semi-log graph of attenuation vs frequency was then plotted. Consequently, the learner could then find the -3 dB or 'half-power' point, which can be seen in Figure 3 below.

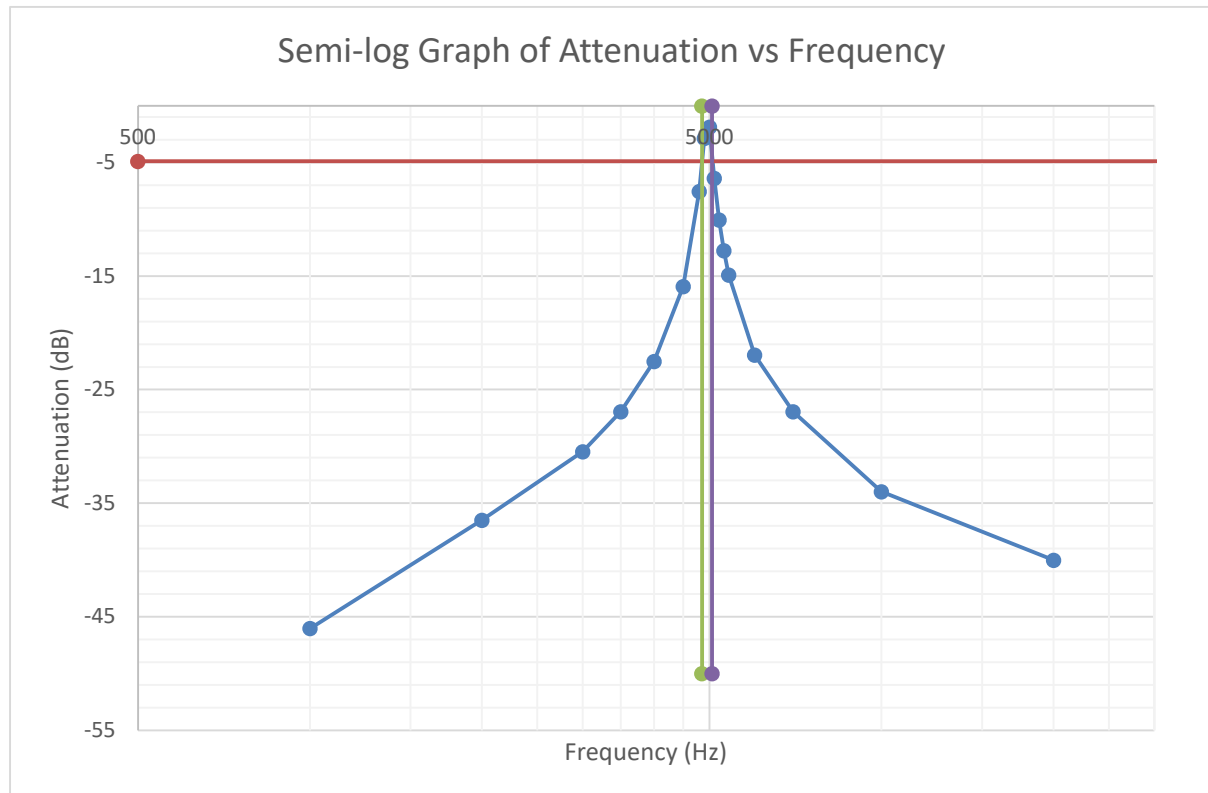


Figure 3: Semi-log graph of Attenuation vs Frequency for Proteus simulation

The intersecting lines that can be seen in Figure 3 above show the -3 dB point (Red), and points f_1 (Green) and f_2 (Grey), which were used to calculate the bandwidth. The semi-log graph in Figure 3 increases gradually until it suddenly rises as it approaches the resonant frequency, then peaks, then decreases rapidly, then gradually slows. As can be seen in Figure 3 and Table 1, the voltages across the inductor and capacitor reach their maximum at resonance. This point is also when the attenuation reaches its maximum of -1.884 dB. The half-power point was determined by subtracting 3 dB from the maximum attenuation, resulting in two intersecting frequencies at 4850 Hz (f_1) and 5050 Hz (f_2). With these values, it is then possible to calculate the bandwidth by subtracting f_1 from f_2 , which results in a value of 200 Hz. After that, the Q factor, also known as the quality factor, was calculated by dividing the resonant frequency by the bandwidth, giving a value of 25. When calculating the Q factor of this circuit using theoretical values with Equation 2, a result of 31.62 is obtained, which is slightly higher than the outcome of 25 that was received from the Proteus simulation.

3 Breadboard Circuit

3.1 Breadboard Set Up

After completing the Proteus simulation of the circuit and recording the results, the student then began to set up the circuit on the breadboard. The breadboard setup consisted of the same components used in the Proteus simulation, which included a 1 k Ω resistor, a 1 μ F capacitor, and a 1 mH inductor. The student connected the resistor in series with an inductor and a capacitor, which are connected in parallel. Then, the signal generator was connected to the green input wire, and the oscilloscope probes were connected between the input wire and the resistor. The signal generator was set to a 2 V peak-to-peak sine wave, starting at 1 kHz and then tested for the same frequencies as the Proteus simulation up to 20 kHz. The set-up of the breadboard circuit can be seen below in Figure 4, 5 & 6.

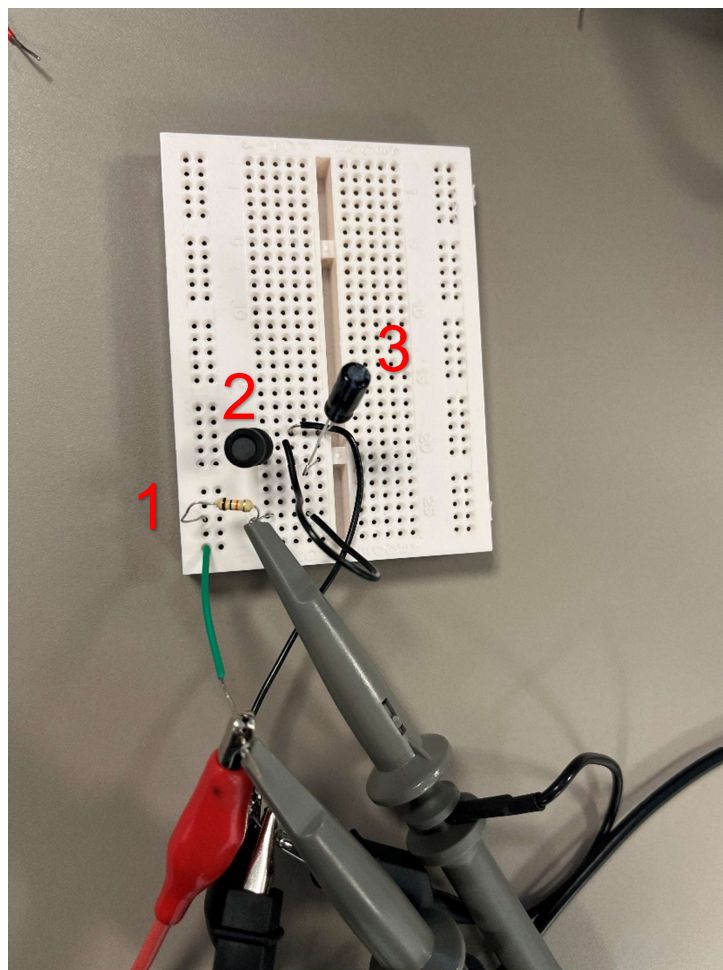


Figure 4: Breadboard setup of RLC circuit

Table 2 below identifies each of the components used in the breadboard RLC circuit seen above in Figure 4.

Table 2: List of components

Component No.	Component
1	1 k Ω resistor
2	1 mH inductor
3	1 μ F capacitor

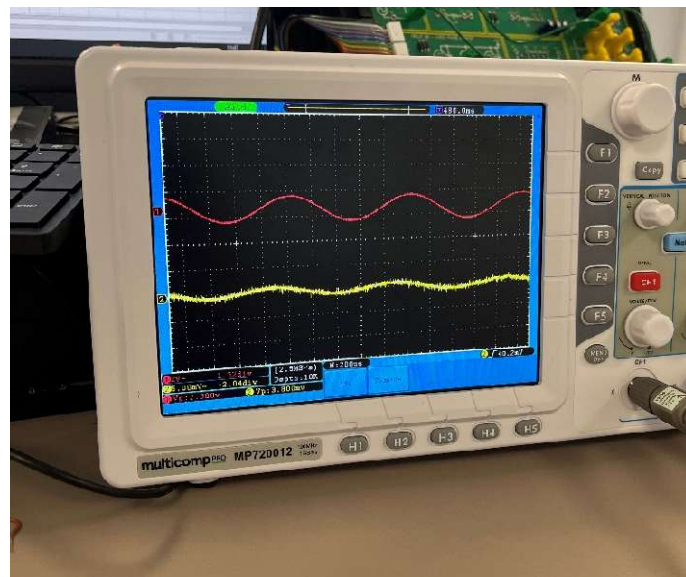


Figure 5: Input and output waves displayed on the oscilloscope

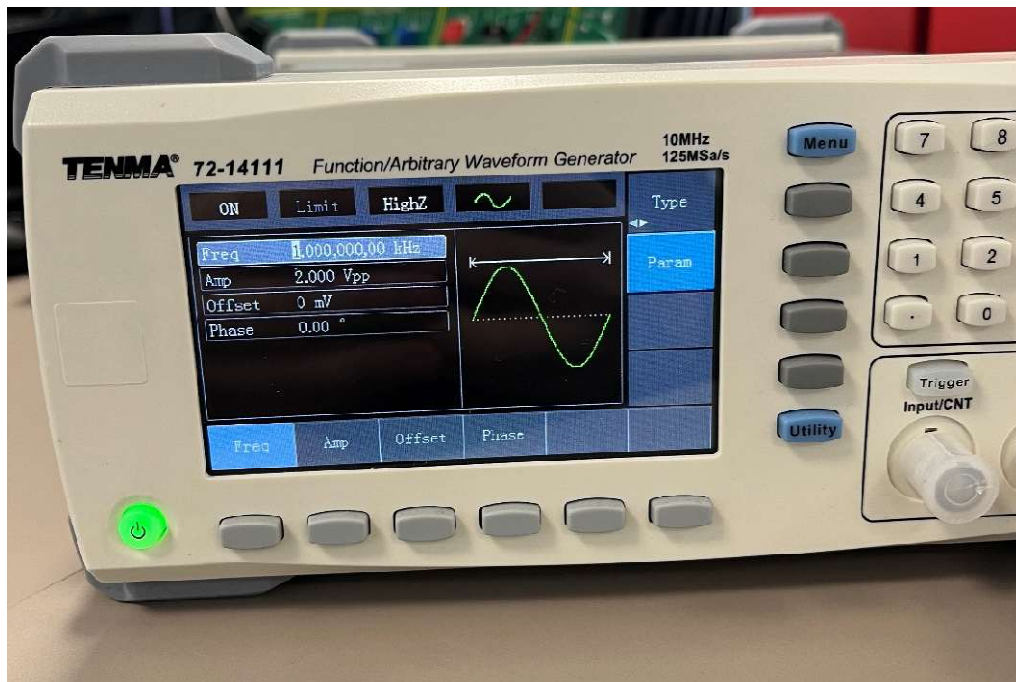


Figure 6: Signal generator setup

3.2 Breadboard Circuit Results

Once the RLC circuit had been set up on the breadboard, it was then tested using the exact frequencies that were used in the Proteus simulation. The results of the breadboard test were recorded in Table 3 below.

Table 3: Results from the breadboard circuit

Frequency (Hz)	Vin (V)	VL (V)	Gain (ratio)	Attenuation (dB)
1000	2.08	0.004	0.001923	-54.3200669
2000	2.08	0.006	0.002885	-50.7982417
3000	2.08	0.008	0.003846	-48.299467
3500	2.08	0.01	0.004808	-46.3612667
4000	2.08	0.013	0.00625	-44.0823997
4500	2.08	0.018	0.008654	-41.2558166
4800	2.08	0.022	0.010577	-39.5128131
4900	2.08	0.024	0.011538	-38.7570419
5000	2.08	0.025	0.012019	-38.4024665
5100	2.08	0.025	0.012019	-38.4024665
5200	2.08	0.026	0.0125	-38.0617997
5300	2.08	0.025	0.012019	-38.4024665
5400	2.08	0.024	0.011538	-38.7570419
6000	2.08	0.018	0.008654	-41.2558166
7000	2.08	0.012	0.005769	-44.7776418
10000	2.08	0.007	0.003365	-49.4593059
20000	2.08	0.004	0.001923	-54.3200669

From the results obtained in Table 3 above, a semi-log graph of attenuation vs frequency was then plotted. As a result of this, the learner could then find the -3 dB or 'half-power' point, which can be seen in Figure 7 below.

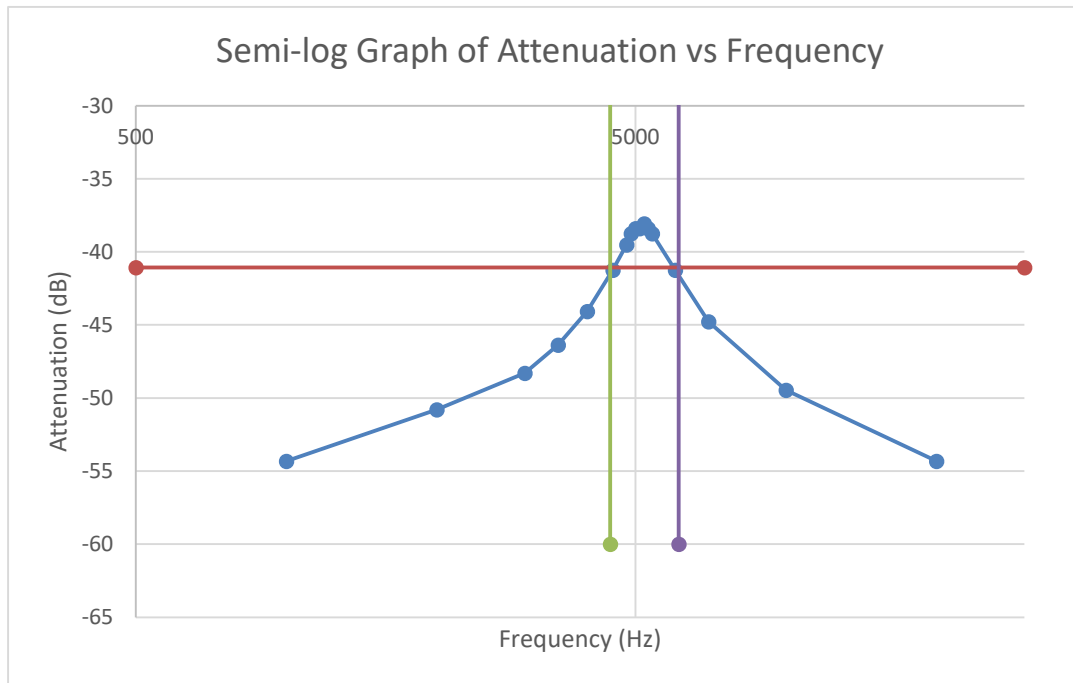


Figure 7: Semi-log graph of Attenuation vs Frequency for breadboard test

As can be seen in Figure 7 above, the horizontal red intersecting line portrays the -3 dB point for the breadboard test. Additionally, the vertical green intersecting line indicates f_1 (4450 Hz), and the purple intersecting line marks f_2 (6100 Hz). These results then made it possible to calculate the bandwidth, which was 1650 Hz. From this graph, the student also obtained the resonant frequency, which was 5200 Hz, and then calculated the Q factor, leading to an outcome of 3.2.

4 Discussion

When comparing the results of both simulations to each other and to theory, there are multiple similarities and differences. For instance, the resonant frequency of the Proteus simulation was 5000 Hz, which is like both the breadboard test and the theory, which are 5200 Hz and 5032.9 Hz, respectively. This is because the Proteus simulation and the theory results have been calculated in an ideal world with no imperfections, whereas the practical experiment has physical elements influencing the results.

Additionally, the graph produced from the Proteus simulation and the graph produced from the breadboard experiment both have a similar shape. However, the graph for the Proteus simulation is narrower than the breadboard simulation, and it also has a higher peak. This caused each method to produce different values for f_1 and f_2 . The simulation produced 4850 Hz for f_1 and 5050 Hz for f_2 , while the breadboard implementation yielded 4450 Hz for f_1 and 6100 Hz for f_2 . As a result of these differences, each simulation yields different bandwidth results.

For the Proteus simulation, the bandwidth is 200 Hz, whereas for the breadboard simulation, the bandwidth is 1650 Hz. Then, when calculating the bandwidth using Equation 4 below and the theory values, the result 159.2 Hz is received.

Equation 4: Formula used to calculate the theoretical bandwidth

$$BW = \frac{f_r}{Q}$$

One of the reasons for this difference is parasitic inductance, which is an unintentional and unavoidable characteristic of all electronic parts and their connections [3]. Furthermore, another factor in this difference may be stray inductance, which can be caused by the test leads and the placement of components on the breadboard, thereby shifting the resonant frequency and altering the Q factor [4].

Moreover, the Q factor received from the Proteus simulation is 25, which is similar to the Q factor calculated from theory using Equation 2, 31.6. However, these values differ significantly from the value received from the breadboard experiment, which is 3.2. Q factor (also known as quality factor) is defined as a dimensionless parameter that describes the efficiency and energy loss in an oscillator or resonator [5]. One of

the causes of the difference in results is when calculating the Q factor with theory, and through simulation, they assume that wired connections have no resistance [6]. Additionally, theory and simulation do not consider the distance between each of the components. This is vital since the resistance of a wire is directly proportional to the length of the wire ($R \propto L$) [7]. This relationship is shown in Figure 8 below.

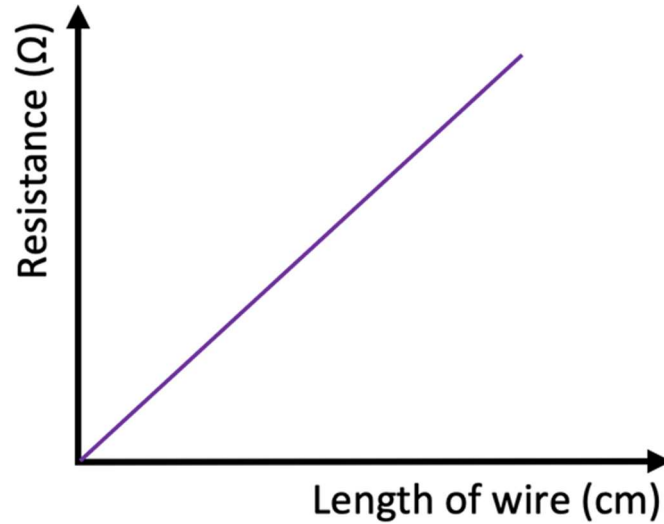


Figure 8: Graph of Resistance vs Length of a wire [7]

One of the additional factors that could have been the cause of the variance in my results is the cross-sectional area of the wires. Wires with a larger cross-sectional area have less resistance to the flow of electric charge, as opposed to wires with a smaller cross-sectional area ($R \propto \frac{1}{A}$) [8]. Furthermore, another factor that affects resistance is the material of the wire. Resistivity is the ability of a material to conduct electric currents and is denoted by the Greek letter rho, ρ [9]. The assumes that the material used in the wires for this experiment is copper, which has a resistivity of $1.72 \times 10^{-8} \Omega\text{m}$, at 20°C [10].

Unaccounted resistance is a major factor contributing to the differences observed between the theoretical, simulated results and those obtained experimentally. The Q factor, defined as a dimensionless measure of efficiency and energy dissipation in resonant systems, directly reflects how losses affect circuit behaviour [5]. Since electrical resistance converts electrical potential energy into thermal energy [11], any unintended energy conversion, such as electrical to thermal, introduces additional losses within the circuit [12], consequently affecting the Q factor.

Furthermore, measurement devices and instruments such as oscilloscopes and signal generators can modify the values measured from the circuit. One of these influences is called the “loading effect”, which changes a circuit's expected behaviour when a measuring device is connected [13]. This is because when a measurement device, such as an oscilloscope, is placed in a circuit, it must draw current from the circuit in order to operate, which forms a new path for the current to flow [13]. Since the oscilloscope draws a portion of the current, the total resistance of that section of the circuit is then decreased, also causing the voltage drop across the component to decrease [13].

An additional potential alteration of practical results can be due to noise and interference. Every measurement includes a collection of undesired signals such as noise, interference and distortion [14]. Also, when comparing the graph obtained from the Proteus simulation to the one received from the breadboard test, it is clear to see that the Proteus simulation has a higher selectivity. Selectivity is a measurement that determines the ability of a receiver to distinguish between desired and undesired signals [15]. The results of the practical experiment show that the circuit has a wide bandwidth, a low Q factor, and a low selectivity. This is due to added resistance that isn't accounted for in the Proteus simulation and means that the circuit doesn't reject nearby frequencies well. Figure 9 below shows a selectivity curve in a parallel RLC circuit.

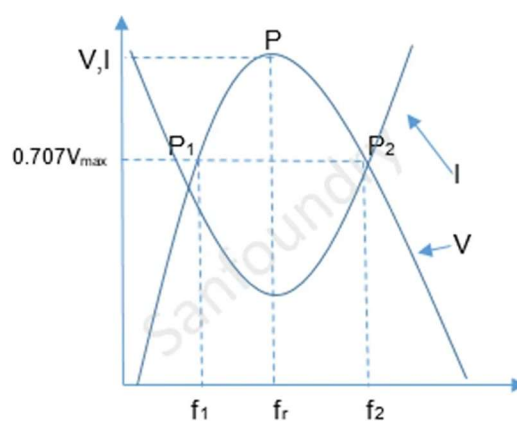


Figure 9: Selectivity curve in parallel RLC circuit [16]

A parallel RLC circuit is known as a rejector circuit because it reaches maximum impedance at its resonant frequency, causing the supply current to drop to a minimum.

The voltage across a parallel resonant circuit will have approximately the same shape as the impedance curve, which can be seen in Figure 9 above. Since the circuit used in this experiment can also be referred to as a rejector circuit, it is fair to say that the Proteus simulation and theoretical results both boast more desirable values than the practical investigation.

Additional factors that can alter the results of this experiment include component values that can vary with the temperature and manufacturing tolerance. Temperature can affect components, whether high or low, especially with semiconductor components, where a 10°C increase can approximately double their failure rate [17]. Although no semiconductor components are used in this experiment, it is still important to recognise when they are present in a circuit. Also, theoretical and Proteus results don't take component tolerances, such as resistors, into account. Resistor tolerance is expressed as a percentage and indicates the extent to which a resistor's resistance can deviate from its stated value [18]. In this experiment, a 1 kΩ resistor with a $\pm 5\%$ tolerance is used, which can be identified by the bands on the resistor. This means that the resistor's resistance can vary between 950 Ω and 1050 Ω. However, this is not only with just resistors, as capacitors and inductors also have manufacturing tolerances.

When comparing the graphs of the Proteus simulation and the practical experiment, it is clear to see that the peak of the breadboard test graph is much lower than the Proteus simulation's graph. This is because an increase in resistance lowers the peak and dampens the curve [19]. Damping produces a flatter response curve, giving a wider bandwidth to the circuit and reducing current magnification by also decreasing the Q factor [19].

5 Conclusion

During this experiment, the student found that the results from the simulation, breadboard and theory had some similarities and differences. It was discovered that the simulation, breadboard and theory had a similar resonant frequency, which was around 5000 Hz. Additionally, the bandwidth determined for the Proteus simulation and theory were both similar and were 200 Hz and 159.2 Hz, respectively. However, it was found that the bandwidth for the breadboard test was 1650 Hz. Furthermore, it was also discovered that the Q factor for the Proteus simulation and theory was similar, which were 25 and 31.6, respectively. It was then identified that the Q factor of the practical experiment was much lower than both of the other values, which was 3.2. In conclusion, the student determined that the reasoning for the differences between the theory, Proteus simulation results and the breadboard test could have been due to a multitude of factors, such as parasitic inductance, temperature, and unaccounted-for resistances like distance between the components, length of the wires, etc.

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