

LOCATION: SWANSEA

LLEOLIAD: ABERTAWE

LEVEL 4

LEFEL 4

EXAMINATION PERIOD

MAY 2024

CYFNOD ARHOLIADAU

MAI 2024

MODULE CODE: GOEE4003

ELECTRICAL AND ELECTRONICS PRINCIPLES

TIME: 2 HOURS

ANSWER ALL QUESTIONS

Equipment or materials required – Calculator, Formula Sheet

Question One (20 Marks)

For the circuit shown in Figure 1 below: -

- i. Calculate the resistance of the circuit within the dashed lines designated the LOAD (i.e. R3 to R8 inclusive) [10 marks]
- ii. Calculate the voltage at point A [3 marks]
- iii. Calculate the **total** power dissipated. In the LOAD [2 marks]
- iv. Calculate the value of the currents I1 and I2 [5 marks]

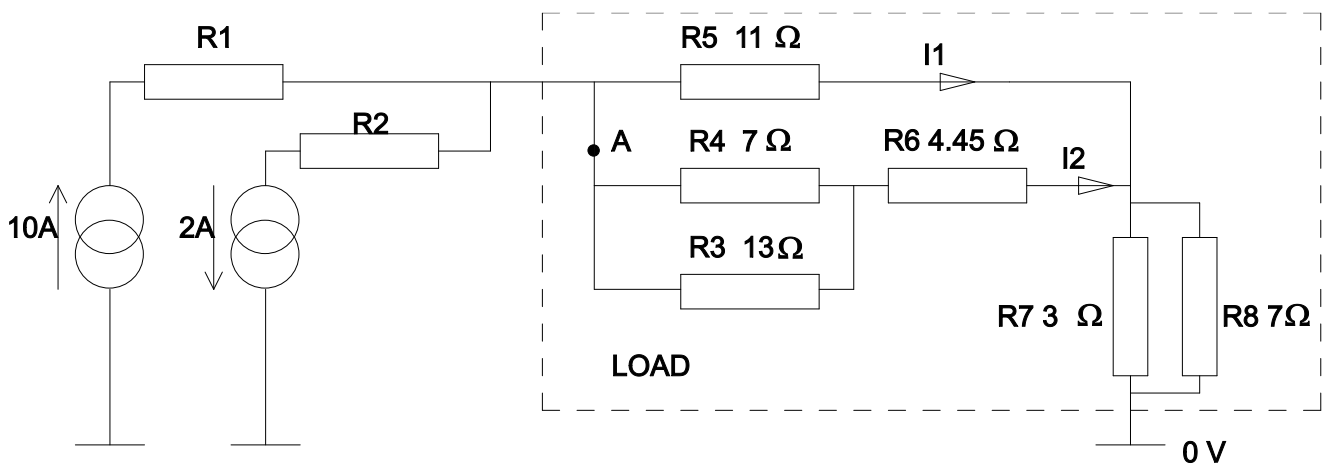


Figure 1

Question Two (30 Marks)

- a) For the circuit in Figure 2, find the branch current I_1 , I_2 and I_3 using mesh analysis. [15 marks]

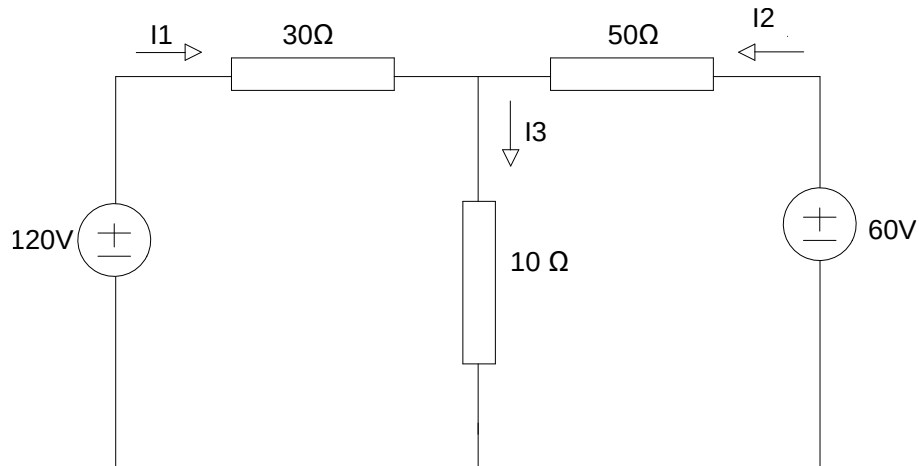


Figure 2

- b. For the circuit shown in Figure 3, find:
- The Thevenin equivalent circuit for the network [8 marks]
 - The value of the adjustable resistance R that results in maximum power transfer across the terminals AB [2 marks]
 - The maximum power transferred in the load [2 marks]
 - Find Norton's equivalent circuit for the network. [3 marks]

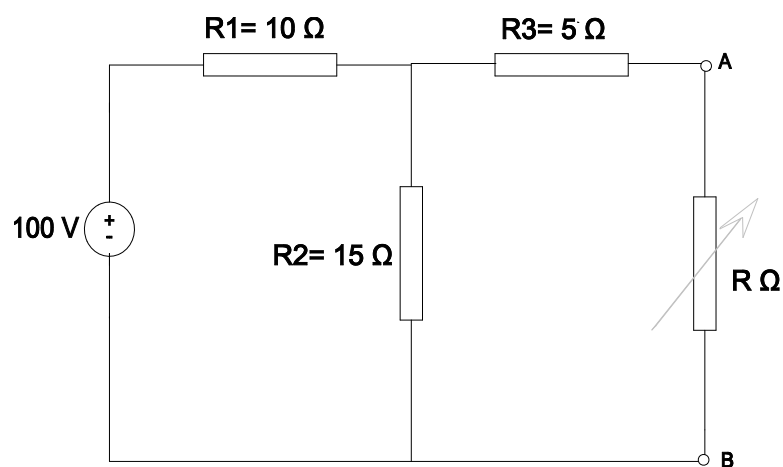


Figure 3

Question Three (20 Marks)

A $100\mu\text{F}$ capacitor in series with a coil of resistance 8Ω and inductance 150mH is connected to a 240V , 50Hz a.c. supply as shown in Figure 4. Calculate:

- | | | |
|------|---|-----------|
| i. | The circuit impedance | [9 marks] |
| ii. | The current flowing in the circuit | [2 marks] |
| iii. | The voltage across the coil | [2 marks] |
| iv. | The voltage across the capacitor | [2 marks] |
| v. | The phase angle between voltage and current | [2 marks] |
| vi. | The real power dissipated | [3 marks] |

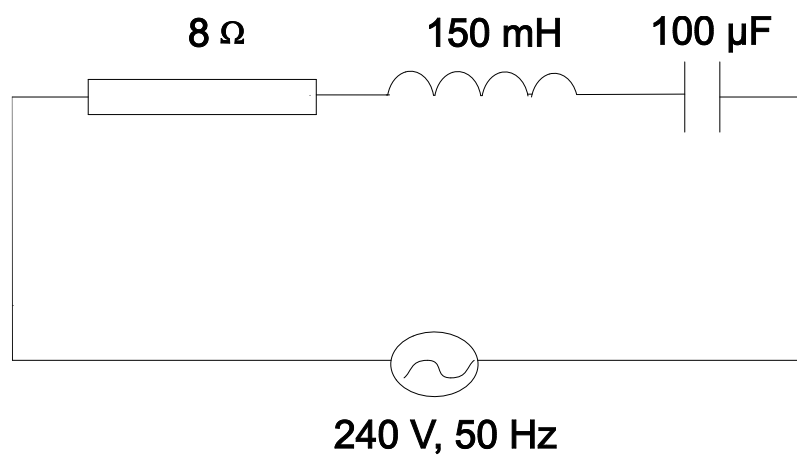


Figure 4

Question Four (30 Marks)

a. Figure 5 below shows a coupled two stage amplifier circuit. Calculate:

- i. The DC current through R_1 and R_2 . [2 mark]
- ii. The DC voltage across R_1 and R_2 . [2 mark]
- iii. The DC voltage at the emitter for first stage. [1 mark]
- iv. The DC emitter and collector currents for first stage. [1 mark]
- v. The DC voltage at the collector for first stage. [1 mark]
- vi. The DC emitter voltage for the second stage. [1 mark]
- vii. The DC emitter current for the second stage. [1 mark]
- viii. The DC voltage at collector for the second stage. [1 mark]

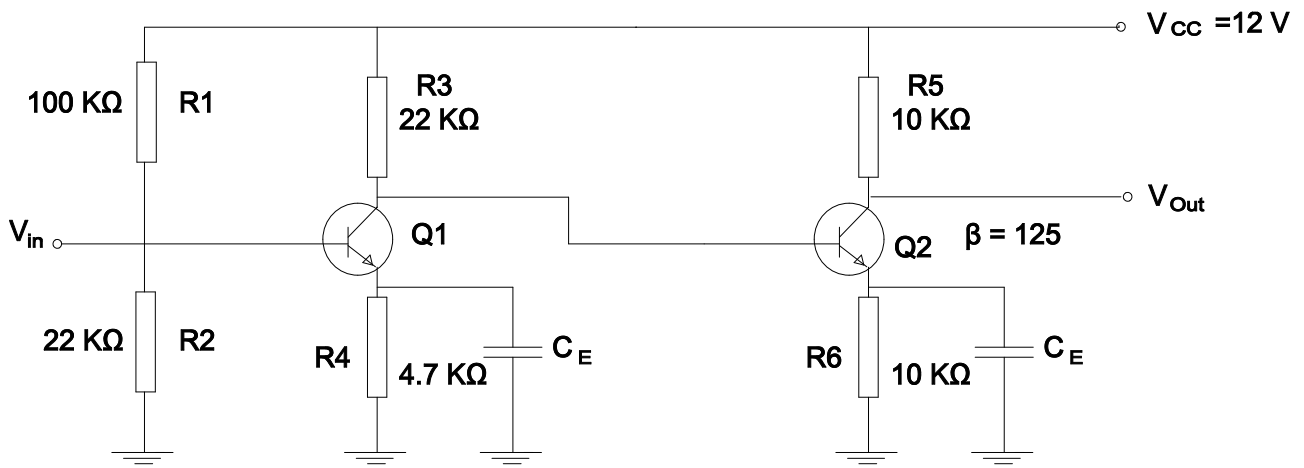


Figure 5

b. Draw the logic circuit design for the following Boolean equations below.

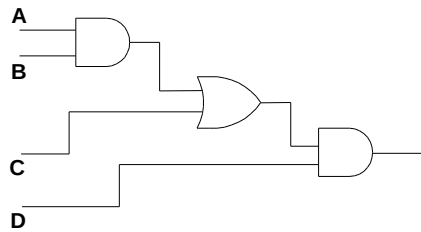
[9 marks]

- i. $Z = A \cdot \bar{B} + C$
- ii. $Z = \bar{A} \cdot (B \oplus C)$
- iii. $Z = A \cdot (B + \bar{B} \cdot C)$

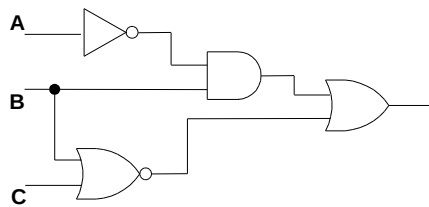
c. Write Boolean algebraic expressions for the circuits below.

[6 marks]

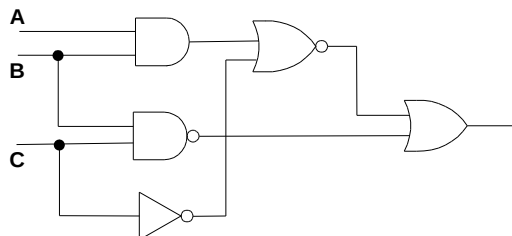
i.



ii.



iii.



d. Simplify the output function X using DeMorgan's theorem.

$$X = \overline{(\overline{A} \cdot \overline{B})(\overline{A} + C)}$$

[5 marks]

End