

MARKING CRITERIA AND STUDENT FEEDBACK

This section details the assessment criteria. The *extent* to which these are demonstrated by you determines your mark. The marks available for each criterion are shown. Lecturers will use the space provided to comment on the achievement of the task(s), including those areas in which you have performed well and areas that would benefit from development/improvement.

Common Assessment Criteria Applied	Marks available	Marks awarded
1. Research-informed Literature Extent of research and/or own reading, selection of credible sources, application of appropriate referencing conventions	10	5
Has applied some research, including sources retrieved independently. Referencing conventions mostly consistently applied.		
2. Knowledge and Understanding of Subject Extent of knowledge and understanding of concepts and underlying principles associated with the discipline.	30	23.5
Excellent knowledge and understanding of the main concepts and key theories. This is reflected in the understanding of the circuit functions and the design work.		
3. Analysis Analysis, evaluation and synthesis, logic, argument and judgement, analytical reflection, organisation of ideas and evidence	20	11
Evidence of some logical, analytical thinking. Has analyse new data and situations without guidance.		
4. Practical Application and Deployment Deployment of methods, materials, tools and techniques, application of concepts, formulation of innovative and creative solutions to solve problems	30	24
Excellent practical work, very little guidance was needed. All relative results were obtain and showed a clear understanding of the design work.		
5. Skills for Professional Practice Attributes in professional practice, individual and collaborative working, deployment of appropriate media, presentation and organisation	10	6.5
Work is coherent and fluent and is well structured and organised.		

Assignment Mark (Assessment marks are subject to ratification at the Exam Board. These comments and marks are to give feedback on module work and are for guidance only until they are confirmed.)	Late Submission Penalties (tick if appropriate)		70%
	Up to one week late		
	First Attempt?	✓	



School of Applied Computing ASSIGNMENT SPECIFICATION

Student name:	Thomas Wolsey	Student P number:	
Programme:	HND Electrical/Electronic Engineering		
Lecturer:	Jason Pointer	Internal Verifier:	Steve Roberts
Assignment Title:	Digital Circuits		
Hand Out Date:	23/03/18	Submission deadline:	11/05/18

Referencing:	In the main body of your submission you must give credit to authors on whose research your work is based. Append to your submission a reference list that indicates the books, articles, etc. that you have read or quoted in order to complete this assignment (e.g. for books: surname of author and initials, year of publication, <u>title of book</u> , edition, publisher: place of publication).		
Disclosure:	I declare that this assignment is all my own work and that I have acknowledged all materials used from the published or unpublished works of other people. All references have been duly cited.		
Student's Signature:	<i>Hardcopy assignments will not be accepted without a signature here</i>	Date:	

Late submission will result in a late penalty mark, as follows:

Up to one week late, maximum mark of 40% for first attempts and 0% for resubmissions.

{Academic Quality Handbook 2015/16 7.5 (5)}

Learning Outcomes tested (from module syllabus)

1. Demonstrate an understanding of semi-conductor components and characteristics and their application in analogue and **digital** electronic circuits.
2. To design, simulate, build, test and evaluate analogue and **digital** electronic circuits using information gained from datasheets.

Tom Wolsey 126039
PSDE 4004 - ELECTRONICS 1
Assignment 3 - Digital Circuits
Jason Pointer

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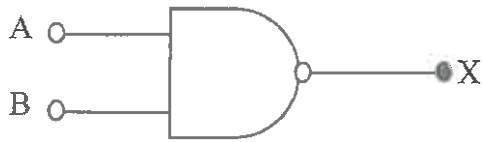
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Part 1 - Combinational Logic

Construct and test the following circuits using NAND gates. For each circuit complete a truth table and measure the logic value at each point indicated in the truth table. Write down the simplified Boolean expression and check that the measured values agree with the expected values.

Write in a part line

(a)

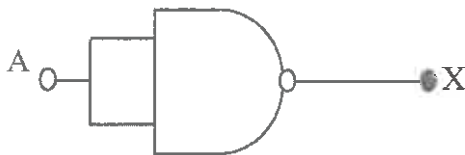


A	B	X
0	0	1
0	1	1
1	0	1
1	1	0

$$X = \overline{A \cdot B}$$

The results above match the expected results

(b)

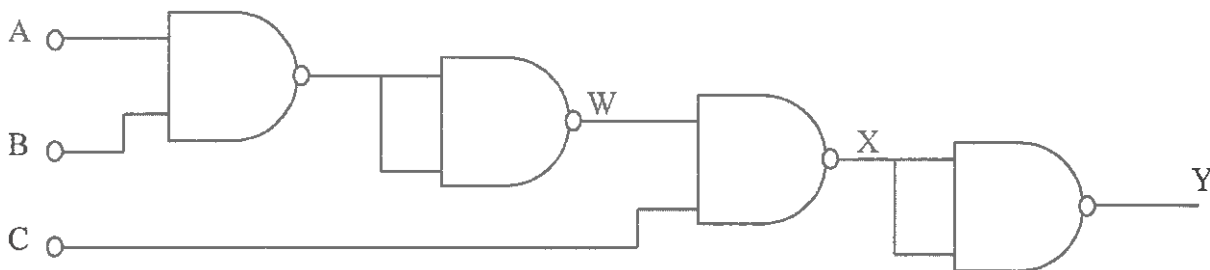


A	X
0	1
1	0

$$X = \overline{A}$$

The results above match the expected results

(c)



A	B	C	W	X	Y
0	0	0	0	1	0
0	0	1	0	1	0
0	1	0	0	1	0
0	1	1	0	1	0
1	0	0	0	1	0
1	0	1	0	1	0
1	1	0	1	1	0
1	1	1	1	0	1

State the logic function for W, X and Y and simplify.

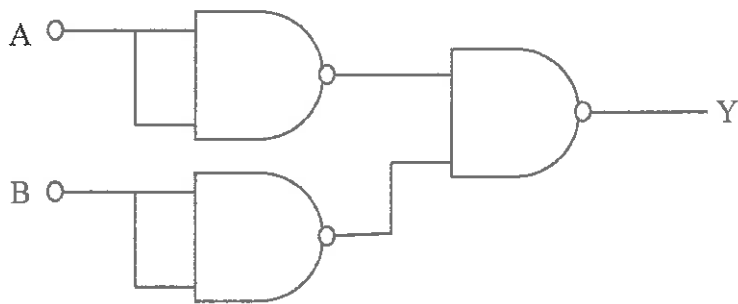
$W = A.B.C' + A.B.C$ simple = $A.B$. 2 input AND gate

$X = A.'B.'C' + A.'B.'C + A.'B.C' + A.'B.C + A.B.'C' + A.B.'C + A.B.C'$ simple = $\overline{A.B.C}$

$Y = A.B.C$ simple = $A.B.C$

These results match the expected outcomes.

(d) What will be the output of the circuit below? If A of circuit (b) is connected to Y what will be the new output.



A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

$$\bar{A}B + A\bar{B} + AB$$

$$A+B$$

OR Gate

A	B	X
0	0	1
0	1	0
1	0	0
1	1	0

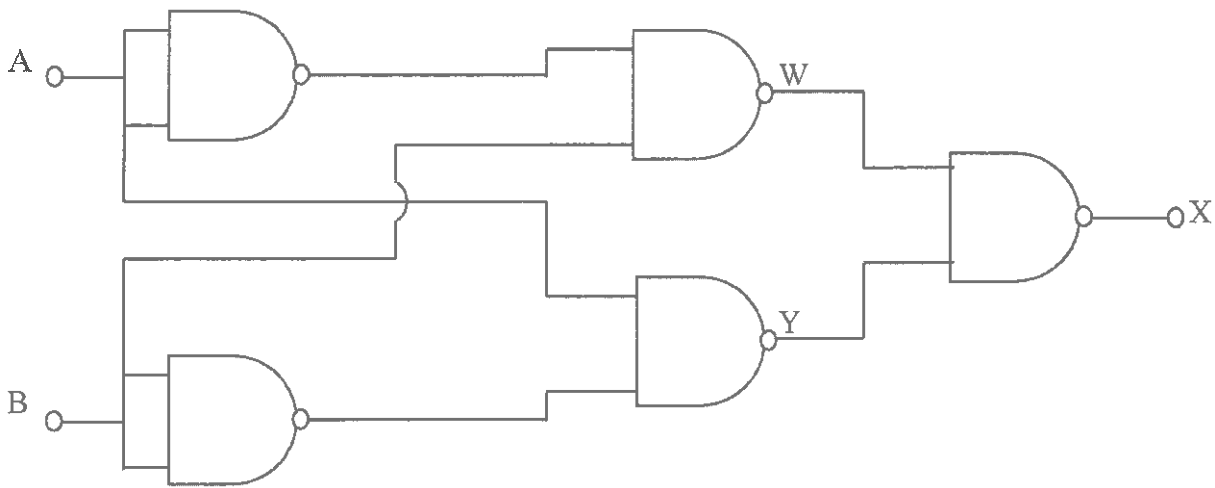
$$\overline{A+B}$$

$$\overline{A+B}$$

NOR gate

The results above match the expected results.

- (e) Construct the following circuit and measure the logic values at W, Y and X. Determine the output equation and confirm that the theoretical values agree with the measured values.



W

A	B	X
0	0	1
0	1	0
1	0	1
1	1	1

$$\bar{A}.\bar{B}+A.\bar{B}+A.B$$

$$\bar{B}+A$$

XOR Gate

$$x = \bar{A}.\bar{B}+A.\bar{B}+A.B$$

$$x = \bar{A}.\bar{B}+A(\bar{B}+B)$$

$$x = \bar{A}.\bar{B}+A \text{ Rule 13 Handout}$$

$$x = A+B$$

Y

A	B	X
0	0	1
0	1	1
1	0	0
1	1	1

$$x = \bar{A}.\bar{B}+A.\bar{B}+A.B$$

$$x = \bar{A}.\bar{B}+B(\bar{A}+A)$$

$$x = \bar{A}.\bar{B}+B$$

$$x = \bar{A}+B$$

X

A	B	X
0	0	0
0	1	1
1	0	1
1	1	0

$$\bar{A}.B + A.\bar{B}$$

$$X = \bar{A}.B + A.\bar{B}$$

XOR

The results above match the truth tables when compared.

1.

Compare the following logic families:

There are many differences between the TTL (Transistor-Transistor Logic) and CMOS (Complementary Metal Oxide Semiconductor), some of the difference are that a TTL chips tend to consume a lot more power compared to CMOS chips especially at rest. Whereas the TTL has a very fast switching speed compared to the CMOS. The CMOS has a higher input voltage of 8V to 9V whereas the TTL has an input range of 2.4V to 5V. The CMOS is more suited to portable appliances.

- ECL

ECL is based on use of current steering switch realised using differential transistor pair. ECL is fastest logic family among all and this is due to avoidance of saturation region for application.

Following are characteristics of ECL logic family.

- propagation rate is about 1 to 2ns
- Noise immunity and power dissipation is worst of all the logic families.
- High Level is -0.8V and Low Level is -1.8V
- It has differential input amplifier, Internal temperature and voltage compensated bias network, emitter follower outputs •

ECL gates provide both true as well as complemented outputs.

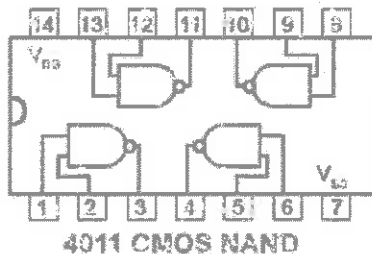
- TTL

Power dissipation is usually 10 mW per gate. Propagation delays are 10 nS when driving a 15 pF/400-ohm load. Voltage levels range from 0 to V_{cc} where V_{cc} is typically 4.75V - 5.25V. Voltage range 0V - 0.8V creates logic level 0. Voltage range 2V - V_{cc} creates logic level 1.

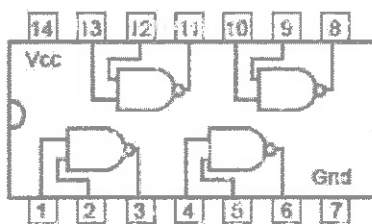
CMOS

The power dissipation is dependent on the power supply voltage, frequency, output load, and input rise time. At 1 MHz and 50 pF load, the power dissipation is typically 10 nW per gate.

Short propagation delays depend on the power supply, the propagation delays are usually around 25 nS to 50 nS.



4011 CMOS NAND



7400 TTL NAND

Specification	TTL	ECL	CMOS
Basic gate	NAND	OR/NOR	NAND/NOR
Fanout	10	25	>50
Power per gate(mWatt)	1-22	4-55	1 @ 1MHz
Noise Immunity	Very Good	Good	Excellent
t _{PD} (ns)	1.5-33	1-4	1-200
Advantages and disadvantages of	<u>TTL>></u>	<u>ECL>></u>	<u>CMOS>></u>

From the website <http://www.rfwireless-world.com/Terminology/Difference-between-TTL-ECL-CMOS.html>, the table above is comparing the three different logic family's.

2.

Simplify the following Boolean equations, ONLY using the LAWS OF BOOLEAN ALGEBRA and DeMORGANS THEOREM. Verify your findings by constructing the logic circuits using NAND gates.

Below can be seen the simplified boolean expressions, and circuits.

i) $F = A(A + \bar{B})$

$$F = A.B + A.\bar{B}$$

$$F = A + A.\bar{B} = A(1 + \bar{B}) = A$$



ii) $F = (A + B)(C + A)$

$$F = A.C + A.A + B.C + B.A$$

$$F = A.C + A + B.C + B.A$$

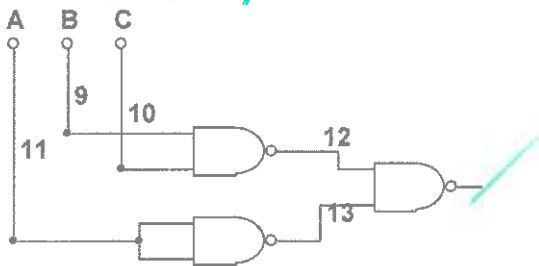
$$F = A(C + 1 + B) + (B.C)$$

$$F = A + (B.C)$$

$$\bar{F} = \overline{A + (B.C)}$$

$$\bar{F} = \bar{A} \cdot \overline{(B.C)}$$

$$F = \overline{\bar{A} \cdot \overline{(B.C)}}$$



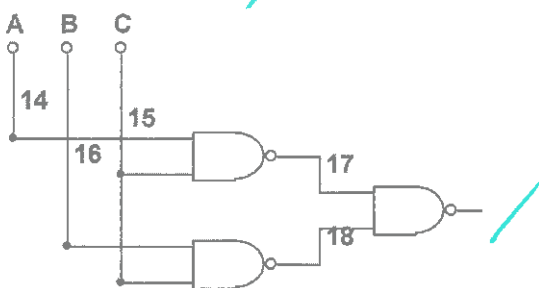
iii) $F = (A + B)C$

$$F = A.C + B.C$$

$$\bar{F} = \overline{A.C + B.C}$$

$$\bar{F} = \overline{A.C} \cdot \overline{B.C}$$

$$F = \overline{\overline{A.C} \cdot \overline{B.C}}$$



iv) $F = (\bar{A} + \bar{B} + \bar{C})(A + \bar{B} + \bar{C})(A + C)(B + \bar{C})$

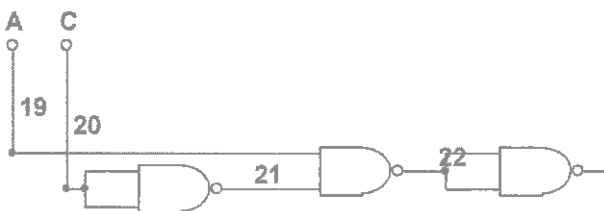
$$F = (\bar{B} + \bar{C})(A + C)(B + \bar{C})$$

$$F = \bar{C}(A + C)$$

$$F = \bar{C}.A + \bar{C}.C$$

$$F = \bar{C}.A + 0$$

$$F = \bar{C}.A$$



Need to verify

Part 2 - Using Combinational Logic to Solve Real Problems

(a)

Below is a 4-bit binary code with the range of numbers 1010 to 1111 not used. A circuit was designed that will detect these invalid codes. The circuit was then made and verify that it performs the required task.

Use the following method: State problem → Construct truth table → Extract Boolean expression → Simplify expression → Construct logic diagram.

A	B	C	D	X
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

$$x = a\bar{b}c\bar{d} + a\bar{b}cd + ab\bar{c}\bar{d} + ab\bar{c}d + abc\bar{d} + abcd$$

AB	CD				
		0	1	11	10
0					
1					
11				1	1
10				1	1

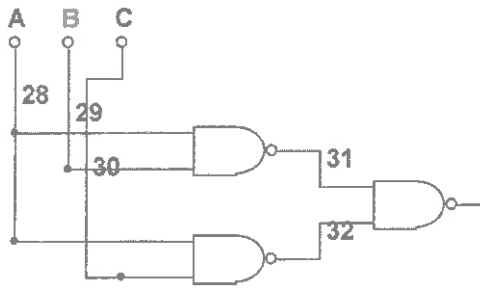
$x = A.B + A.C$

DeMorgan

$$\bar{X} = \overline{A.B + A.C}$$

$$\bar{X} = \overline{(A.B) . (A.C)}$$

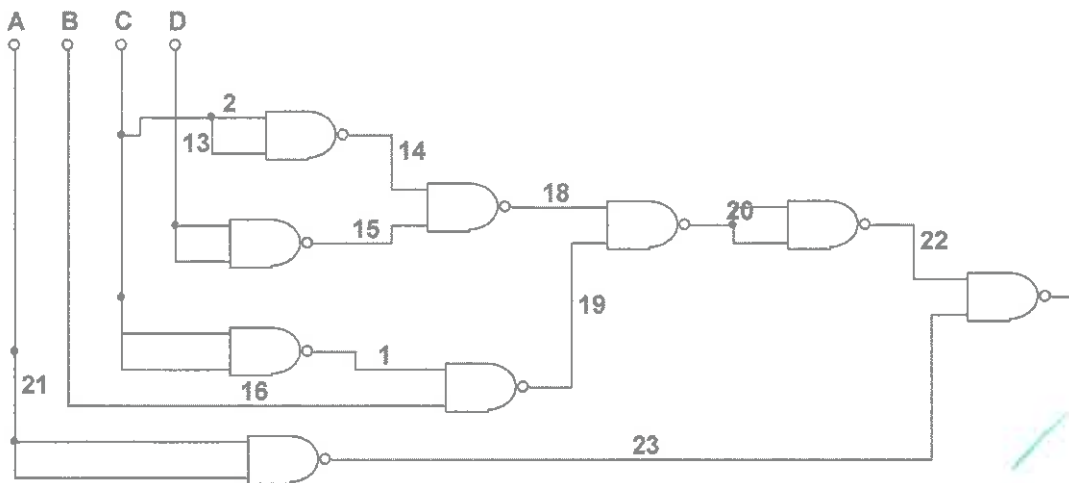
$$X = \overline{(A.B) . (A.C)}$$



The circuit when designed and constructed it functioned as per the requirements in the specification.

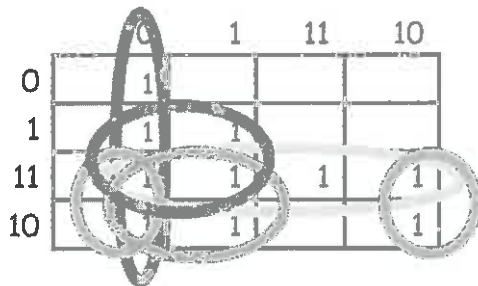
(b)

Below a 2-bit comparator where by the output is HIGH when the one of the two-bit number is equal to or greater than a second two-bit number. The comparator was built and confirm that it operated correctly.



Bit 1		Bit 2		X
A	B	C	D	
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

AB,CD



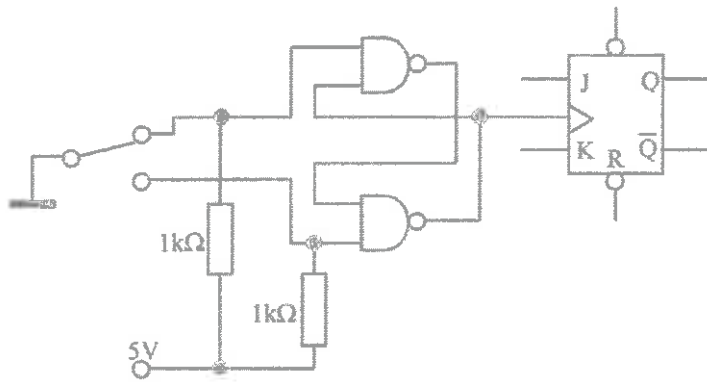
$$X = \bar{C}\bar{D} + A\bar{D} + A\bar{C} + AB + B\bar{C}$$

The circuit when designed and constructed it functioned as per the requirements in the specification.

Part 3 - Sequential Logic

The truth table of the J-K Flip-Flop

- (a) Construct the following circuit on the Logic Tutor, monitoring the clock, Q and $\bar{Q}$ outputs with the on-board LEDs.



(b) Complete Table 1, entering an x for 'don't care states'.

Inputs					Outputs	
Preset (S)	Clear (R)	Clock	J	K	Q	$\bar{Q}$
0	1	X	X	X	1	0
1	0	X	X	X	0	1
0	0	X	X	X	1	0
1	1		L	L	0	1
1	1		H	L	1	0
1	1		L	H	0	1
1	1		H	H	1	0

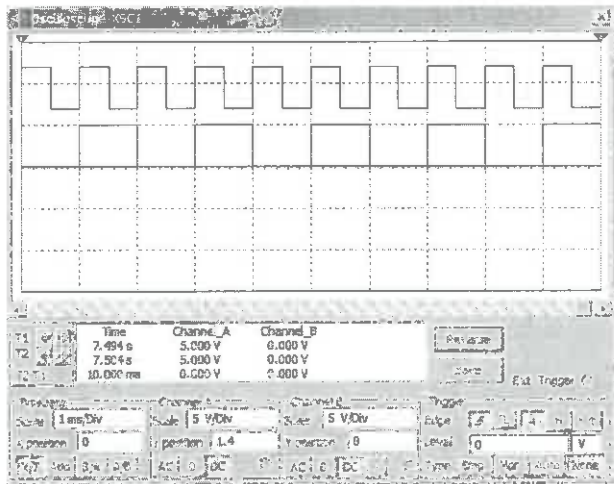
(c) Your observations should enable you to answer the following questions:

- What is significant about the output state when Preset = Clear = Logic '0'?
It provides a test to make sure that Q and not Q are functional. It can also be used to test the output device.
- At what part of the clock pulse is the input data transferred to the device?
It triggers on the negative edge and transfers the data on logic 0 of the clock.
- At what part of the clock pulse is the output data transferred to the output?
The data is transferred to the output on the negative edge or logic 0.
- What clock triggering action does the SN7476 have?
The SN7476 has a negative edge triggering action.
- The cross-coupled NAND gates are for switch debouncing. Why are they needed and how do they work?

Debouncing is needed to help when using a mechanical switch, as the physical inputs makes and breaks connection several times in a very short period, which may not be observable visually, this then causes the bouncing effect. The gates help by latching the circuit on or off there for stopping any bounce coming through. Debouncing is not only used for circuits it's also used for software as well.

(d) Frequency division properties of J-K Flip-Flops

- Replace the existing clock circuit with the TTL output of the signal generator.
- Set the generator to 1kHz and Preset = Clear = J = K = '1'.
- Connect the oscilloscope to both the clock input and Q output and sketch the two observed waveforms above each other on the same time axis.



When the clock input occurs q changes to the opposite state, or it toggled.

(e) Asynchronous Counters

- Construct the following circuit, with J = K = '1' for both flip-flops.
- Connect the Q outputs to LEDs, and the clock input to the one-shot signal generator on the Logic Tutor.
- Clear the counter and apply successive clock pulses and record the Q outputs in Table 3(a).

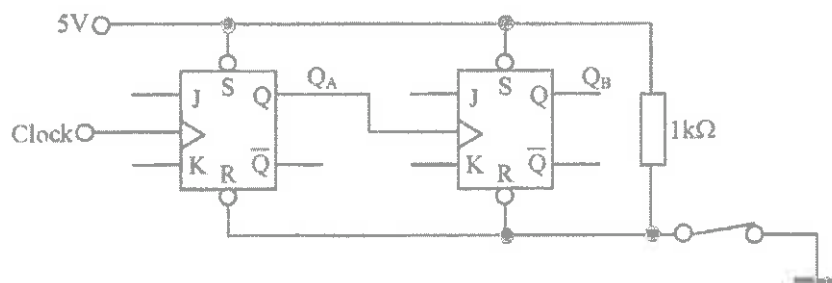
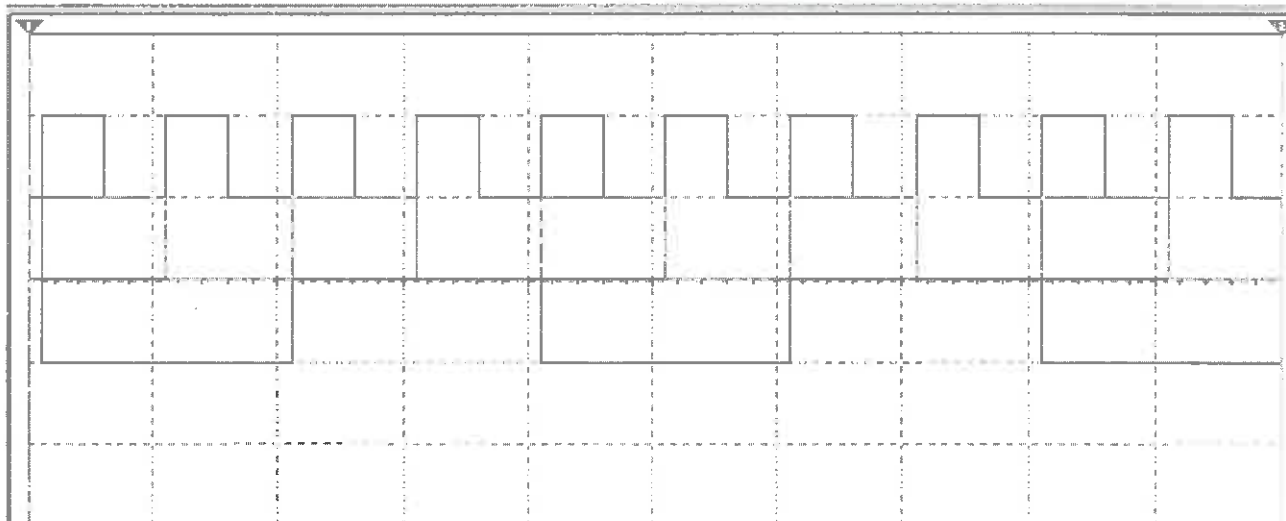
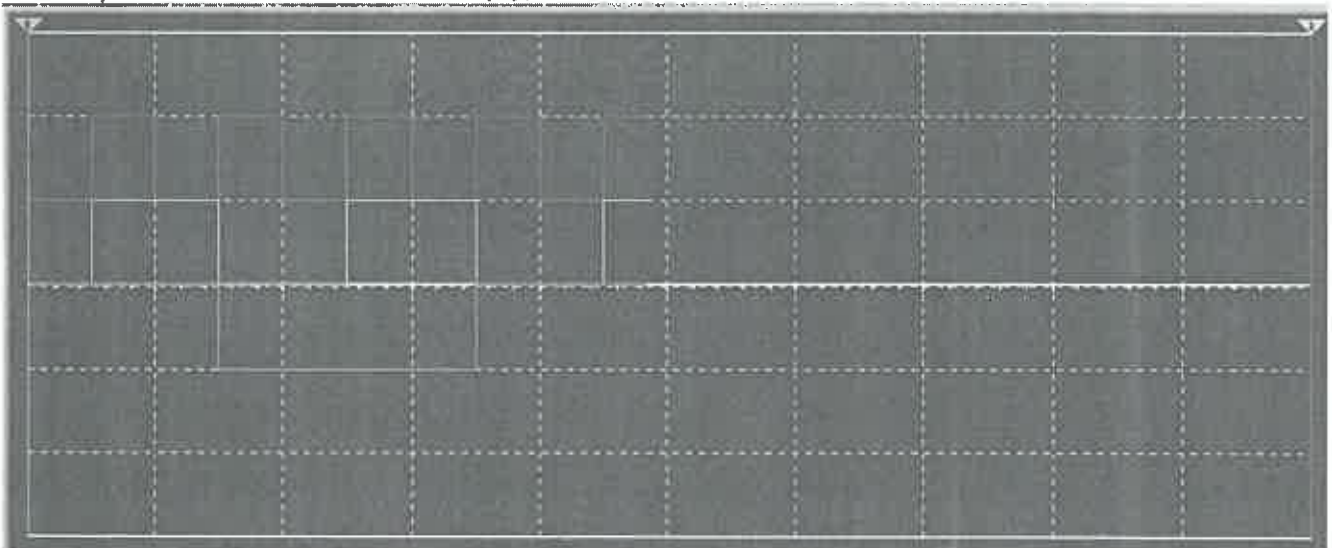


	Table 3(a)		Table 3(b)	
Pulse	QA	QB	QA	QB
Clear	0	0	0	0
1	1	1	1	0
2	0	1	0	1
3	1	0	1	1
4	0	0	0	0
5	1	1	1	0

iv) Now substitute the one-shot clock signal for the low frequency clock on the Logic Tutor and sketch the Clock, QA and QB output waveforms above each other on the same time axis.



v) Transfer the clock connection from the Q to QBAR output and repeat the above, enter your results in Table 3(b), and sketch the waveforms as before.

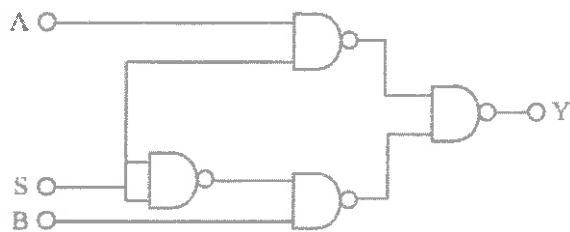


vi) What is the difference between the two circuits?

The difference is that the first circuit counts forward and the second one is counting backwards.

↑
Not clear

(f) Up / Down Selector



i) Construct the two-input multiplexer circuit shown below.

ii) Construct a truth table to prove that when $S = '1'$, Y follows A , when $S = '0'$, Y follows B

A	B	Y
0	0	0
0	1	0
1	0	1
1	1	1

$S = 1$

A	B	Y
0	0	0
0	1	1
1	0	0
1	1	1

$S = 0$

iii) Connect the multiplexer circuit in between the two flip-flops such that Q is connected to A , $\overline{Q}$ to B and Y to the clock input of the second flip-flop.

iv) Confirm that your counter counts up or down, depending on whether S is '1' or '0'. The circuit counts up when 1 down when 0 this has been confirmed.

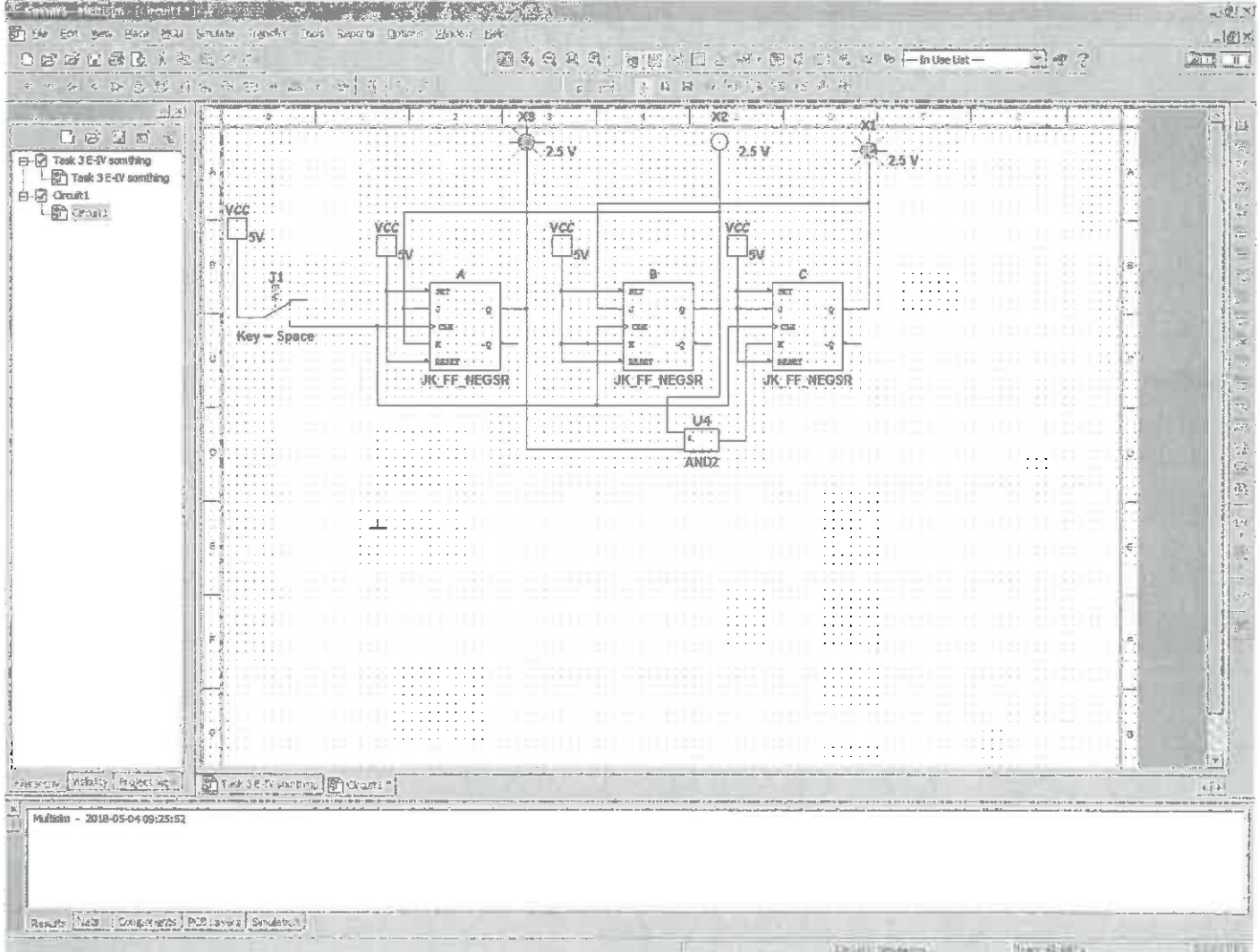
Part 4 - Using Sequential Logic to Solve Real Problems

Design and simulate a 3-stage synchronous binary counter that will produce the odd numbers (including zero) in the range 0 to 7.

Below can be seen the steps it took to build a 3 stage synchronous binary count that produces odd numbers between 0 and 7.

R Reset			Next			Input					
Q_a	Q_b	Q_c	Q_a	Q_b	Q_c	J_a	K_a	J_b	K_b	J_c	K_c
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	1	0	X	1	X	X	0
0	1	1	1	0	1	1	X	X	1	X	0
1	0	1	1	1	1	X	0	1	X	X	0
1	1	1	0	0	0	X	1	X	1	X	1

JA	QB QC					KA	QB QC				
QA		00	01	11	10	QA		00	01	11	10
	0	0	0	1	x		0	x	x	x	x
	1	x	x	x	x		1	x	0	1	x
JA = QB						KA = QB					
JB	QB QC					KB	QB QC				
QA		00	01	11	10	QA		00	01	11	10
	0	0	1	x	x		0	x	x	1	x
	1	x	1	x	x		1	x	x	1	x
JB = QC						KB=1					
JC	QB QC					KC	QB QC				
QA		00	01	11	10	QA		00	01	11	10
	0	1	x	x	x		0	x	x	0	x
	1	x	x	x	x		1	x	0	1	x
JC = 1						KC = QA.QB					



The circuit when designed and constructed functioned as per the requirements in the specification. This can be seen partly from the screen shot above.

Reference

Switch Bounce and How to Deal with It. 2018. Switch Bounce and How to Deal with It. [ONLINE] Available at: <https://www.allaboutcircuits.com/technical-articles/switch-bounce-how-to-deal-with-it/>. [Accessed 25 May 2018].

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