



Complete, fold and seal
(see note 2 below)

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Examination Answer Books

12 Pages

Instructions to Candidates

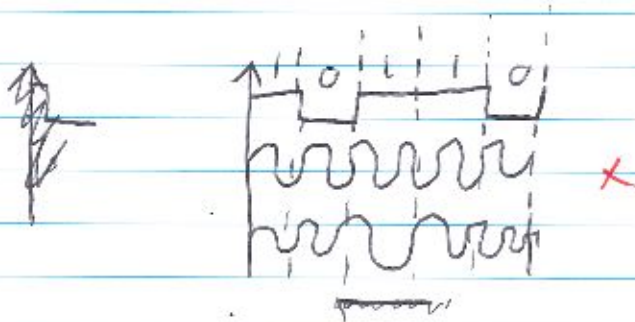
1. Please give the information requested in the boxes below.
2. Enter your name in the space provided to the right, fold over and seal down (using the label provided) to hide your name.
3. The answers must be legibly written. The Examiners can either ignore illegible script or have it typed and the expense of typing charged to the candidate.
4. Write your answers in ink.
5. Begin each answer on a fresh page. Do all rough work in the answer book and cross it through.
6. No part of this book is to be torn out; it must be handed in complete.
7. If more books than one are used, fasten them together using the tags available from the invigilator(s).
8. Every book must be handed in. In no circumstances may answer books, used or unused, be taken out of the examination venue.

1	Student Number	1909752
2	Title of Examination Paper	Signals and Dig Comms
3	Module Code	SGEE 5005
4	Date and Time of Examination	12/5/22 09:30 - 12:00
5	Examination Venue	
6	Seat Number	
7	Number of Answer Books handed in	

List the numbers of the questions you have attempted	Office Use
A9	
B2 e	
B2 d	
B2 a	
b2 b	
A2	
A5	
A8	
A1	
A	10
B2	21
Total	31 %

~~A7~~ ~~Analogue input voltage is applied to a parallel comparator. Each comparator has a reference voltage derived from voltage divider resistors. Comparator output is applied to a multiplexer to a bit encoder. A bit is held by a latch to produce a digital output. These outputs are held until the next sample instant where the next set of digital values are held. Although flash converters are fast they require a limited amount of comparators. An n -bit conversion requires 2^n comparators. Therefore a 2-bit requires 2 comparators and a 16-bit requires 65536 comparators. Other types of slower converters are counting converter and successive approximation converters.~~

A9 The digital data stream is used to change the frequency of the carrier signal

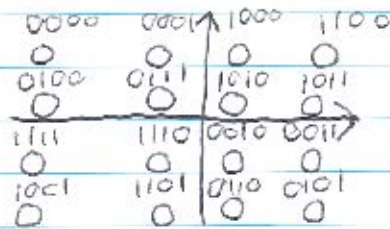


~~B2e~~
B2e

quantisation takes a continuous range of values and replaces them with a binary number. An error occurs between the input voltage and the binary representation this depends on the resolution of the ADC.

4

B2 d The 16-QAM has 4 '1' and 4 '0' which is a total of 16 symbols. there are 3 amplitudes and 3 phase shifts per quadrant. The 16-QAM modulates the phase shift and ~~am~~ amplitude.



1010 Phase Shifts 65° and $0.33 V_{max}$
 1011 Phase Shifts 15° and $0.75 V_{max}$
 1100 Phase Shifts 75° and $0.75 V_{max}$
 1000 Phase Shifts 45° and $1.5 V_{max}$

B2 a $2n = 2^{10} = 1024$
 $PDR = 20 \log 1024 = 60.206 \text{ dB}$
 $q = \frac{32}{1024} = 0.0313$

$V_{QNR} = \frac{0.0313}{\sqrt{12}} = 9.0355 \text{ mV}$

$SNR = \frac{4.7}{9.0355 \times 10^{-3}} = 520.17$

in dB $= 20 \log 520.17 = 54.323 \text{ dB}$

B2b

~~Approximates~~ takes the analogue signal voltage and compares with approximate voltages generated at the DAC output. The Shift register (SAR) is cleared and the DAC output is 0. the conversion is initiated by taking the conversion line Low. The clock pulse sets the MSB to 1. the DAC output is now one half the FSR. if it is greater than FSR/2 then the MSB is latched. if it is lower than FSR/2 it will be taken low by the conversion line. The next clock pulse sends an n bit to the DAC and the DAC output will be FSR/4. if the MSB was latched the DAC becomes 3FSR/4 if the MSB was lost it will remain FSR/4. the analogue input and DAC output will still be compared. if the analogue input is greater than the DAC output it will be latched. if it is lower it will be lost.

6.

A2

$$m = \frac{V_{max} - V_{min}}{V_{max} + V_{min}} = \frac{V_{modulation}}{V_{carrier}}$$

$$= \frac{35 - 9}{35 + 9}$$

$$= \frac{26}{44}$$

$$m = 0.590$$

2

A5

$$VSWR = \frac{1 + |\Gamma_V|}{1 - |\Gamma_V|} = \frac{V_I + V_R}{|V_I| - |V_R|}$$

$$|\Gamma_V| = \frac{Z_L - Z_0}{Z_L + Z_0}$$

$$|\Gamma_V| = \frac{V_R}{V_I}$$

$$|\Gamma_V| = \frac{4}{10} = 0.4$$

3

B(6)

A(5)

$$V_{SWR} = \frac{1+0.4}{1-0.4}$$

$$= 2.3$$

$$\text{or } V_{SWR} = \frac{V_I + V_R}{V_I - V_R}$$

$$= \frac{10+4}{10-4}$$

$$= 2.3 \checkmark$$

$$V_L = V_I + V_R$$

$$V_L = 10+4 = 14V$$

A8

$$P_{\text{sideband}} = \frac{1}{2} m^2 P_{\text{carrier}}$$

$$= \frac{1}{2} \times 0.4^2 \times 2.15$$

$$= 0.172 \quad \times$$

A7

Analogue input voltage is applied to each parallel comparator. Each comparator has a reference voltage derived from a chain of voltage divider resistors. A comparator output is either high (logic 1) or low (logic 0) which is applied to a ~~n~~ level to n bit encoder. n bits are held by a latch to produce a digital output. These outputs are held due to the latch until the next sample instant where the next set of digital output values are held. Although flash converters are fast they ~~require a~~ ~~limited~~ are limited by the amount of comparators. An n bit conversion requires 2^n comparators. therefore n=8 bits requires 256 comparators and n=16 bits requires ~~65536~~ 65536 comparators. Other types of slower ~~comparators~~ converters are counting converters and successive approximation converters.